Advanced Topics in VLSI

EE6361

Jan 2017

Course Objectives

- Introduce students to some relevant advanced topics of current interest in academia and industry
- Make students aware of some advanced techniques
- Make students aware of work happening in India

Current Topics

- Embedded Memory Design
  - DRAMs + Yield Estimation (Janakriaman, IITM)
  - SRAMs (Rahul Rao, IBM India)
  - **TCAMs (Self Study)**
- Electronic Design Automation for Circuits (Sridhar Rangarajan, IBM India)

Learning Objectives for EDRAM

- Explain the working of a (e)DRAM. What is Embedded mean?
- Explain the working of a feedback sense amplifier and modify existing designs to improve performance
- Calculate the voltage levels of operation of various components for an eDRAM
- Introduce stacked protect devices to reduce voltage stress of the WL driver
- Calculate the number of samples required to estimate yield to specified accuracy and confidence
- Explain the use of importance sampling to reduce the number of samples required in step 6

Learning Objectives for SRAM

- Articulate memory hierarchy and the value proposition of SRAMs in the memory chain + utilization in current processors
- Explain SRAM building blocks and peripheral operations and memory architecture (with physical arrangement)
- Articulate commonly used SRAM cells (6T vs 8T), their advantages and disadvantages
- Explain the operation of a non-conventional SRAM cells, and their limitations
- Explain commonly used assist methods
- Explain how variations impact memory cells

Learning Objectives for EDA

- Describe the role of CAD tools in VLSI Physical Design process.
- Explain various design phases and physical design flow
- Articulate the commonly used algorithms in physical design tools
- Detailed understanding of placement and routing techniques.
- Describe the role of physical synthesis in design closure
- Incremental synthesis and optimization and its role in physical design closure

If time permits

- Articulate as how static timing analysis works
- Articulate leakage and dynamic power modelling

Grading

- Assignments – 20%
- Self Study Seminar – 20%
- Quiz – 20%
- End Semester – 40%

Refresher

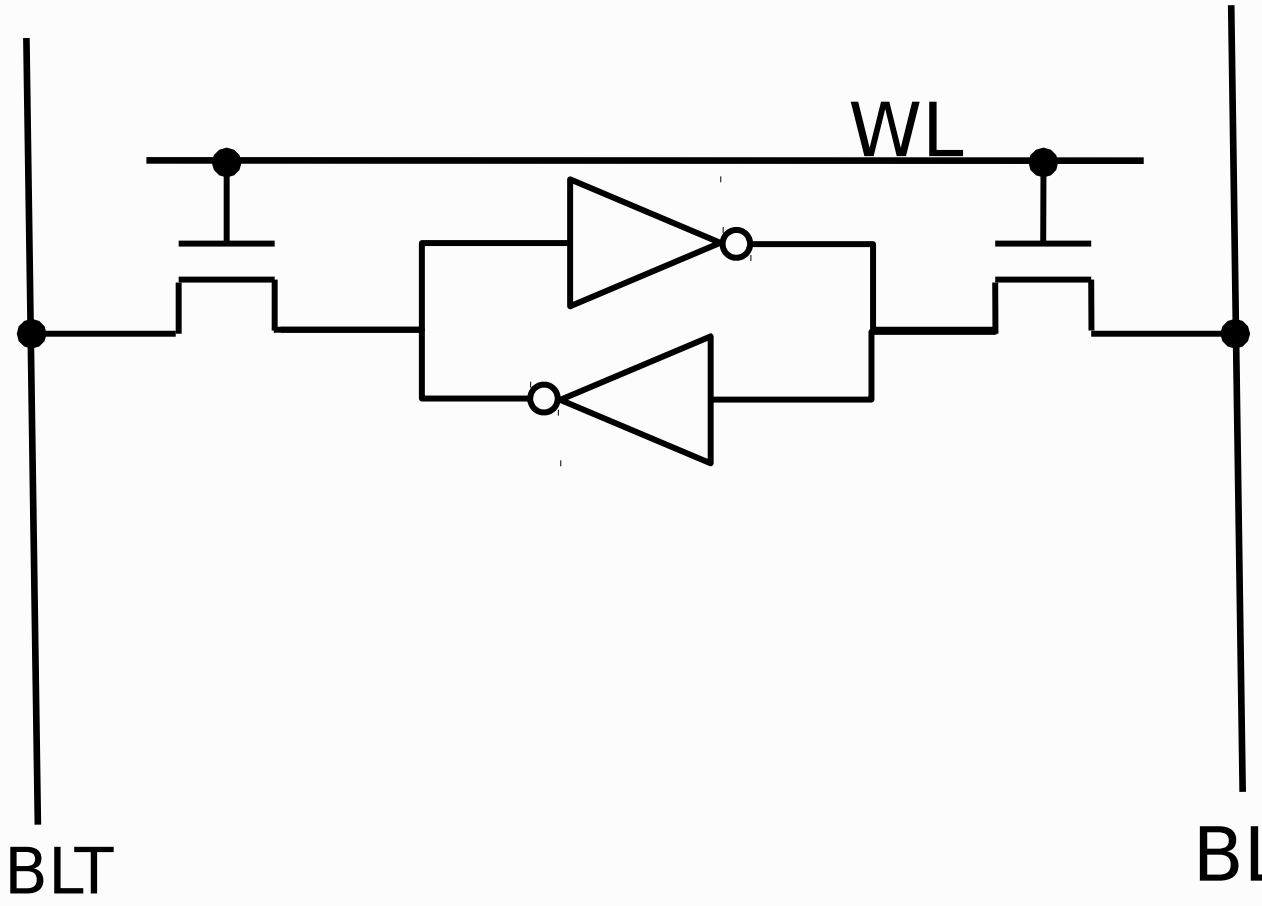
Refresher

- Inverter trip point and noise margins
- Short Channel Effect
  - Sub-threshold leakage
  - DIBL
  - GIDL
- Stacking Effect
- Pass transistors
- 6T SRAM basics

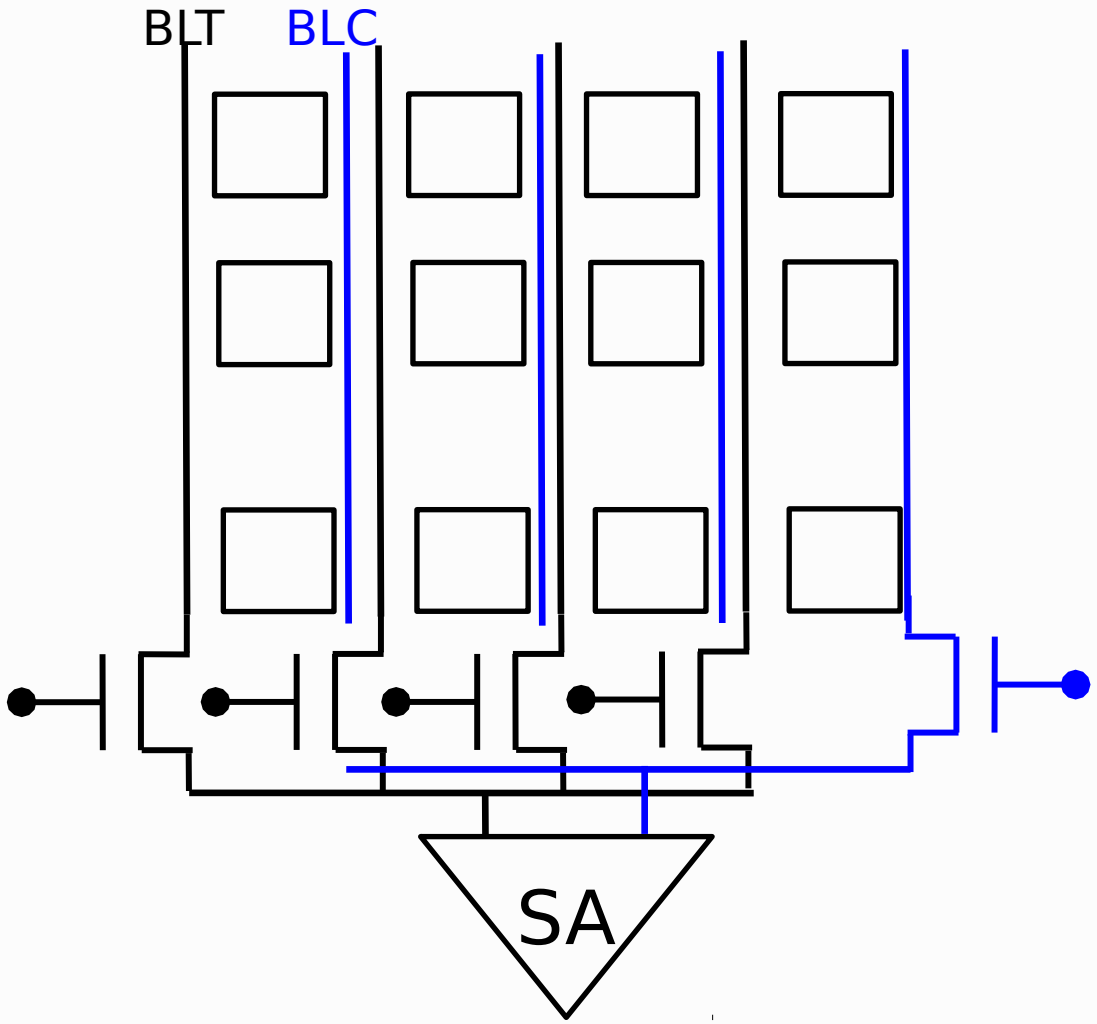
Review of SRAM

- Basic 6T SRAM cell
- Read and Write operation
  - Sizing of devices
- Sense Amps

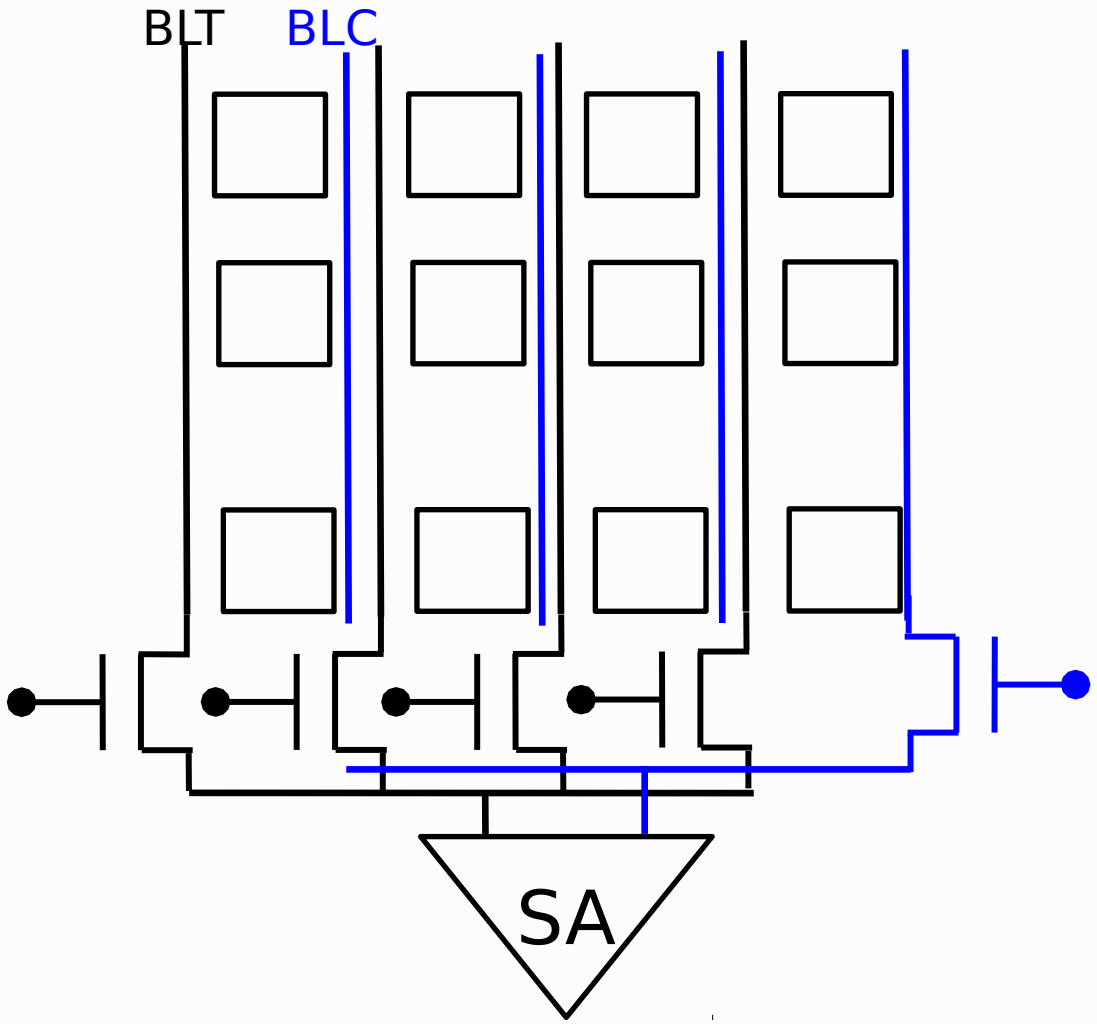
6T SRAM



6T SRAM Array



6T SRAM Array



6T SRAM Array

SRAMs cannot be pre-charged to ground because

- The pull up PFET will malfunction
- The pass transistor is an NFET and hence will not allow a successful read ONE
- The pass transistor is an NFET and hence read ONE will be slow
- Who said you can't precharge to ground?

6T SRAM Array

In an SRAM, PD= Pull down NFET, PU= Pull up PFET and PT=Pass transistor

- ○ PD > PT > PU
- ○ PD > PU > PT
- ○ PU > PT > PD
- ○ Size doesn't matter!

Embedded DRAM

Janakiraman V

Assistant Professor

Electrical Department

IIT Madras

Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example
- References

Acknowledgement

- Raviprasad Kuloor (Course slides were prepared by him)
- John Barth, IBM SRDC for most of the slides content
- Madabusi Govindarajan
- Subramanian S. Iyer
- Many Others

Topics

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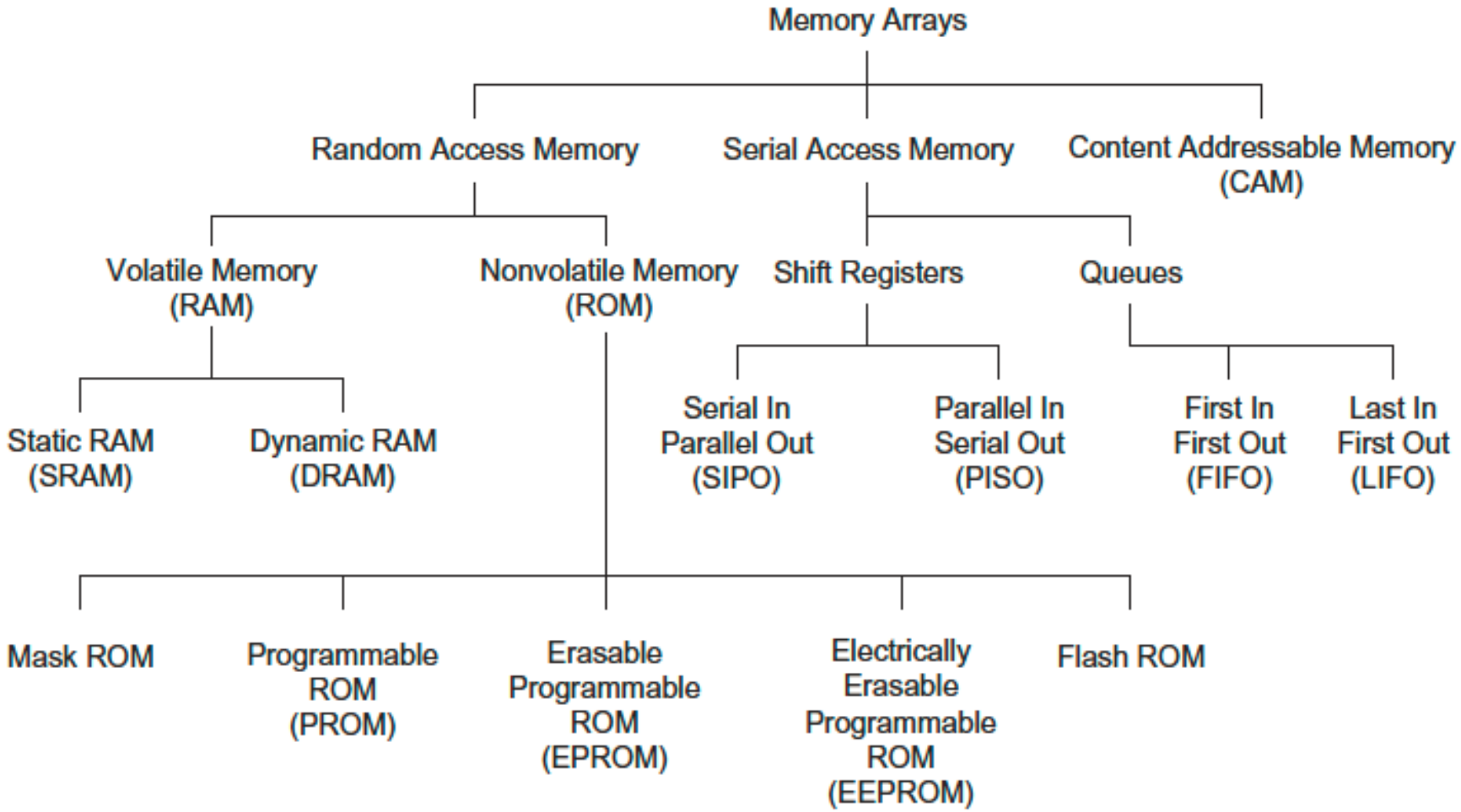
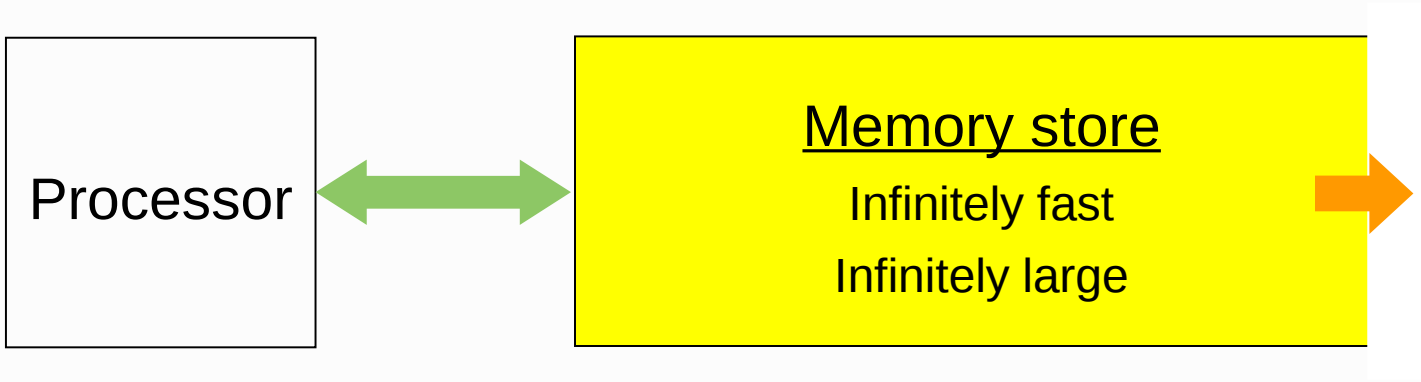
Memory Classification revisited



Motivation for a memory hierarchy – infinite memory



Cycles per Instruction (CPI) = Number of processor clock cycles required per instruction

CPI[∞ cache]

Finite memory speed

CPI = CPI[∞ cache] + FCP

Finite cache penalty

Locality of reference – spatial and temporal

Temporal

If you access something now you'll need it again soon

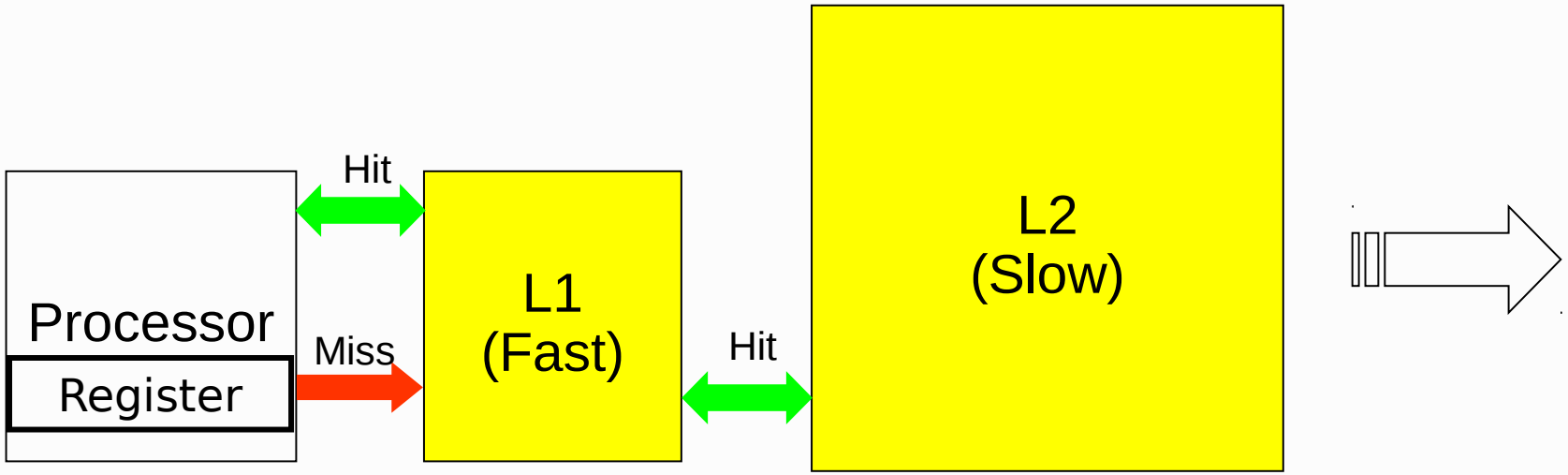
e.g: Loops

Spatial

If you accessed something you'll also need its neighbor

e.g: Arrays

Exploit this to divide memory into hierarchy

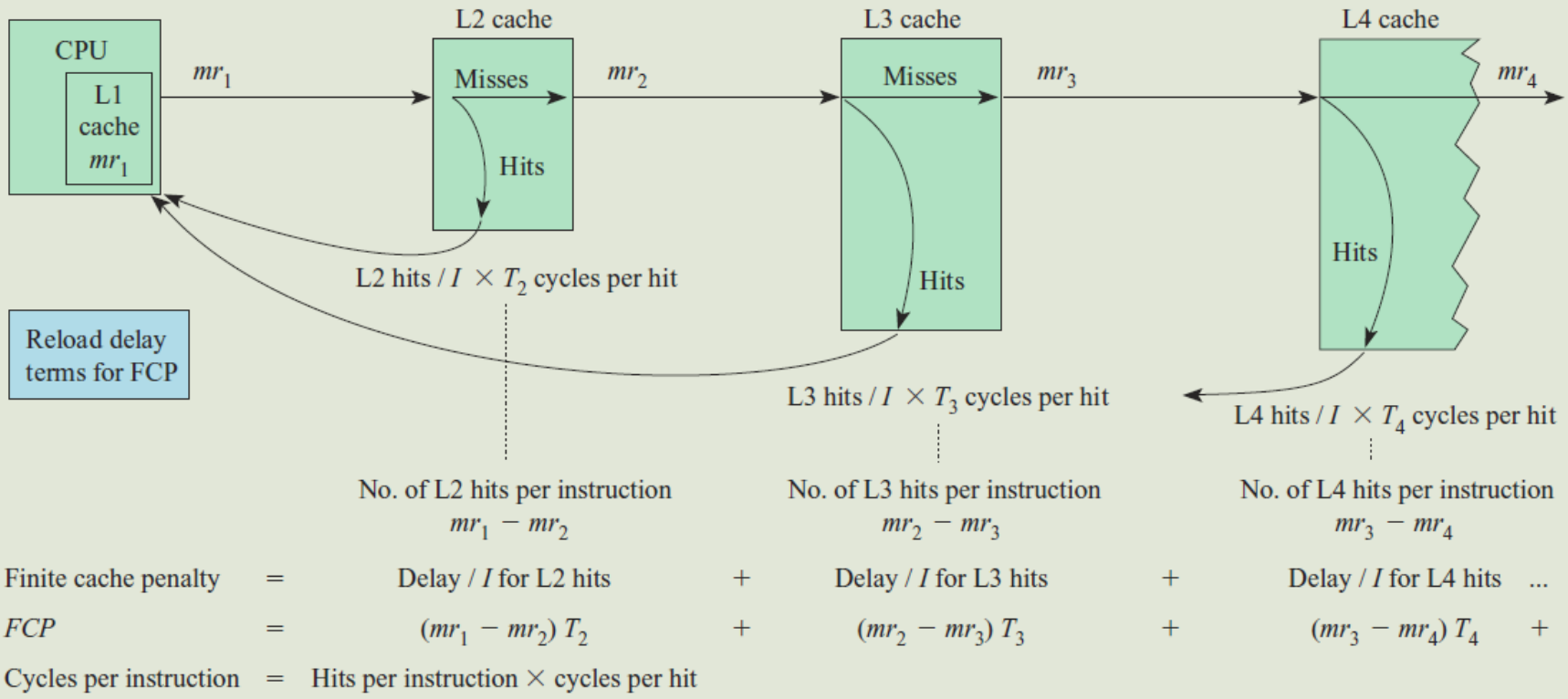


Cache size impacts cycles-per-instruction

Logic-based eDRAM: Origins and rationale for use

R. E. Matick
S. E Schuster

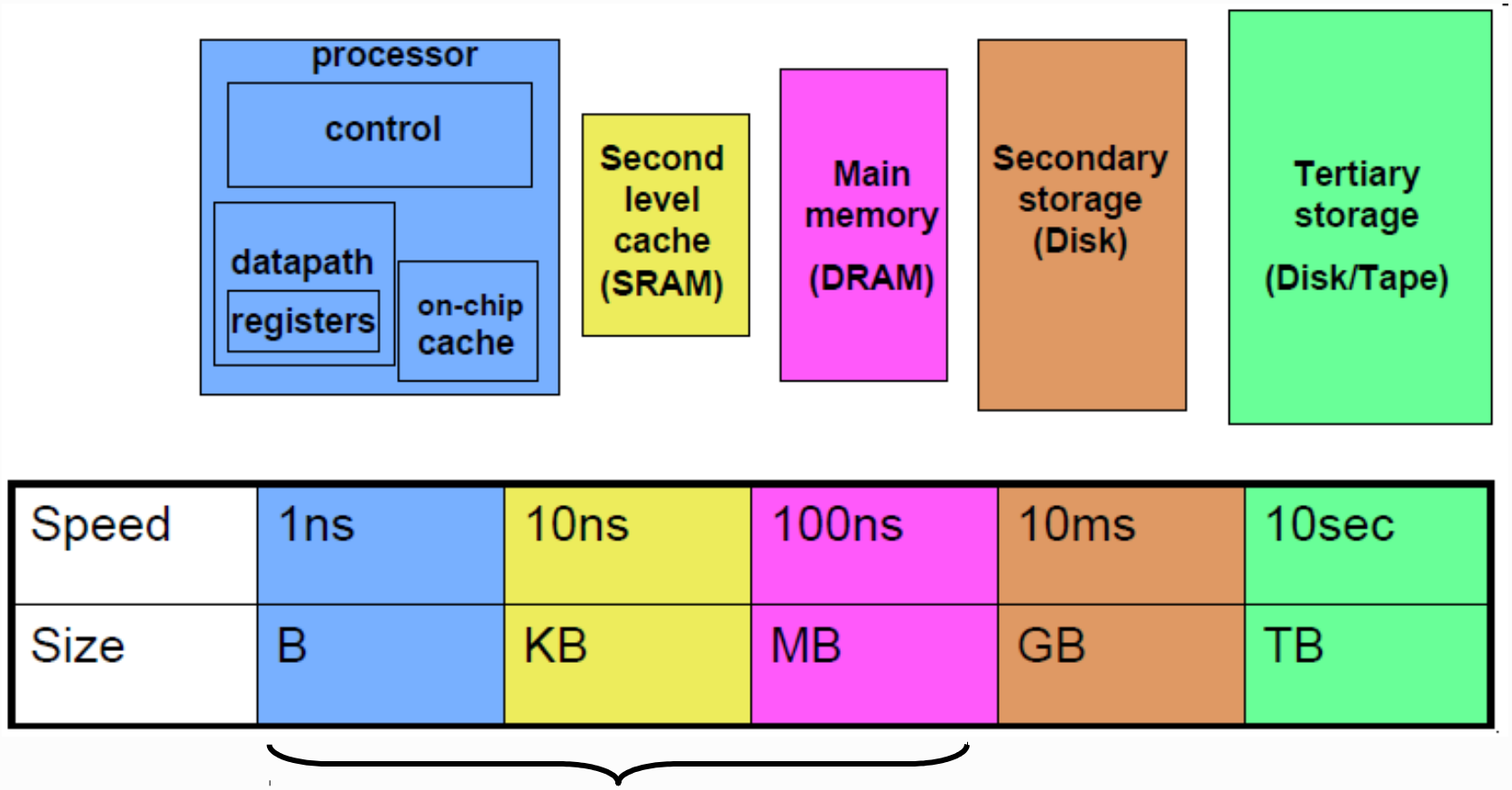
IBM J. RES. & DEV. VOL. 49 NO. 1 JANUARY 2005



Finite cache penalty	=	Delay / I for L2 hits	+	Delay / I for L3 hits	+	Delay / I for L4 hits ...
FCP	=	$(mr_1 - mr_2)\, T_2$	+	$(mr_2 - mr_3)\, T_3$	+	$(mr_3 - mr_4)\, T_4$ + ...
Cycles per instruction	=	Hits per instruction × cycles per hit				

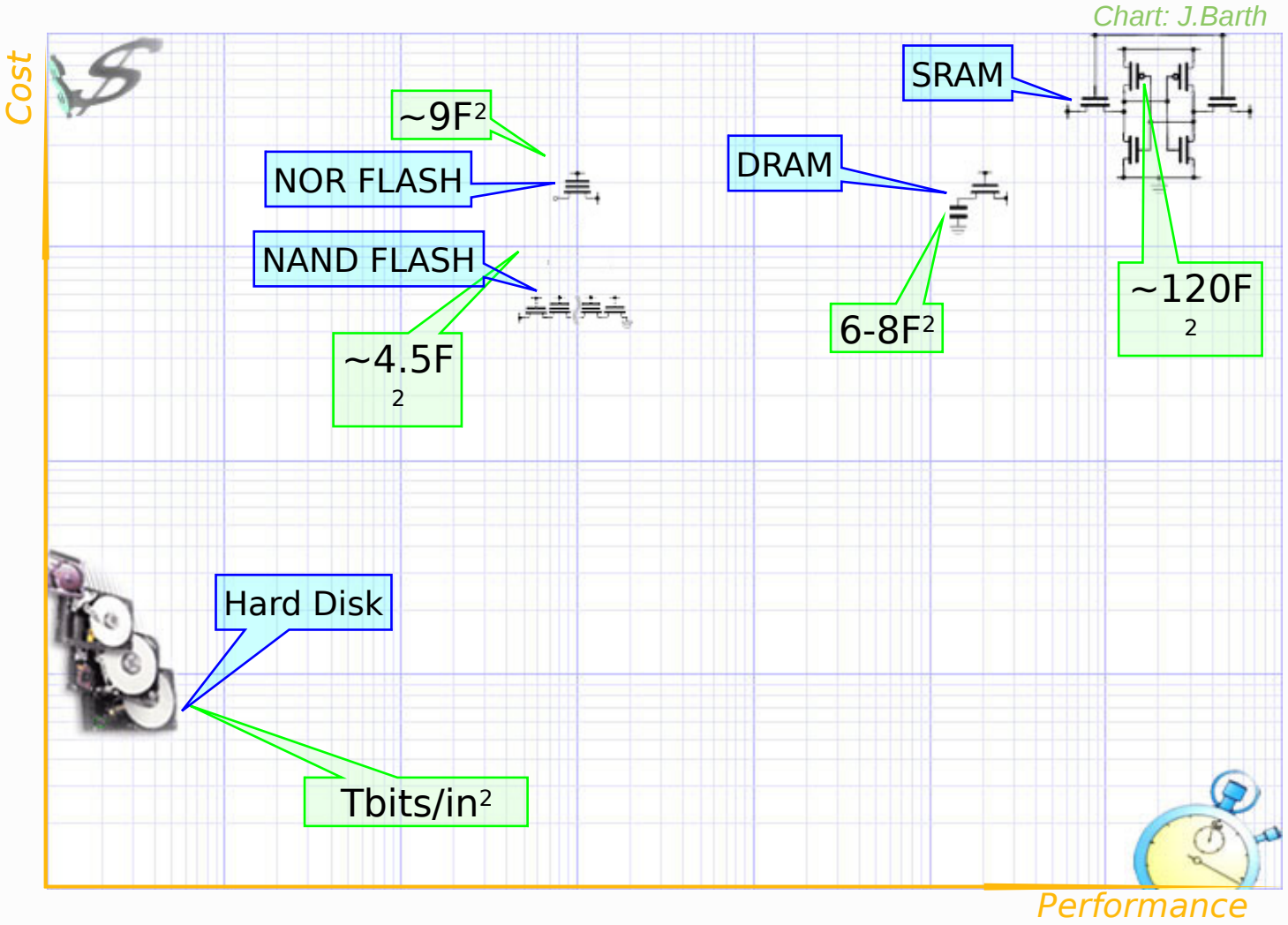
→ Access rate reduces: Slower memory is sufficient

Cache size impacts cycles-per-instruction



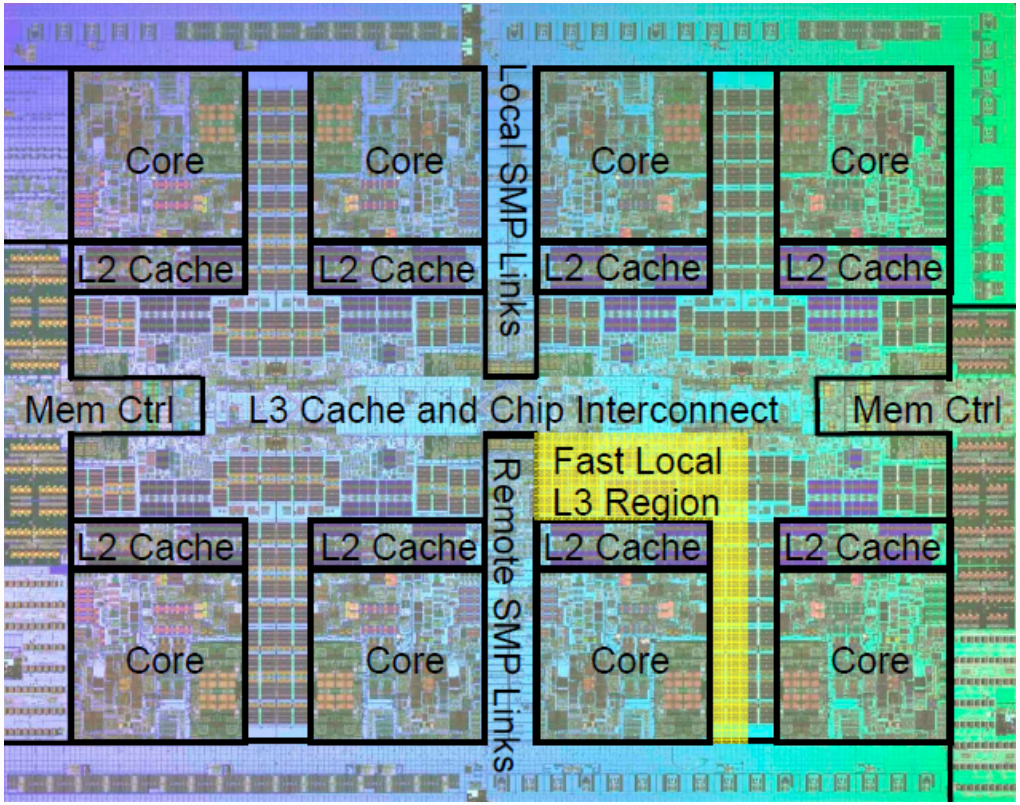
For a 5GHz processor, scale the numbers by 5x

Technology choices for memory hierarchy



eDRAM L3 cache

Power7 processor

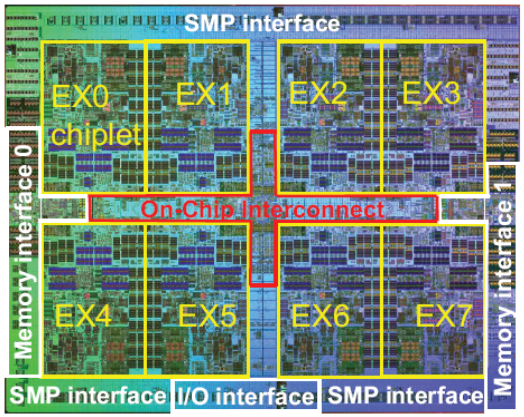


Move L2,L3 Cache inside of the data hungry processor

Higher hit rate Reduced FCP

Embedded DRAM Advantages

IBM Power7tm
32MB eDRAM L3

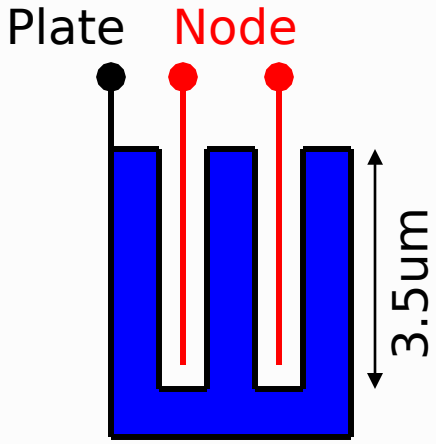


Memory Advantage

- 2x Cache can provide > 10% Performance
- ~3x Density Advantage over eSRAM
- 1/5x Standby Power Compared to SRAM
- Soft Error Rate 1000x lower than SRAM
- Performance ? DRAM can have lower latency !
- IO Power reduction

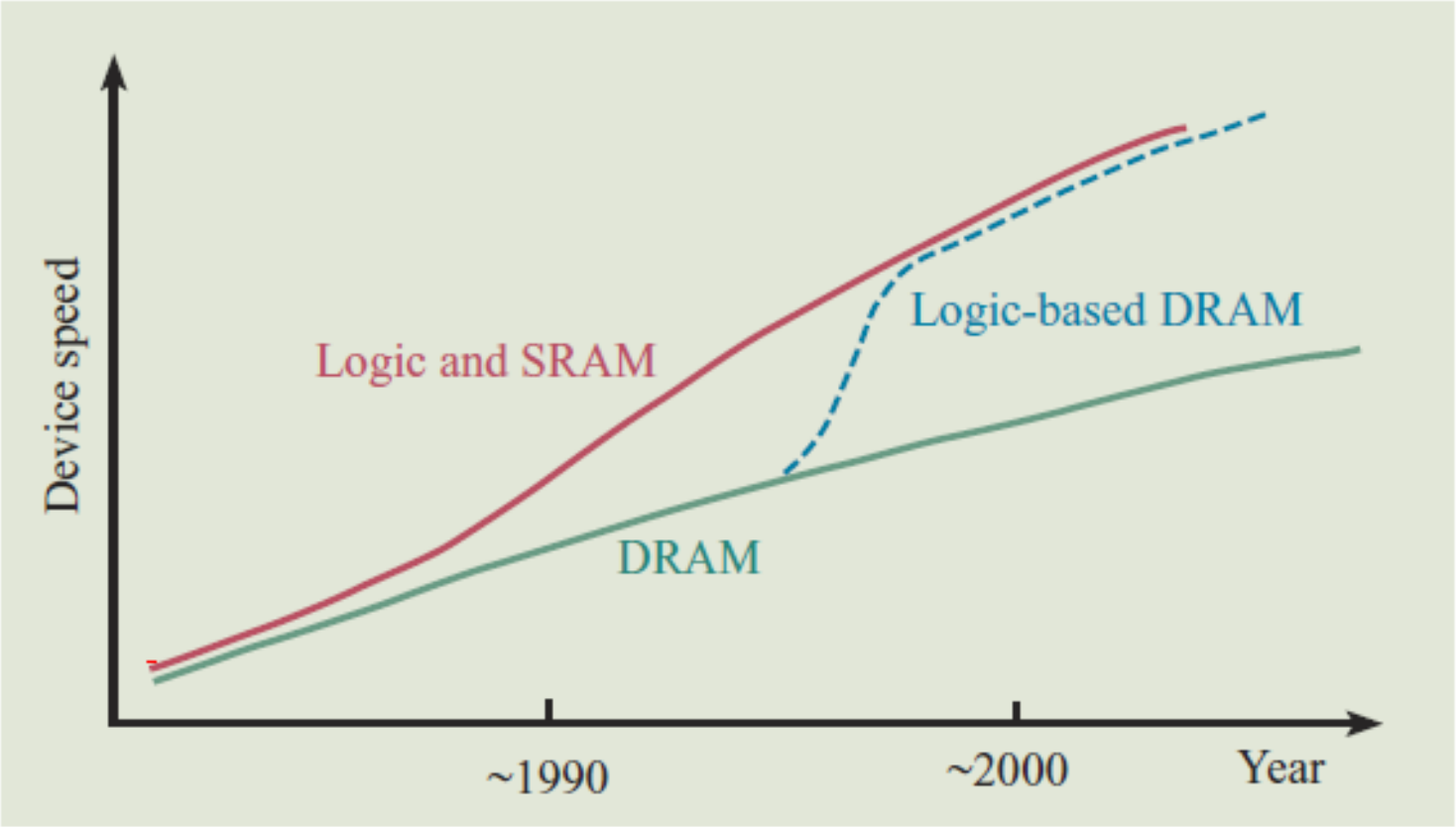
Deep Trench Capacitor

- Low Leakage Decoupling
- 25x more Cap / μm^2 compared to planar
- Noise Reduction = Performance Improvement
- Isolated Plate enables High Density Charge Pump

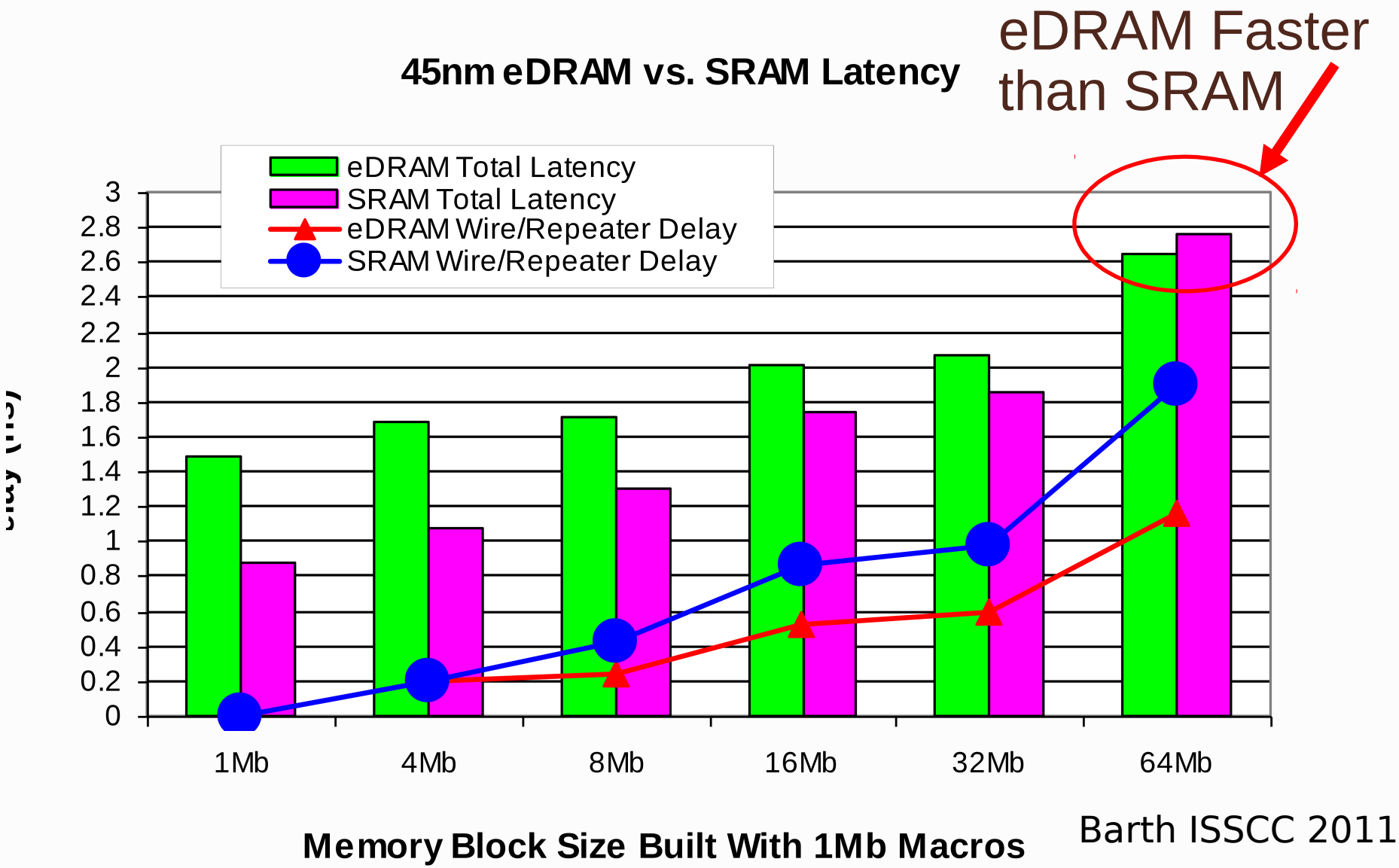


Cache performance – SRAM vs. DRAM

Chart: Matick & Schuster, op. cit.



Embedded DRAM Performance



Barth ISSCC 2011

Question 3

Comparing SRAM and eDRAM which of the following is true?

- eDRAM can be faster than SRAM for small size memories
- SRAM is more succeptable to SEUs
- SRAM process of manufacturing is more complicated
- Stand by power in SRAM is lower

Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example

Fundamental DRAM Operation

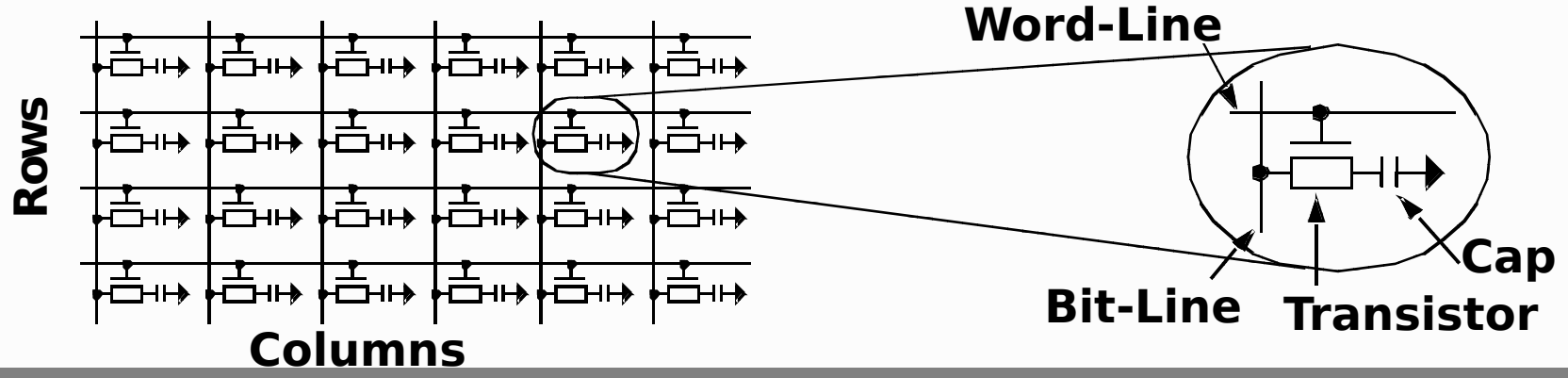
Memory Arrays are composed of Row and Columns

Most DRAMs use 1 Transistor as a switch and 1 Cap as a storage element (Dennard 1967)

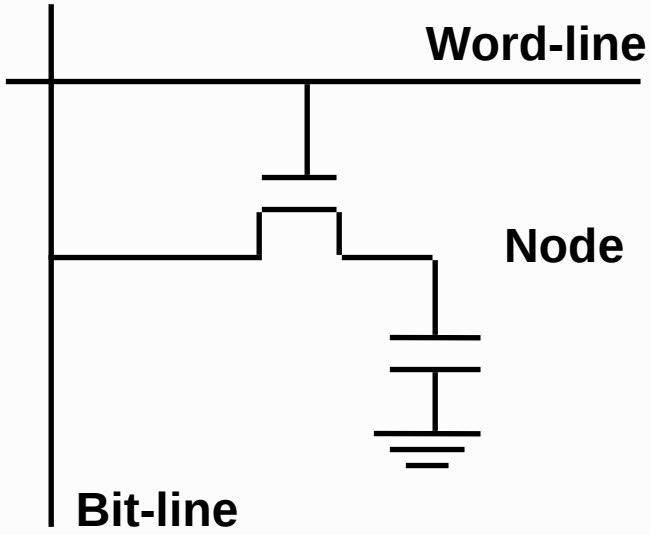
Single Cell Accessed by Decoding One Row / One Column (Matrix)

Row (Word-Line) connects storage Caps to Columns (Bit-Line)

Storage Cap Transfers Charge to Bit-Line, Altering Bit-Line Voltage



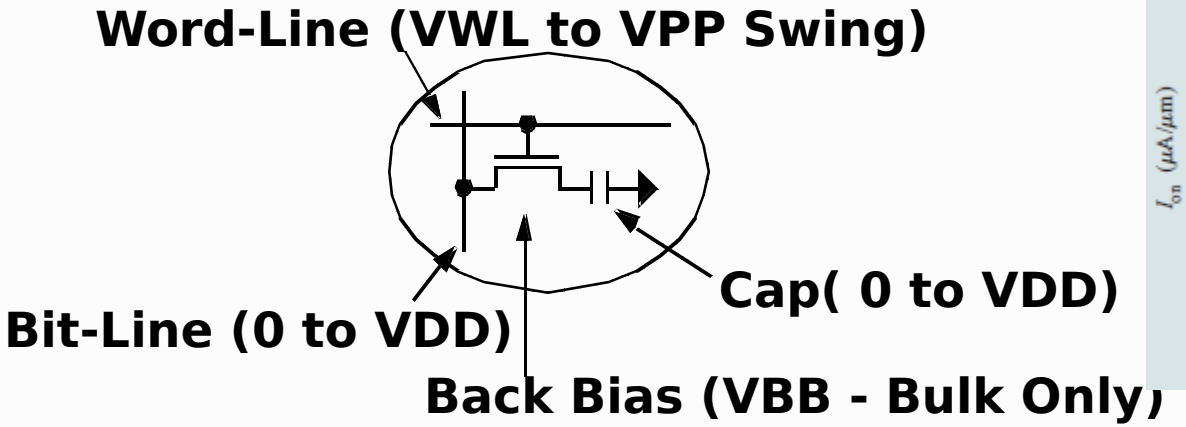
1T1C DRAM Cell Terminals

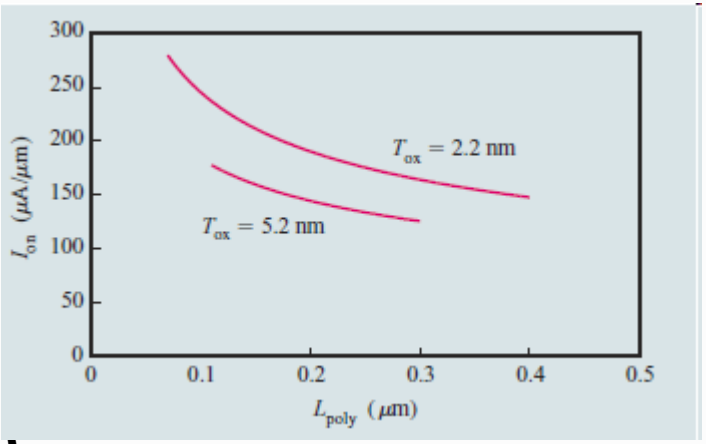


Voltage Levels?

IBM J RES & DEV 2005

1T1C DRAM Cell Terminals





VWL: GND or Negative for improved leakage

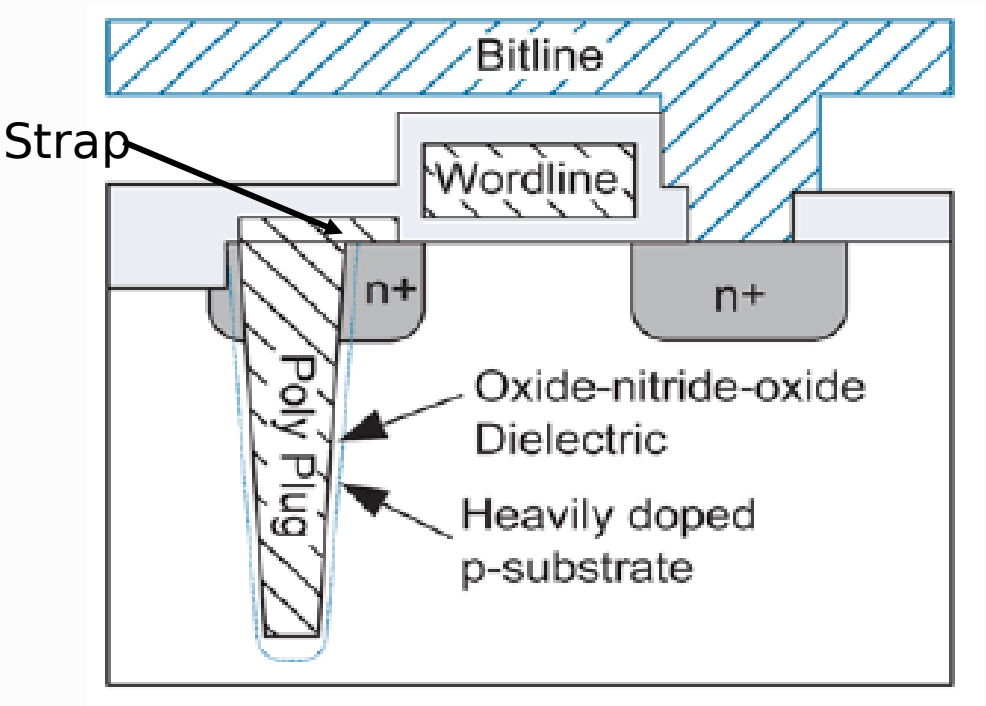
VPP: 1.5V up to 3.5V depending on Technology

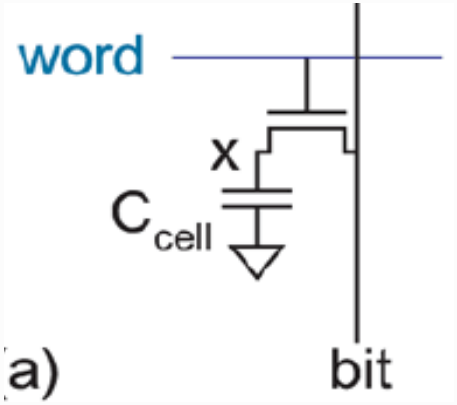
VBB: Typically Negative to improve Leakage
Not practical on SOI

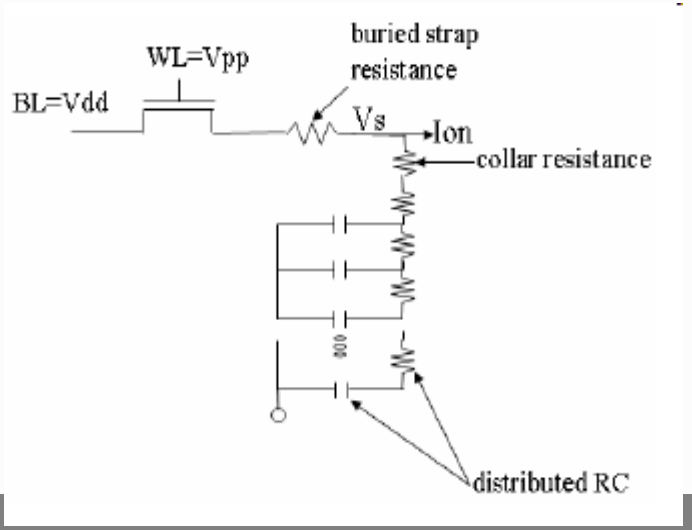
IBM J RES & DEV 2005

DRAM cell Cross section

- Store their contents as charge on a capacitor rather than in a feedback loop.
- 1T dynamic RAM cell has a transistor and a capacitor

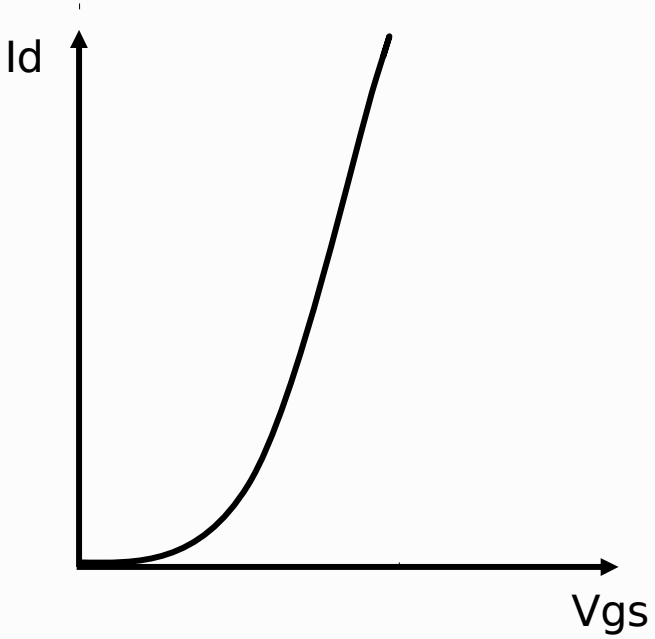


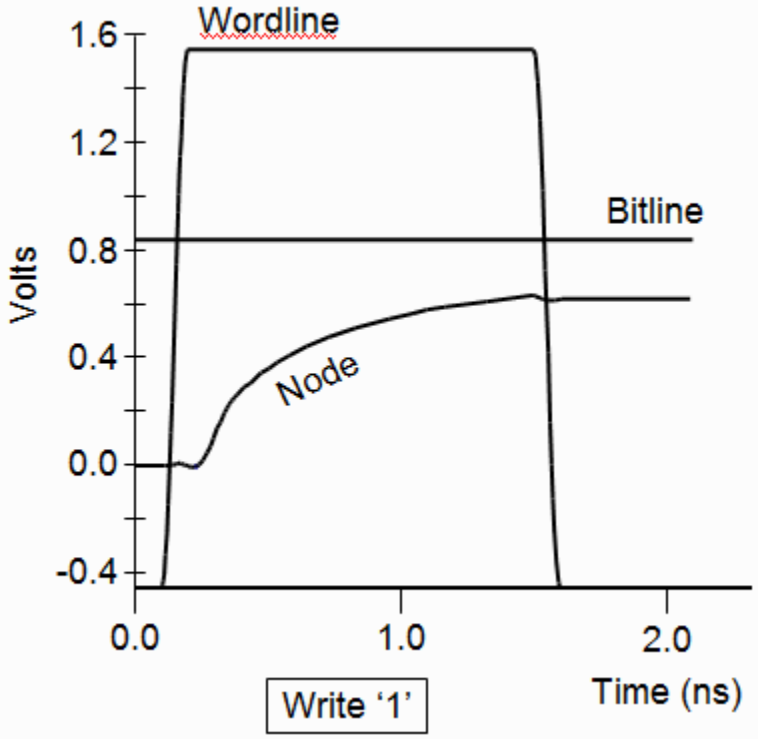




CMOS VLSI design - PEARSON

Storing data ‘1’ in the cell

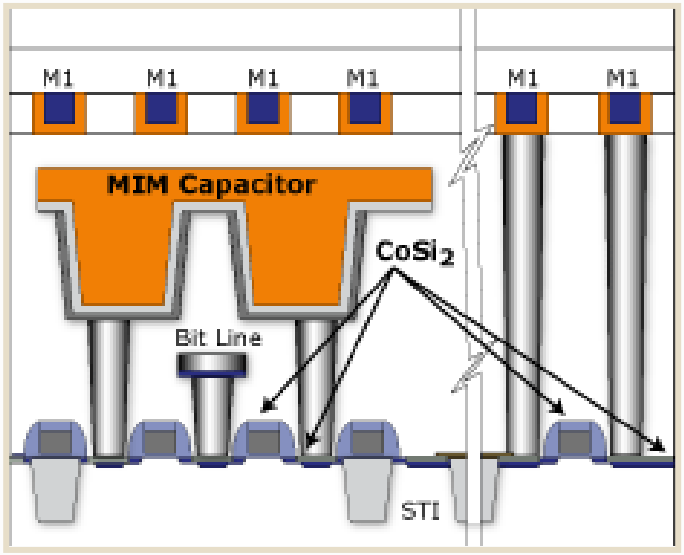




Vgs for pass transistor reduces as bitcell voltage rises, increasing Ron

Why there is a reduction in cell voltage after WL closes? Experiment

MIM Cap v/s Trench



MIM eDRAM Process

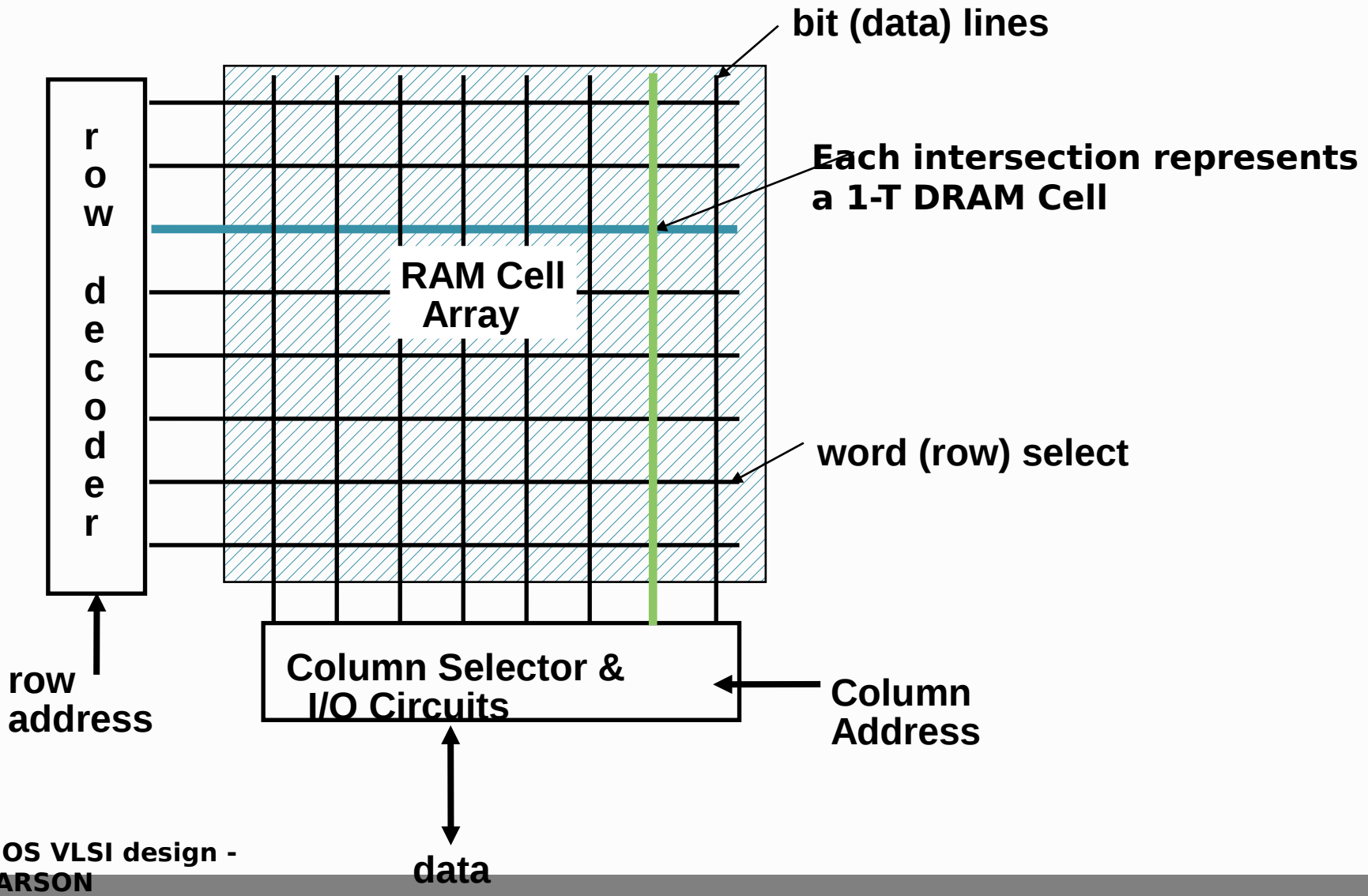
Back End

Front End

Trench eDRAM Process

- Stack capacitor requires more complex process
- M1 height above gate is increased with stacked capacitor
  - M1 parasitics significantly change when wafer is processed w/o eD
  - Drives unique timings for circuit blocks processed w/ and w/o eDR
    - Logic Equivalency is compromised – **Trench is Better Choice**

Classical DRAM Organization



DRAM Subarray

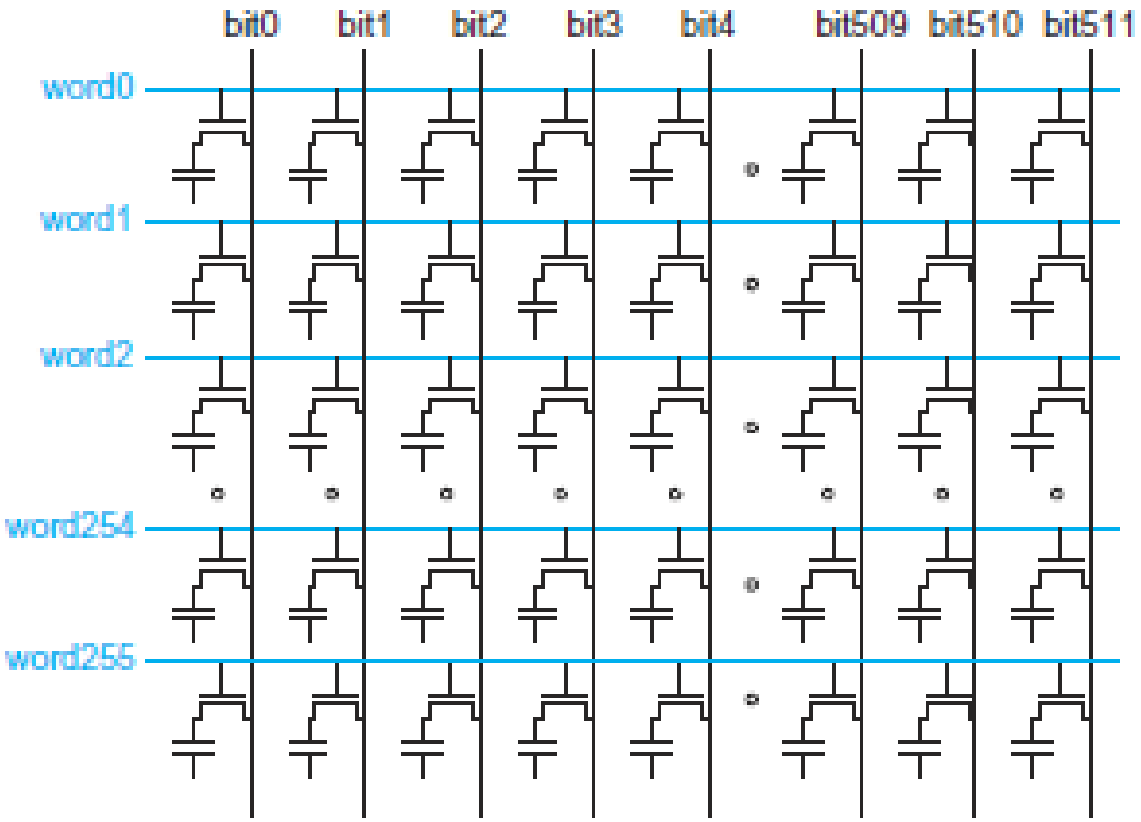
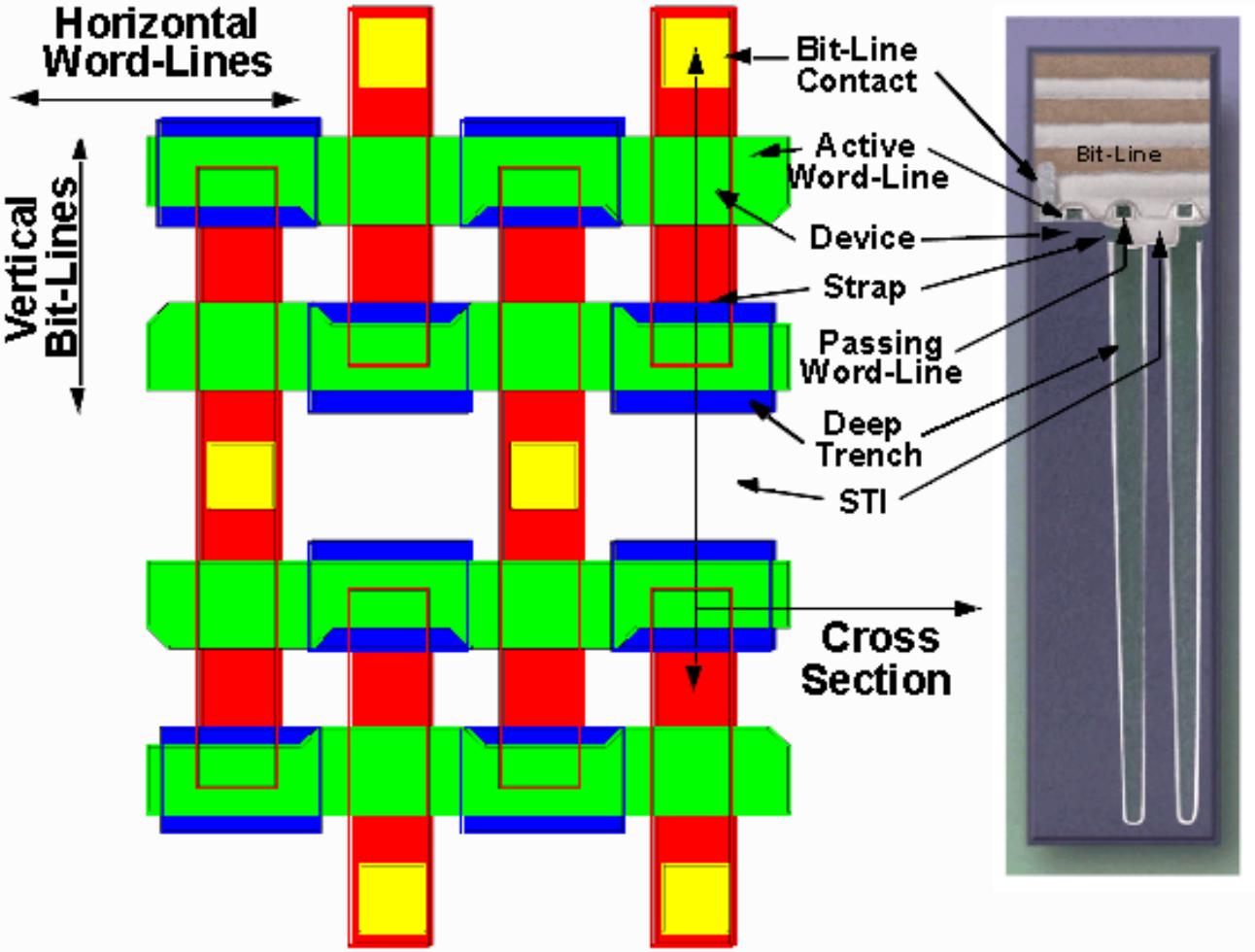
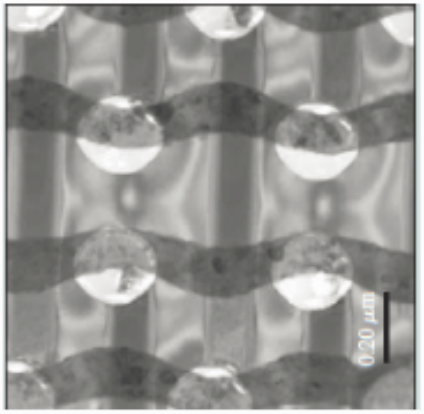


FIGURE 12.43 DRAM subarray

CMOS VLSI design - PEARSON

Trench cell layout and cross-section





Silicon Image

Question 4

In a certain eDRAM process VDD=800mV and the pass transistor has a nominal VTH of 200mV with the worst case VTH variation 50mV. VPP should be

- At least 800mV
- At least 1050 mV
- At most 550 mV
- At most 1050 mV

References so far

Barth, J. et al., “A 300MHz Multi-Banked eDRAM Macro Featuring GND Sense, Bit-line Twisting and Direct Reference Cell Write,” ISSCC Dig. Tech. Papers, pp. 156-157, Feb. 2002.

Barth, J. et. al., “A 500MHz Multi-Banked Compilable DRAM Macro with Direct Write and Programmable Pipeline,” ISSCC Dig. Tech. Papers, pp. 204-205, Feb. 2004.

Barth, J. et al., “A 500MHz Random Cycle 1.5ns-Latency, SOI Embedded DRAM Macro Featuring a 3T Micro Sense Amplifier,” ISSCC Dig. Tech. Papers, pp. 486-487, Feb. 2007.

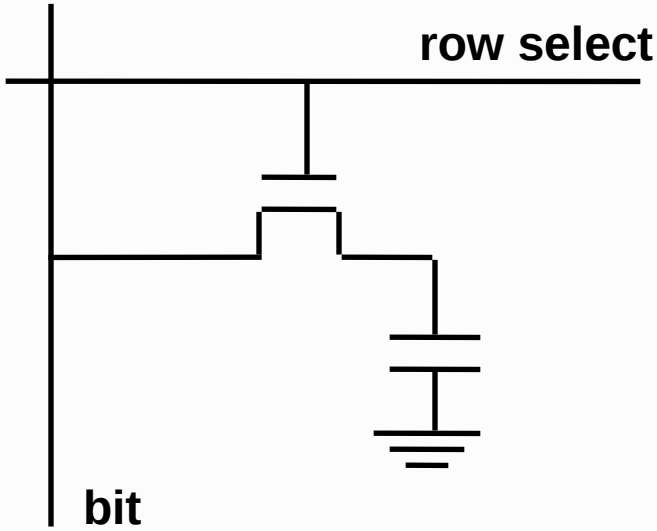
Barth, J. et al., “A 45nm SOI Embedded DRAM Macro for POWER7TM 32MB On-Chip L3 Cache,” ISSCC Dig. Tech. Papers, pp. 342-3, Feb. 2010.

Butt,N., et al., “A 0.039um2 High Performance eDRAM Cell based on 32nm High-K/Metal SOI Technology,” IEDM pp. 27.5.1-2, Dec 2010.

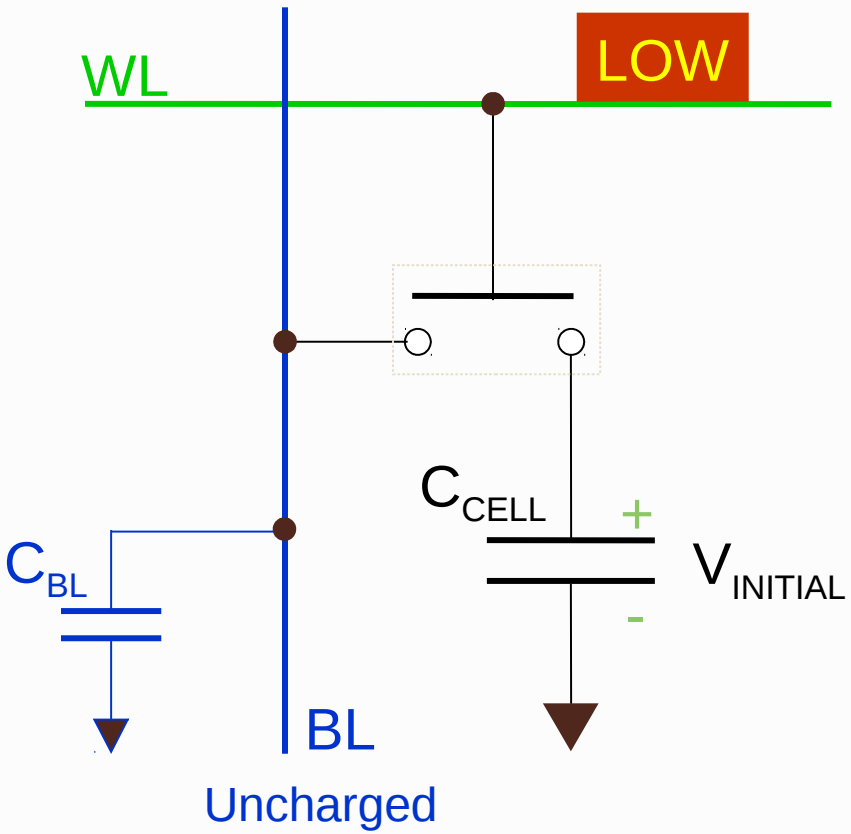
Bright, A. et al., “Creating the BlueGene/L Supercomputer from Low-Power SoC ASICs,” ISSCC Dig. Tech. Papers, pp. 188-189, Feb. 2005.

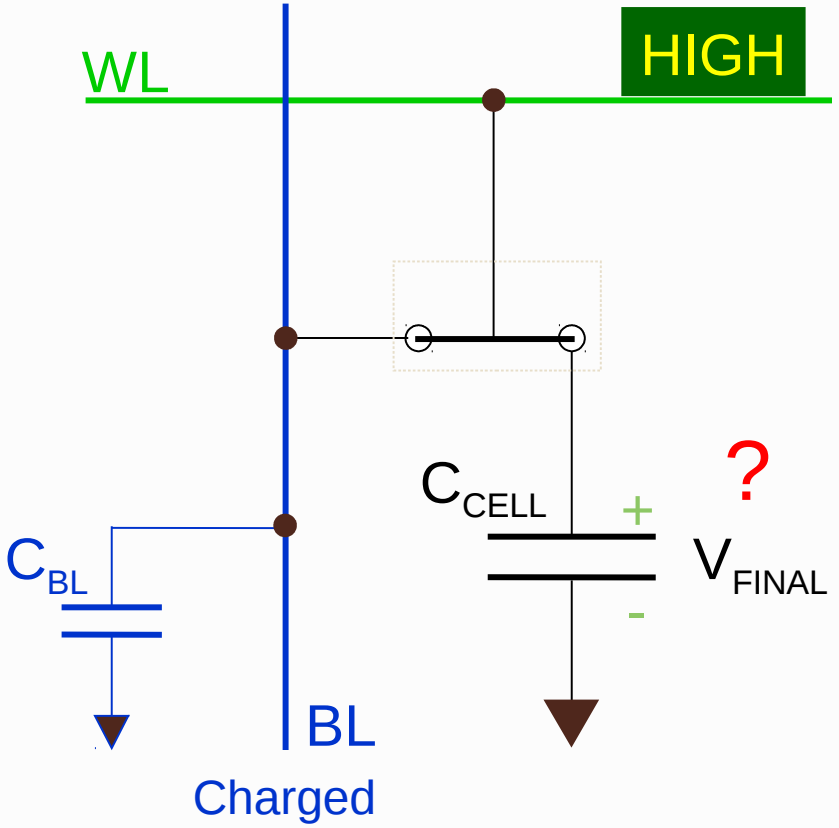
DRAM Read, Write and Refresh

- Write:
  - 1. Drive bit line
  - 2. Select row
- Read:
  - 1. Precharge bit line
  - 2. Select row
  - 3. Cell and bit line share charges
    - Signal developed on bitline
  - 4. Sense the data
  - 5. Write back: restore the value
- Refresh
  - 1. Just do a dummy read to every cell & auto write-back

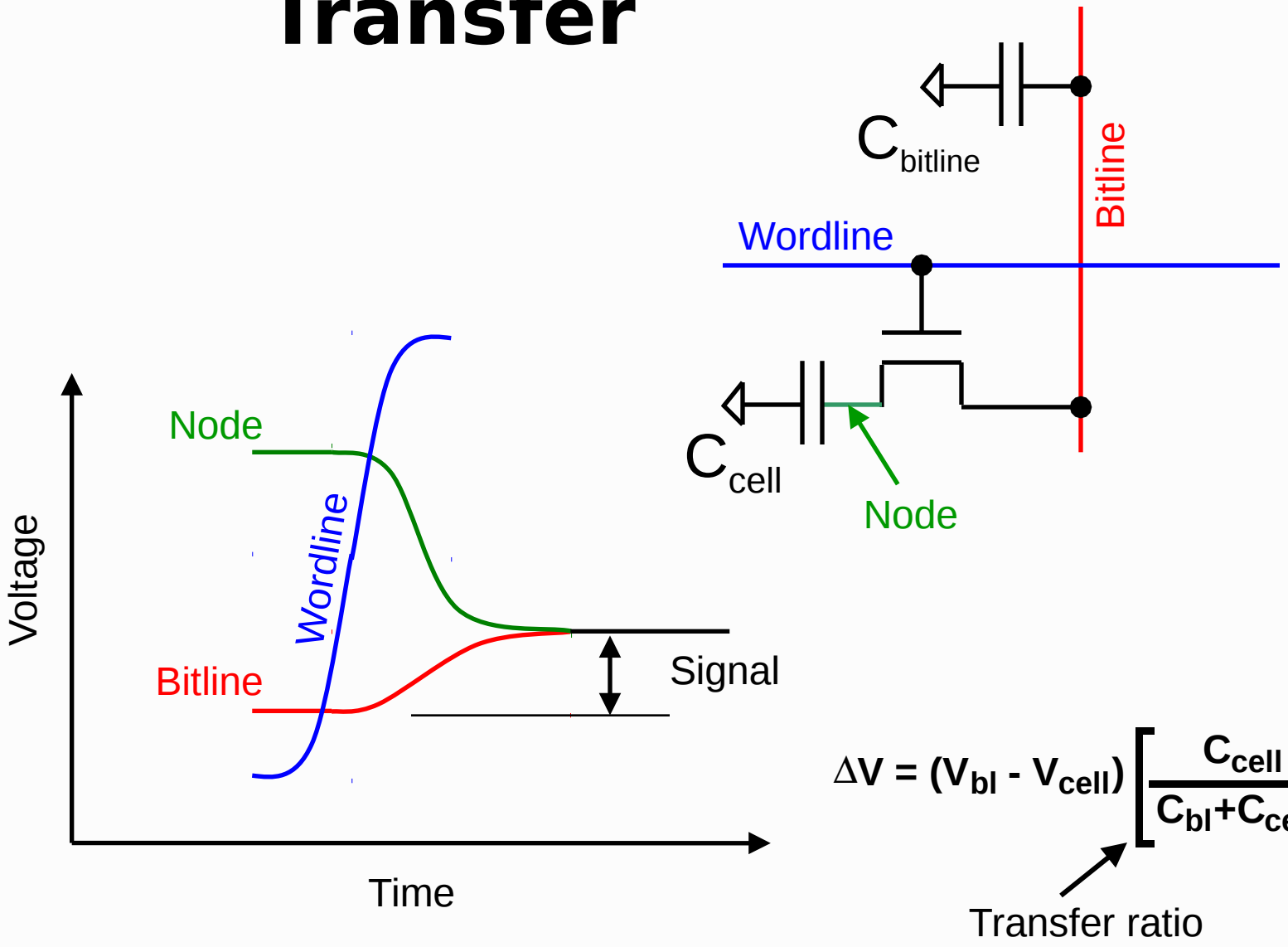


Cell transfer ratio





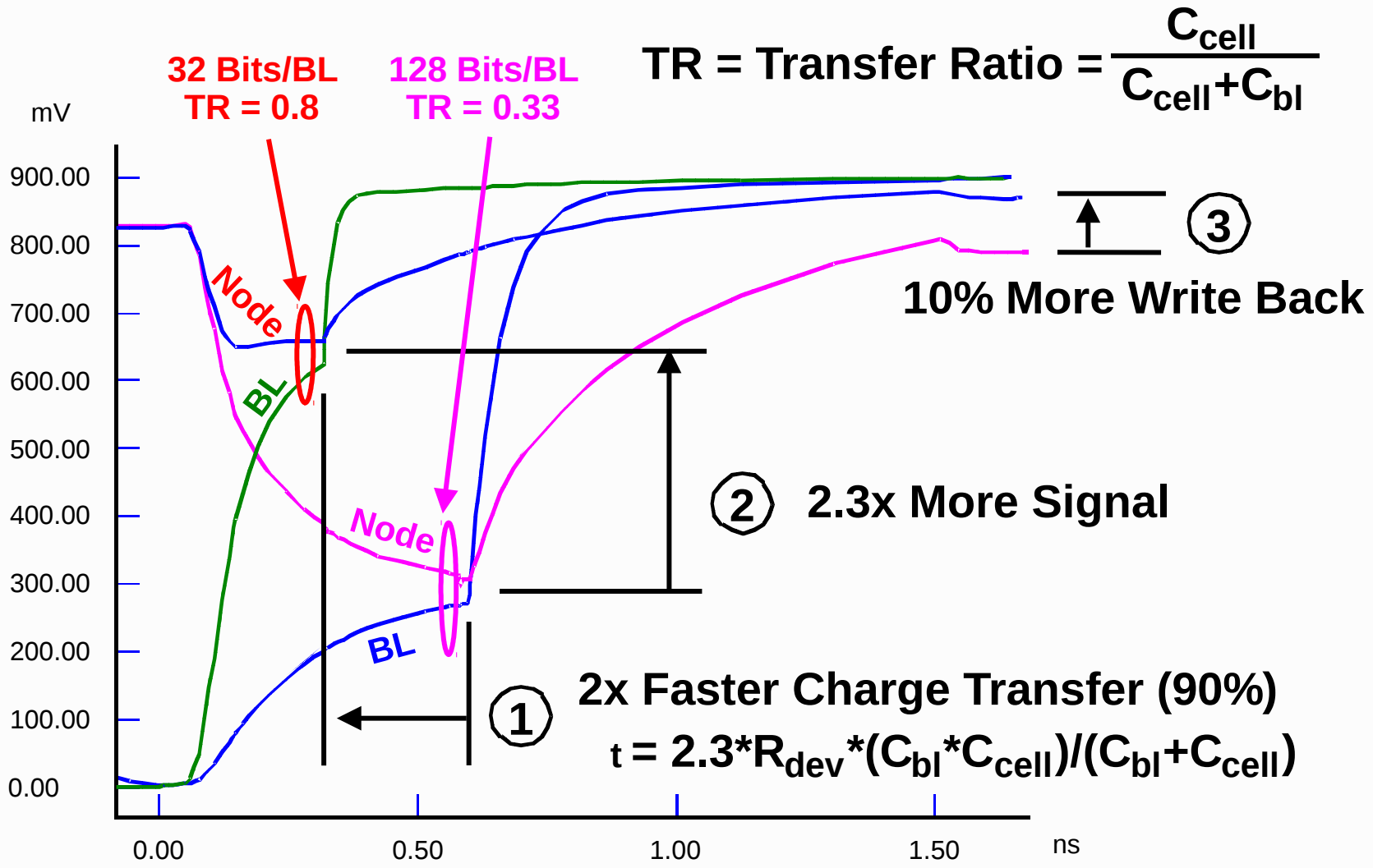
Cell Charge Transfer



$$\Delta V = (V_{bl} - V_{cell}) \left[\frac{C_{cell}}{C_{bl}+C_{cell}} \right]$$

Transfer ratio

Bits per Bit-Line v/s Transfer Ratio



Segmentation

Array Segmentation Refers to WL / BL Count per Sub-Array

Longer Word-Line (More Bit-Lines per Word-Line)

Slower but more area efficient – Less Decoders and drivers

Longer Bit-Line (more Word-Lines per Bit-Line)

Less Signal (Higher Bit-Line Capacitance = Lower Transfer Ratio)

More Power (Bit-Line CV is Significant Component of DRAM Power)

Slower Performance (Higher Bit-Line Capacitance = Slower Sense Amp)

More Area Efficient (Fewer Sense Amps)

Number of WLs Activated determines Refresh Interval and Power

All Cells on Active Word-Line are Refreshed

All Word-Lines must be Refreshed before Cell Retention Expires

64ms Cell Retention / 8K Word Lines = 7.8us between refresh cycles

Activating 2 Word-Lines at a time = 15.6us, 2x Bit-Line CV Power

Choice of SA

Depending on signal developed SA architecture is chosen

Direct sensing

- Requires large signal development
- An inverter can be used for sensing
- Micro sense amp (uSA) is another option

Differential sense amp

- Can sense low signal developed

This is choice between area, speed/performance

Question 5

The diffusion capacitance of the pass transistor is 100aF. If metal capacitance is negligible, in order to achieve a transfer ratio of at least 0.7 with 33 cells connected to a BL, the cell capacitance should be

- ○ At least 7.7fF
- ○ At least 7.7 pF
- ○ At most 7.7 fF
- ○ At most 7.7 pF

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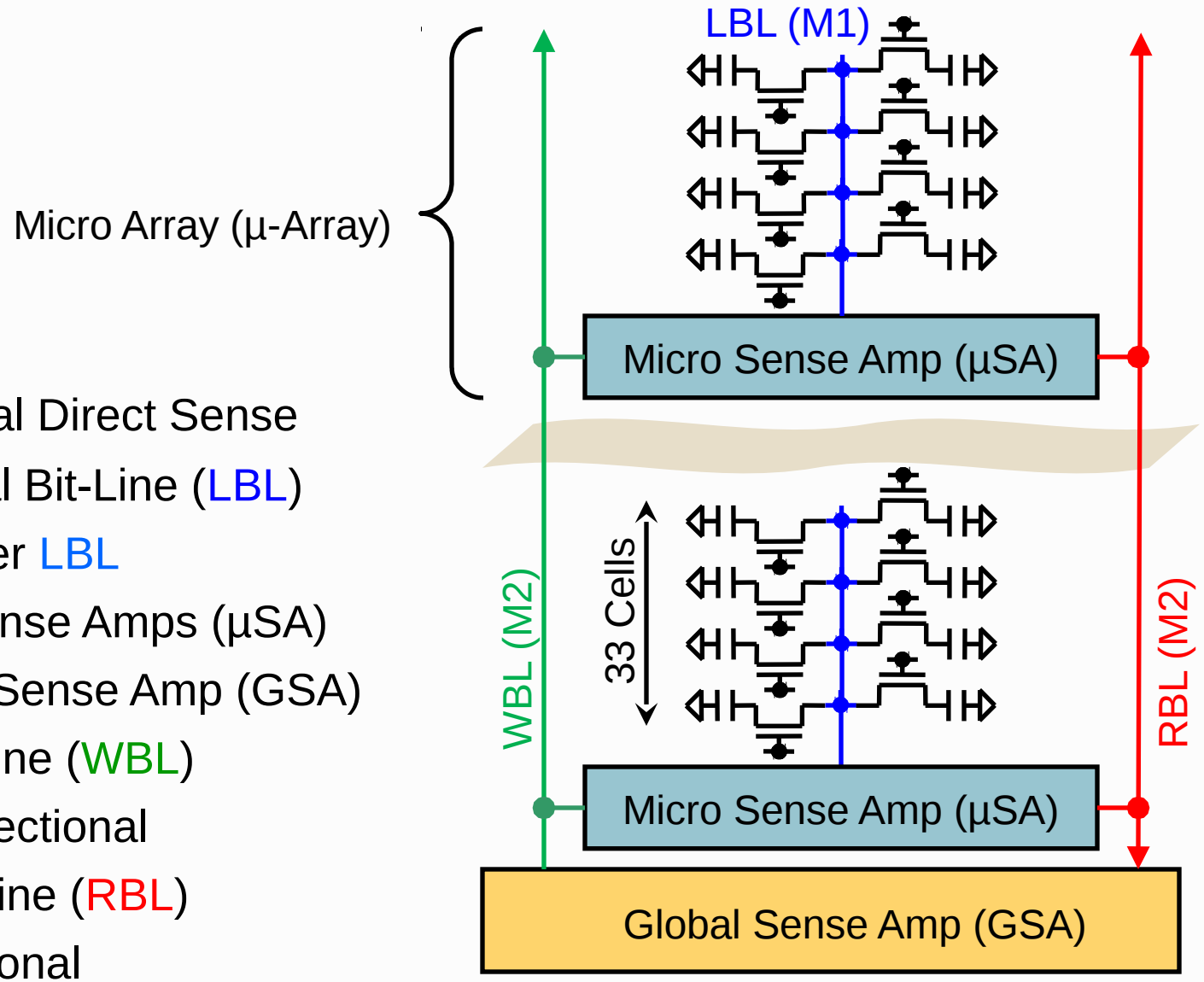
DRAM Operation Details (Case Study)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

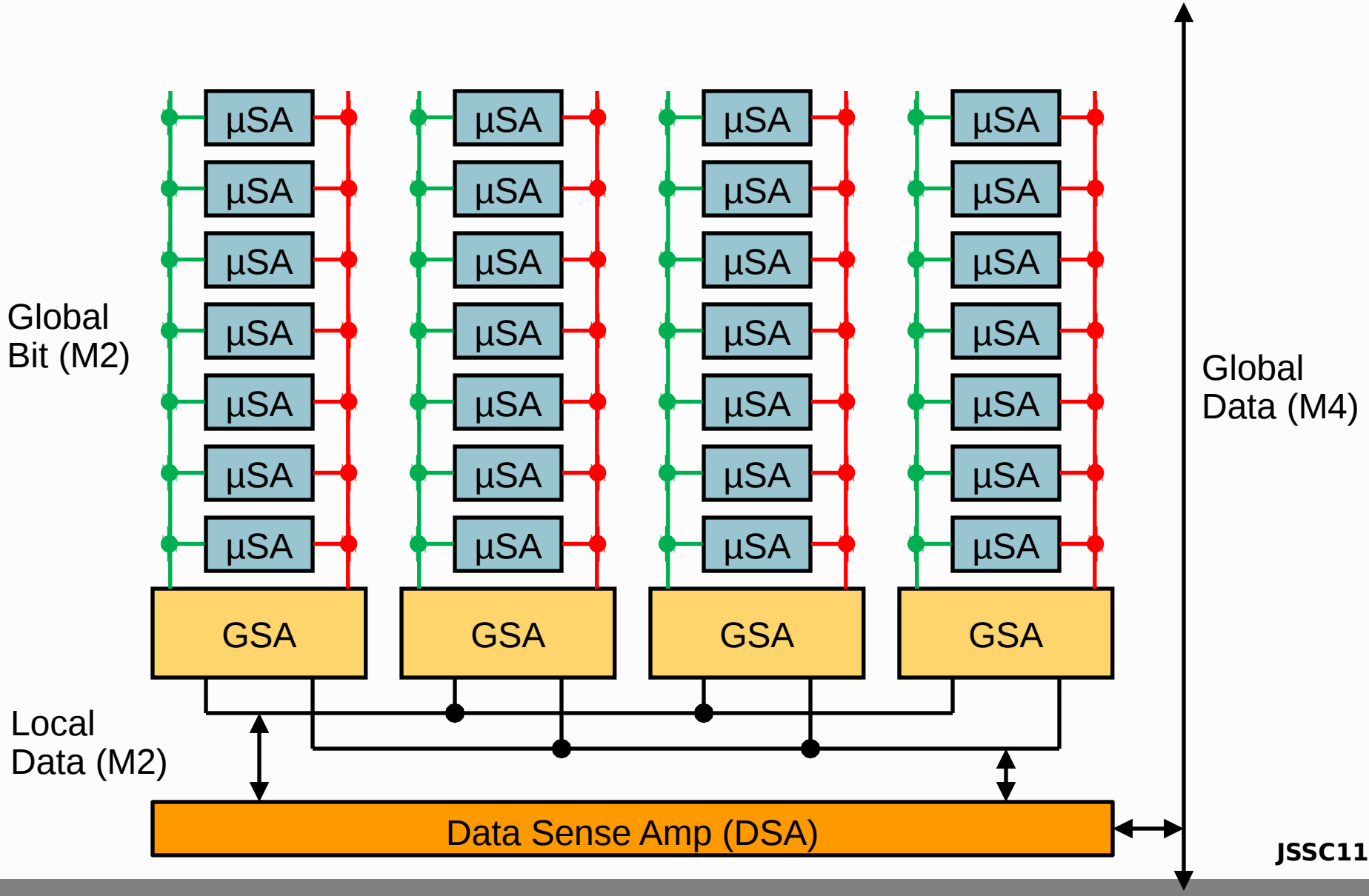
A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier (John Barth/IBM)

Micro Sense Architecture

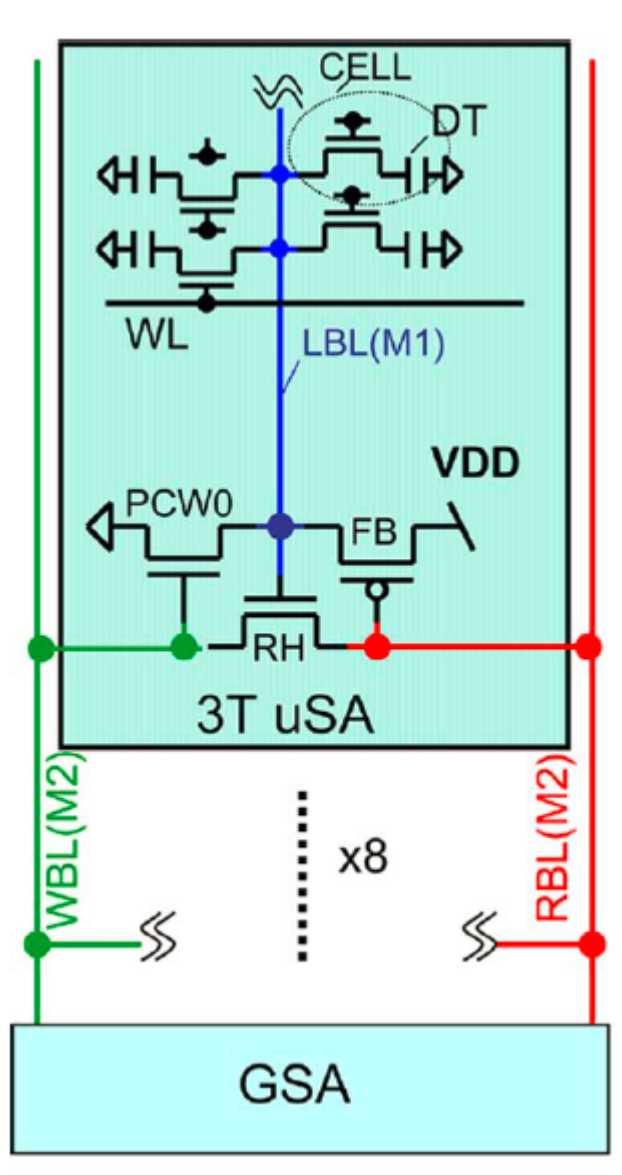


- Hierarchical Direct Sense
- Short Local Bit-Line (LBL)
  - 33 Cells per LBL
- 8 Micro Sense Amps (μSA) per Global Sense Amp (GSA)
- Write Bit-Line (WBL)
  Uni-Directional
- Read Bit-Line (RBL)
  Bi-Directional

levels


Global
Bit (M2)
µSA
GSA
Local
Data (M2)
Data Sense Amp (DSA)
Global
Data (M4)
JSSC11

3T uSA operation



Pre-charge

WL is low. WBL and RBL both pre-charged to HIGH.
Next GSA drives WBL low. **LBL floats to GND level**

Read “0”

LBL remains LOW. RBL is HIGH. Sensed as a “0”

Read “1”

LBL is HIGH. Turns on RH, pulls RBL LOW.
+ feedback as pFET FB turns ON. Sensed as a “1”

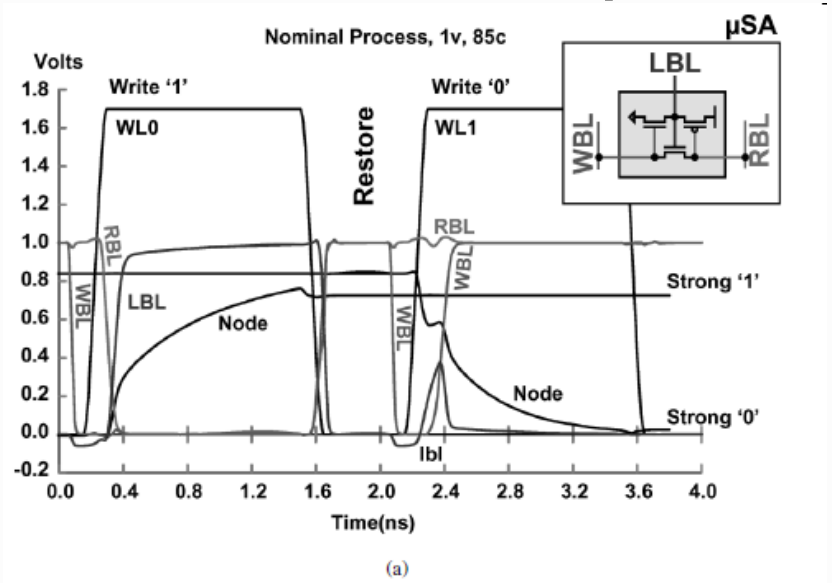
Write “1”

GSA pulls RBL to GND. FB pFET turns ON
Happens while WL rises (direct write)

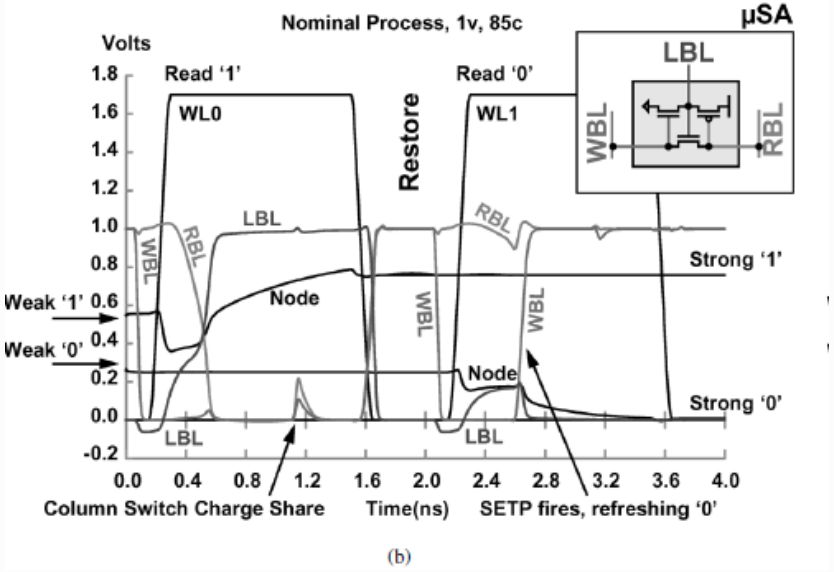
Write “0”

WBL is HIGH, PCW0 ON. Clamps LBL to GND
As WL activates.

Micro Sense Amp Simulations



(a)



(b)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

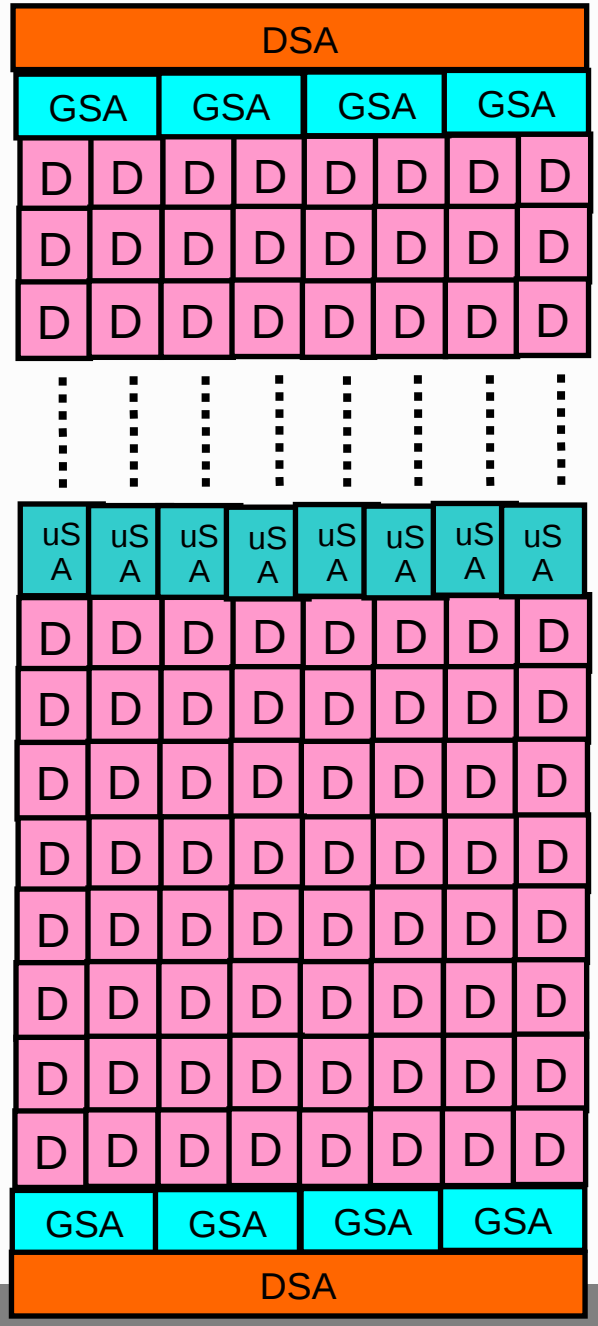
A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier

JSSC08

Layout Floor plan of Array+SA

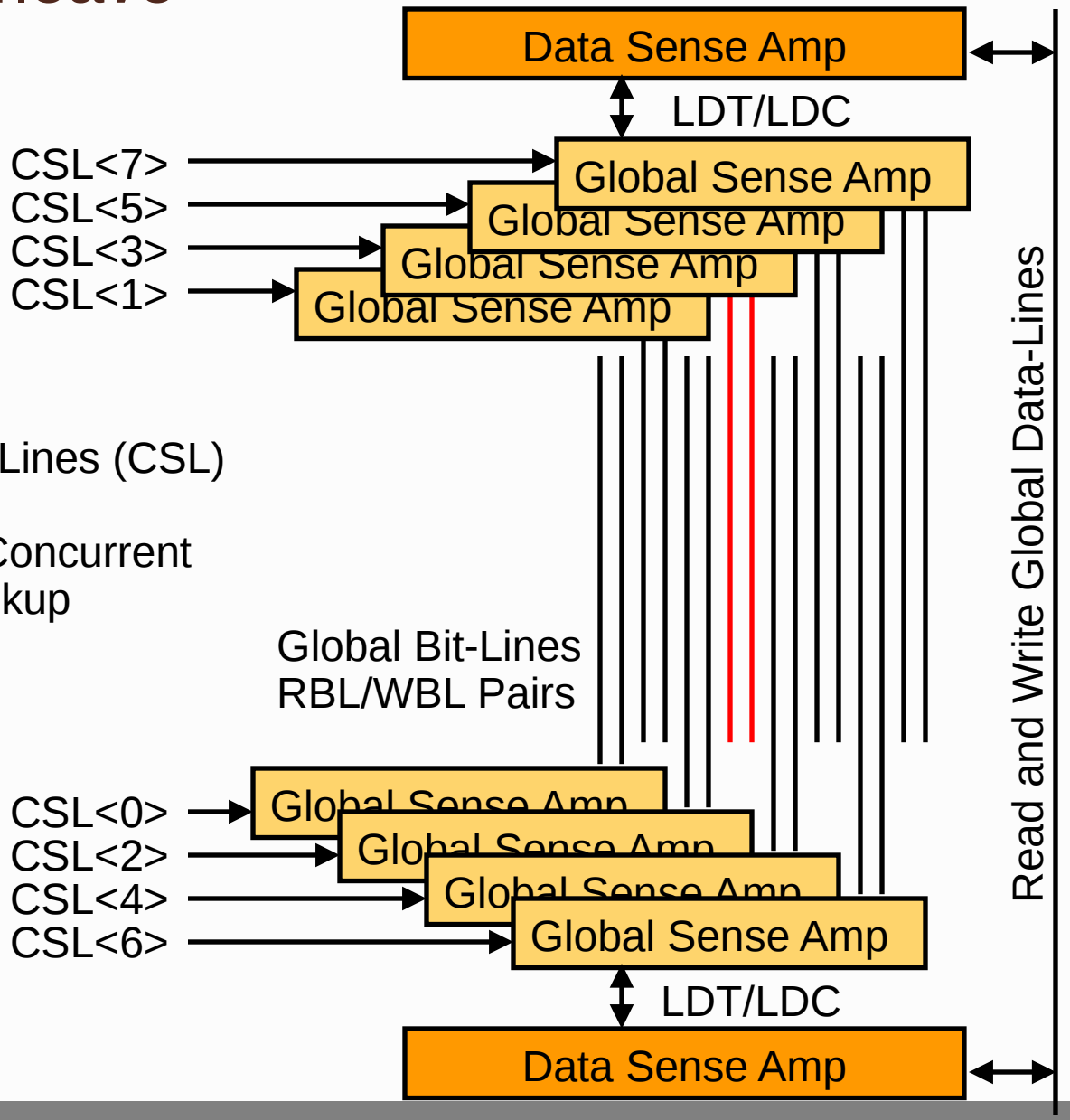
GSA Should fit into the bitcell width or n*bitcell width

Thus, distributed GSA on two sides of bitcell array



Column Interleave

- 1 of 8 Column Select Lines (CSL)
- Fire Early for Write
- Fire Late to Support Concurrent Cache Directory Lookup



Question 6

Q6. In a 3T micro sense amp, sensing a one is controlled is directly controlled by the trip point of

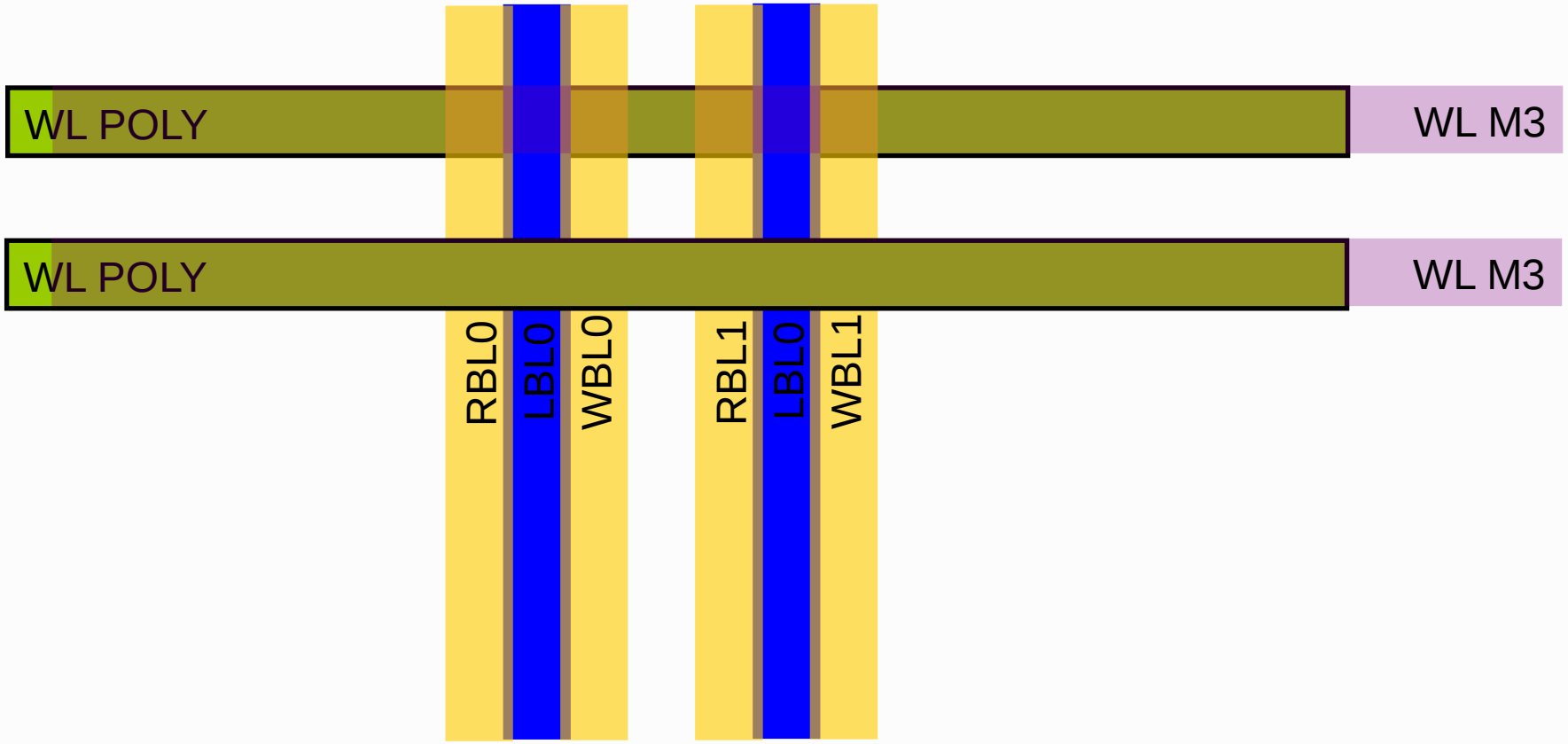
- NFET RH
- Pre-charge NFET (PC)
- Pull up PFET (FB)
- Pass transistor of the cell being read

Question 1 (Feb 2 2017)

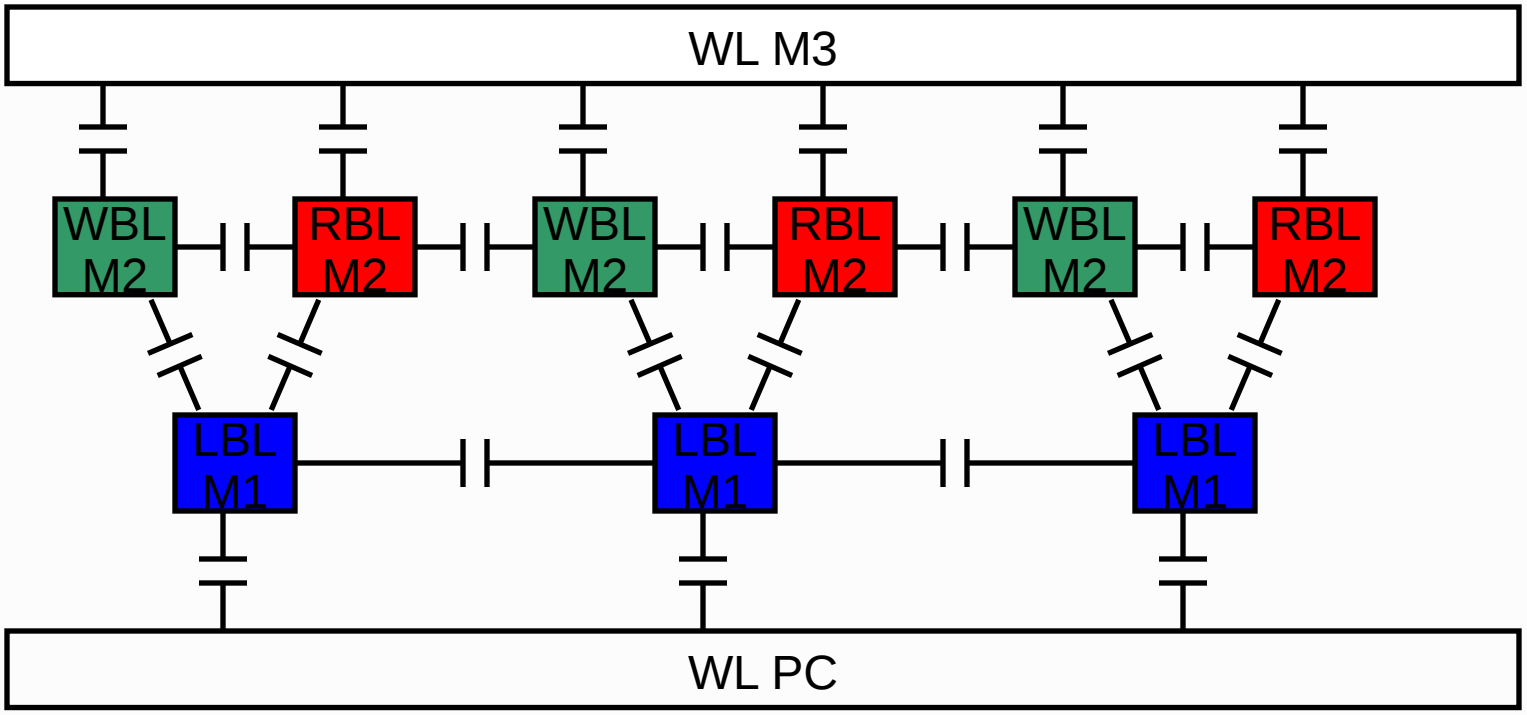
Q7. The problem with the 3T micro sense family is that

- It is slow to sense a ZERO
- It cannot accommodate more than 33 cells per LBL
- it consumes too much dynamic and leakage power
- It is too slow to sense a ONE

LAYOUT of array



Micro Sense Local Bit-line Cross Section



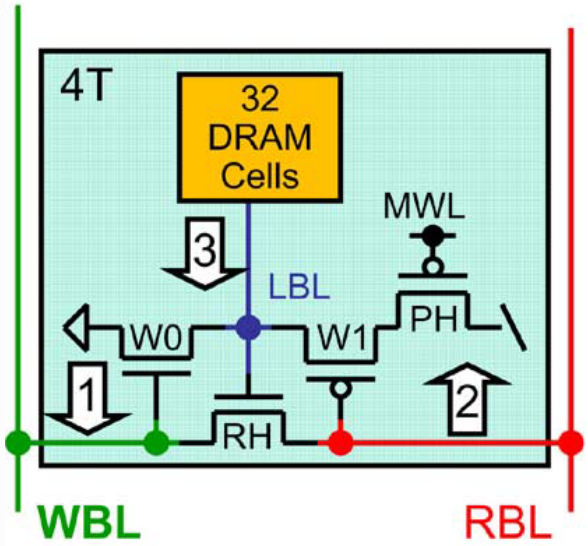
Single Ended Sense – Twist not effective
Line to Line Coupling must be managed

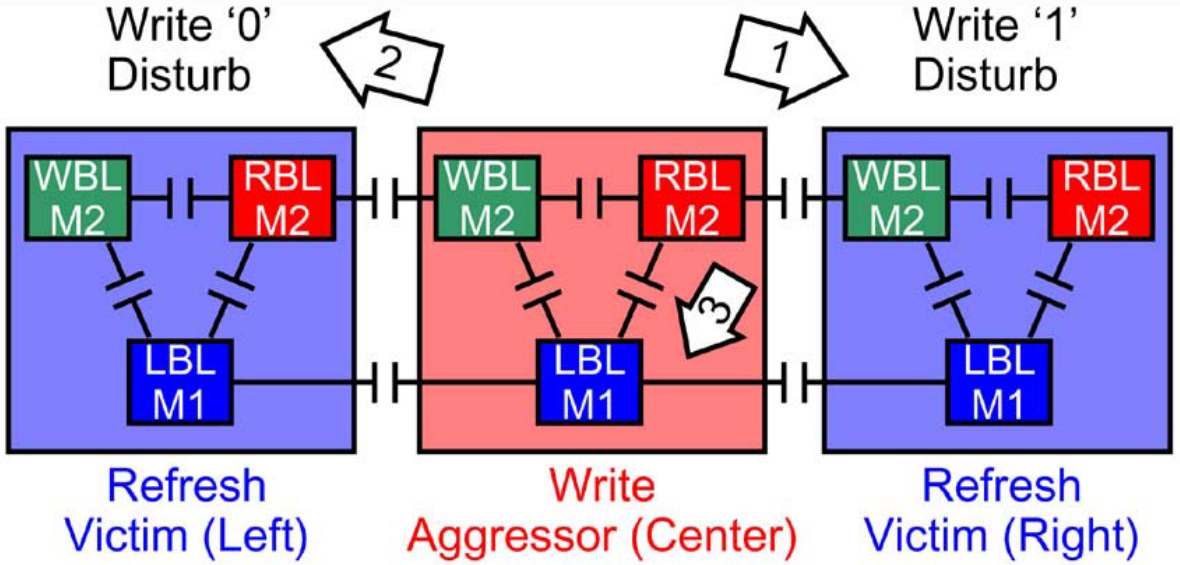
Question 2 (Feb 2 2017)

Q2. In a 3T micro sense amp, in stand by mode, the following leakage current is a serious concern

- Through PCW0
- Through RH
- Through FB
- Stand by leakage is not a concern

Micro Sense Coupling Mechanisms

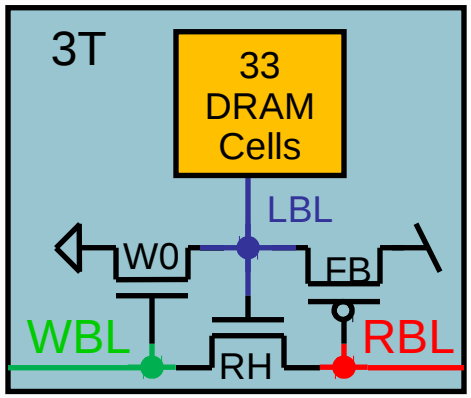




1. Write '1' Couples WBL below Ground
   Increasing RH leakage during Refresh '0'
2. Write '0' Couples RBL above VDD
   Delaying Feedback during Refresh '1'
3. Read '1' Couples Half-Selected LBL Below GND
   Increasing Array Device Sub-VT Leakage

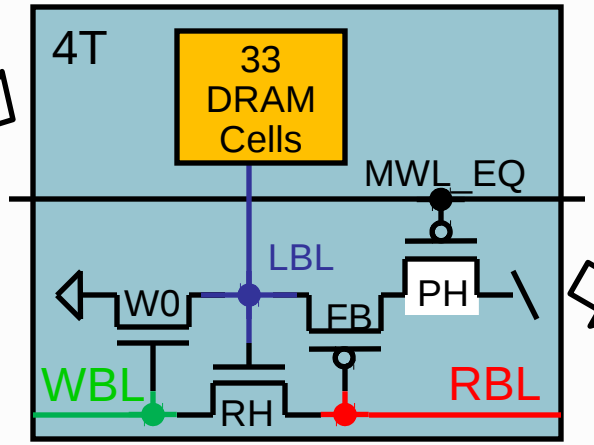
Micro Sense Evolution

1. Write Zero (W0)
2. Read Head (RH)
3. Feed-Back (FB)



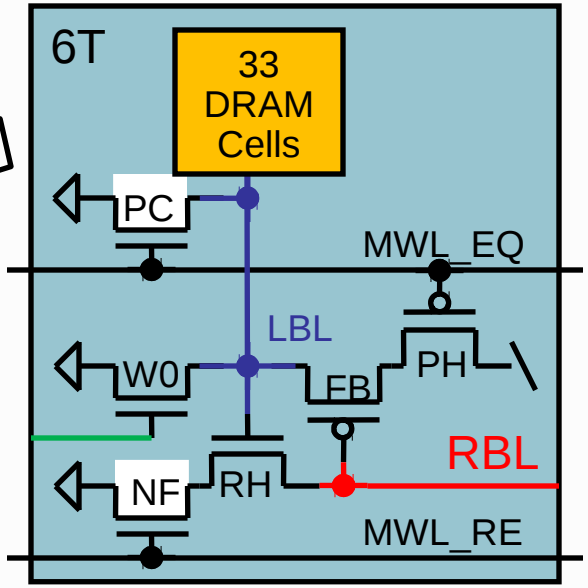
Barth, ISSCC'07

4. PFET Header (PH)
   - LBL Power Gate
   - LBL Leakage



Klim, VLSI'07

5. Pre-Charge (PC)
   - WBL Power (Write '0' Only)
6. NFET Footer (NF)
   - RBL Leakage
   - Decompose Pre-Charge and Read Enable (MWL_RE)



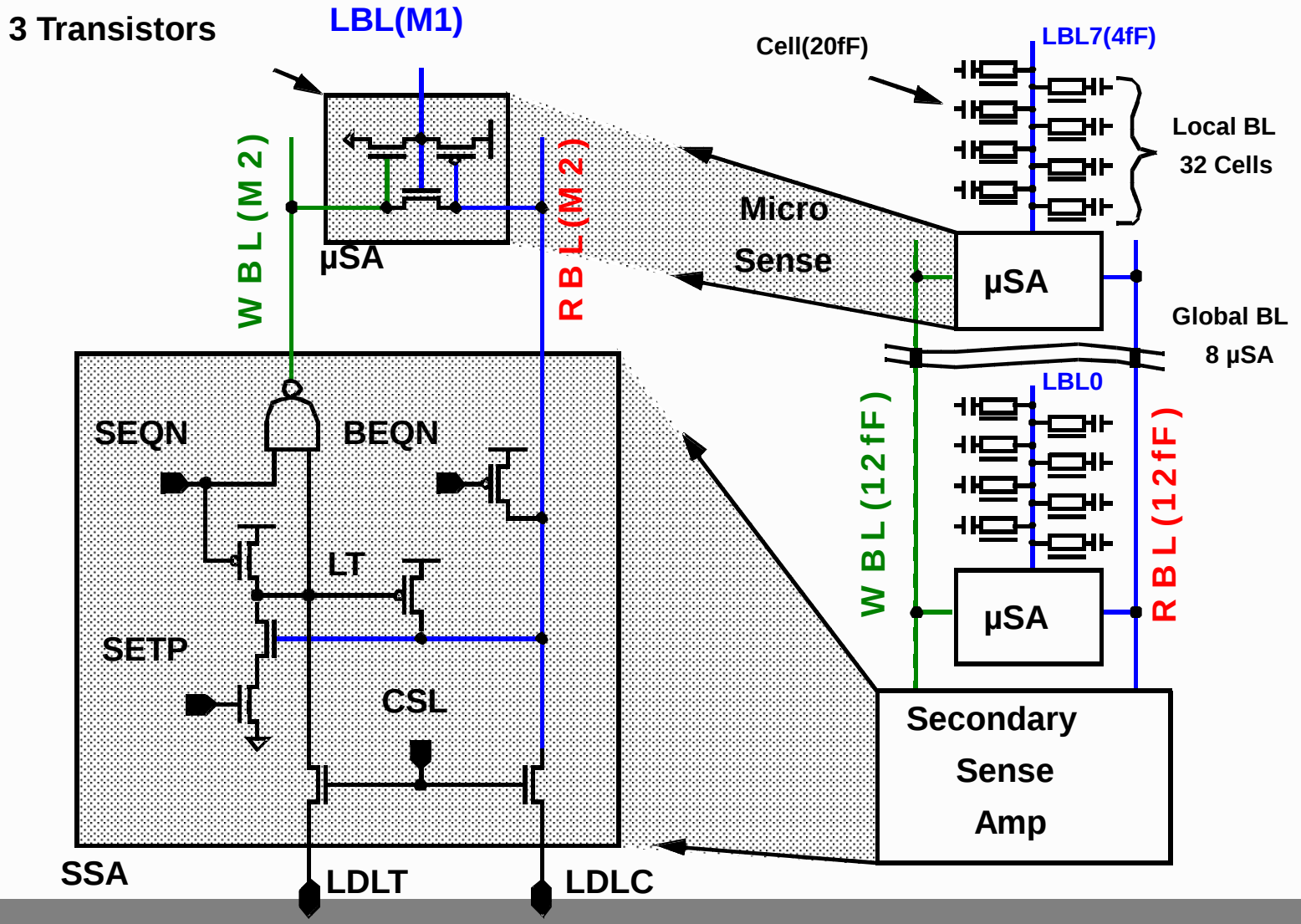
JSSC11

Power Reduction

Power Reduction
Traded for Transistor Count

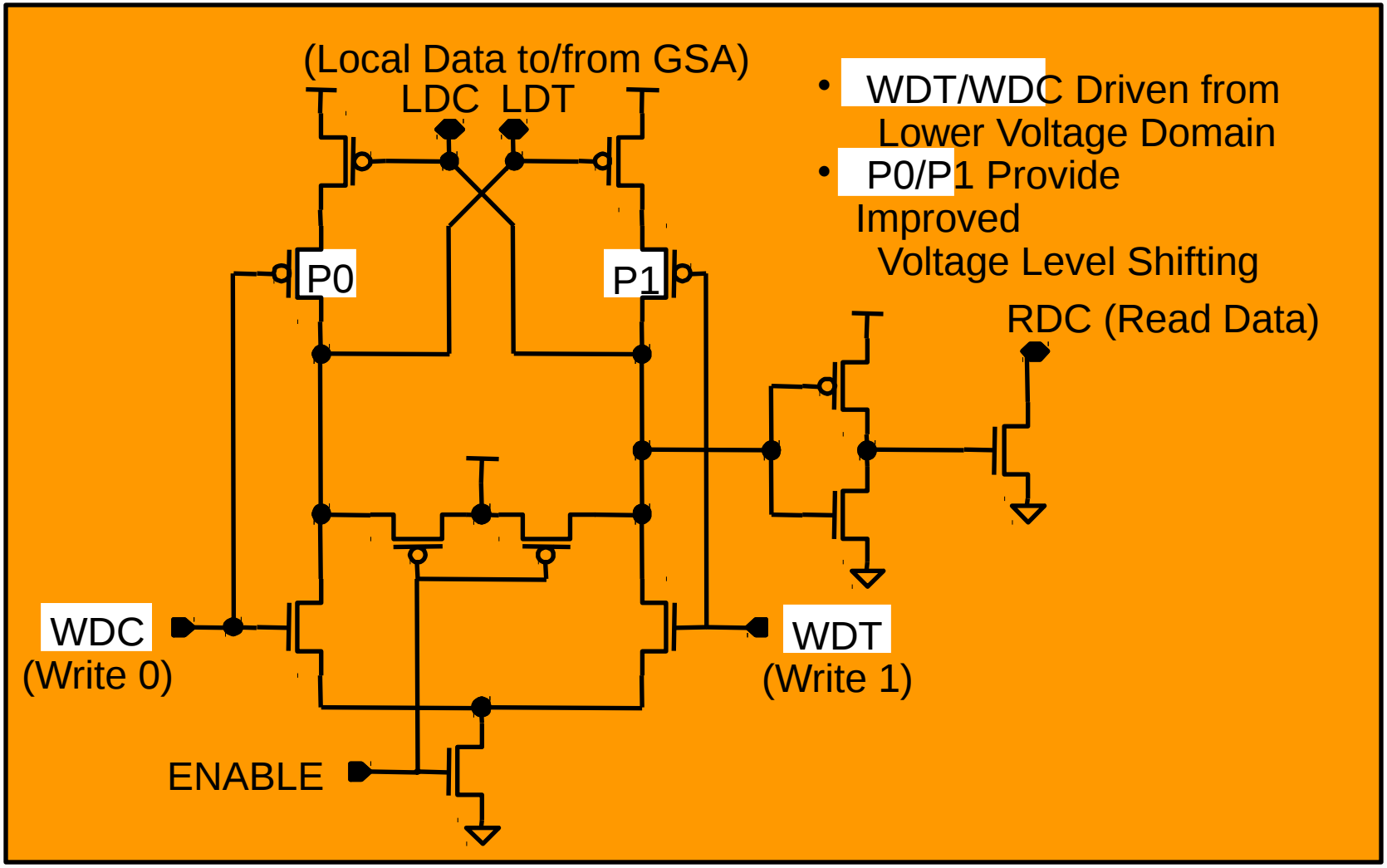
Increased Transistor Count

Micro Sense Architecture (μSA)



JSSC08

Data Sense Amp (DSA)

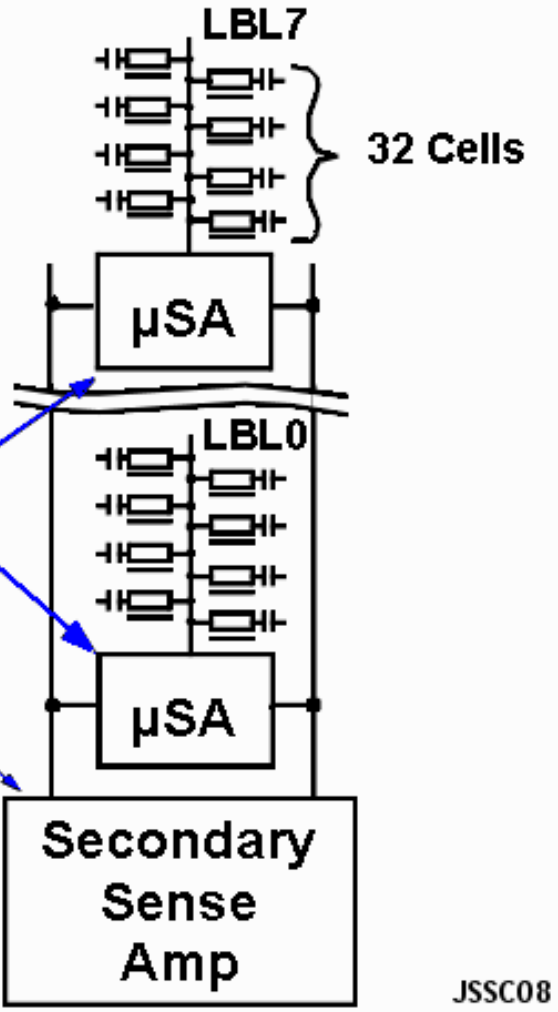


Micro Sense Advantage

Fast Performance of Short Bit-Line

Area Overhead of 4x Longer Bit-Line

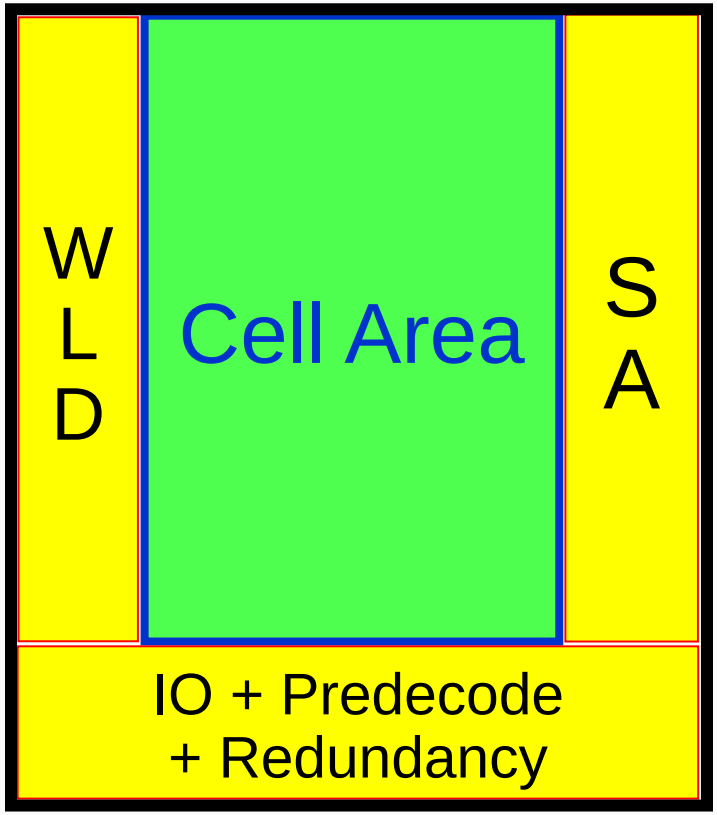
Bits/BL	256	128	32
Sense Amp	10%	20%	19%
Reference Cells	2.3%	4%	-
Twist Region	2%	2.6%	-
Second Sense Amp	-	-	8%
Total	14.3%	26.6%	27%



Same Overhead

JSSC08

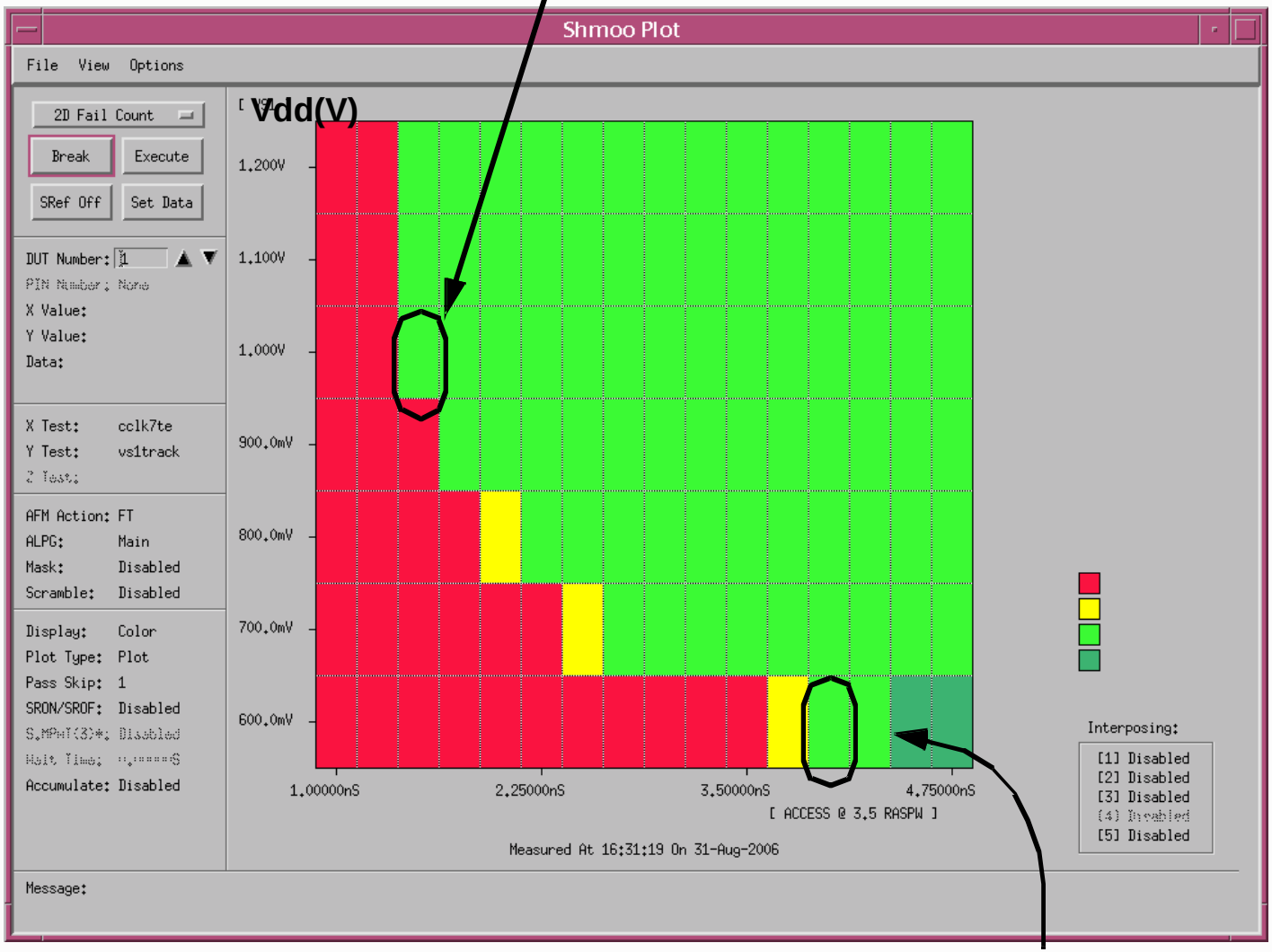
Array utilization



Utilization = $\frac{\text{Cell Area}}{\text{Total Area}}$

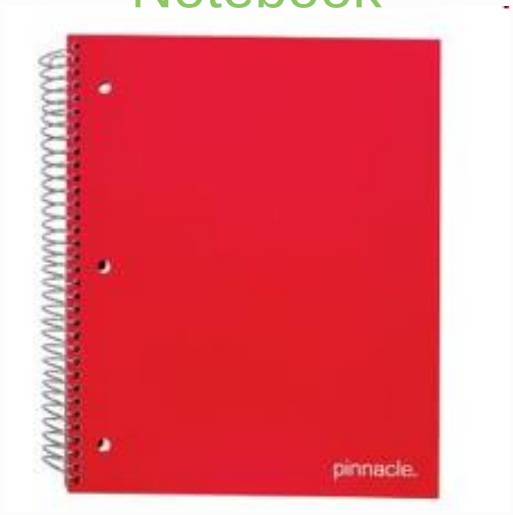
Mbits/mm^2

Access Shmoo



Redundancy

Notebook



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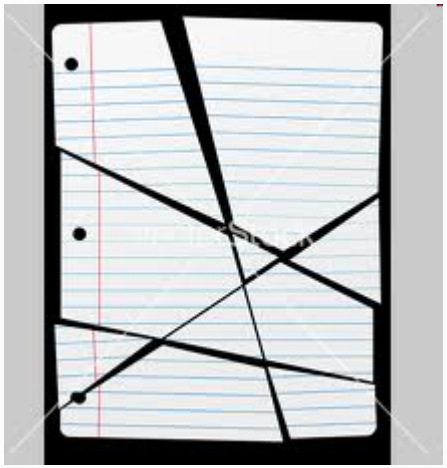
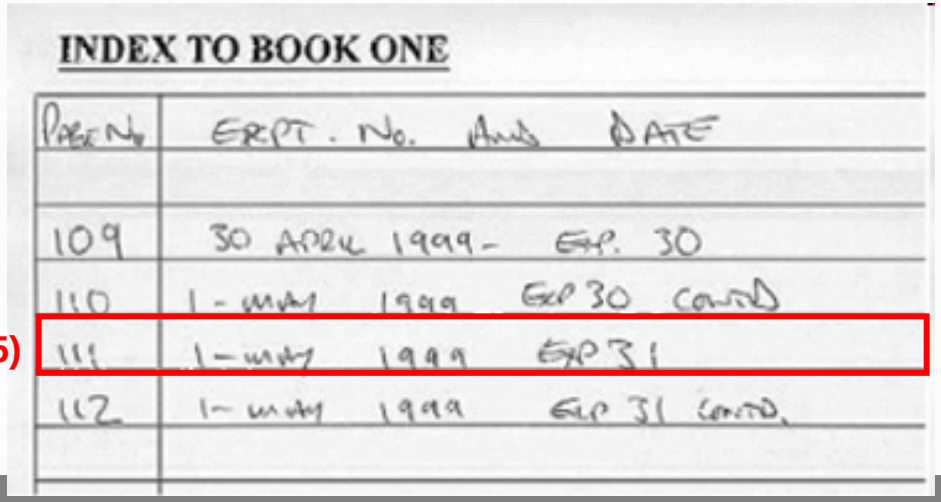


Extra Page R05

eFuse based repair table

(see page R05)



INDEX TO BOOK ONE

PAGE No.	EXPT. No. AND	DATE
109	30 APRIL 1999 -	EXP. 30
110	1 - MAY	1999 EXP 30 CONTD
111	1 - MAY	1999 EXP 31
112	1 - MAY	1999 EXP 31 CONTD.

Topics

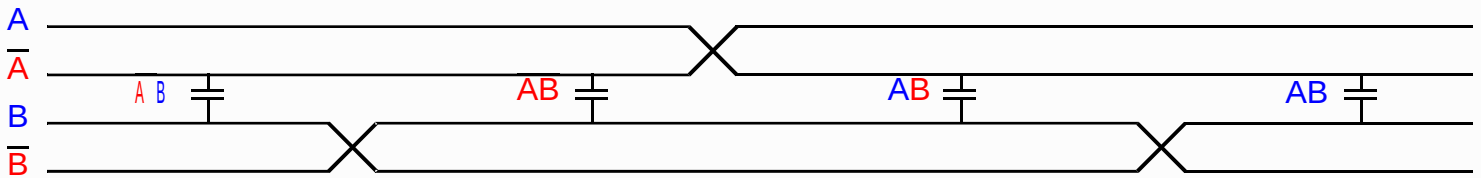
- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example

Noise

oupling and Local Process Variation effectively degrades signal

xternal Noise (Wire or Sx) Reduced to Common Mode by Folding

Line to Line Coupling Limited by Bit-Line Twisting



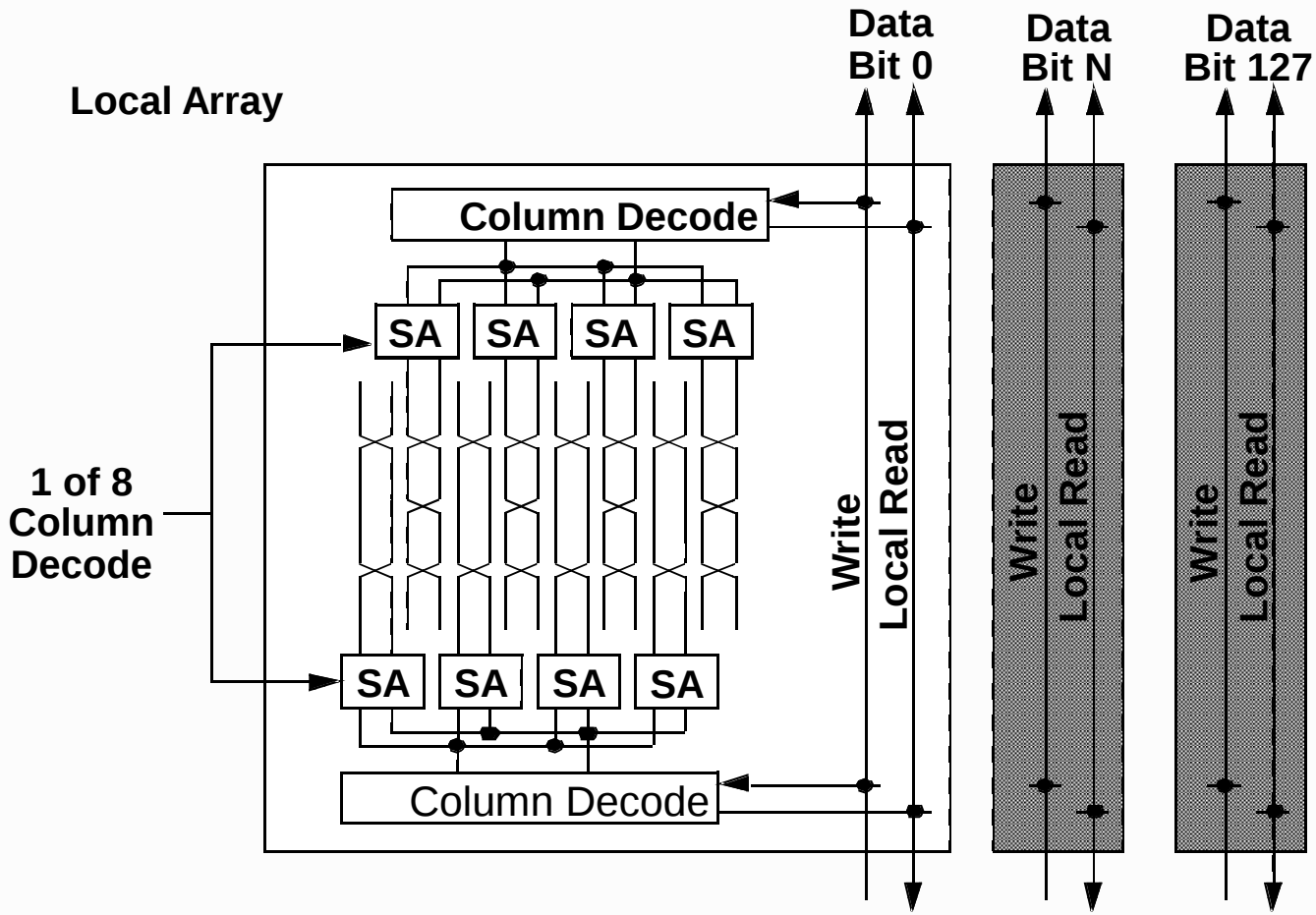
A Couples Equally into B and $\overline{B}$

V_t and L Mis-Match Limited by Longer Channel Length

Overlay Mis-Alignment Limited by Identical Orientation

apacitive Mis-Match Limited by careful Physical Design (Symmetry)

Interleaved Sense Amp w/ Bit-Line Twist



Open and Folded Bitline Schematic

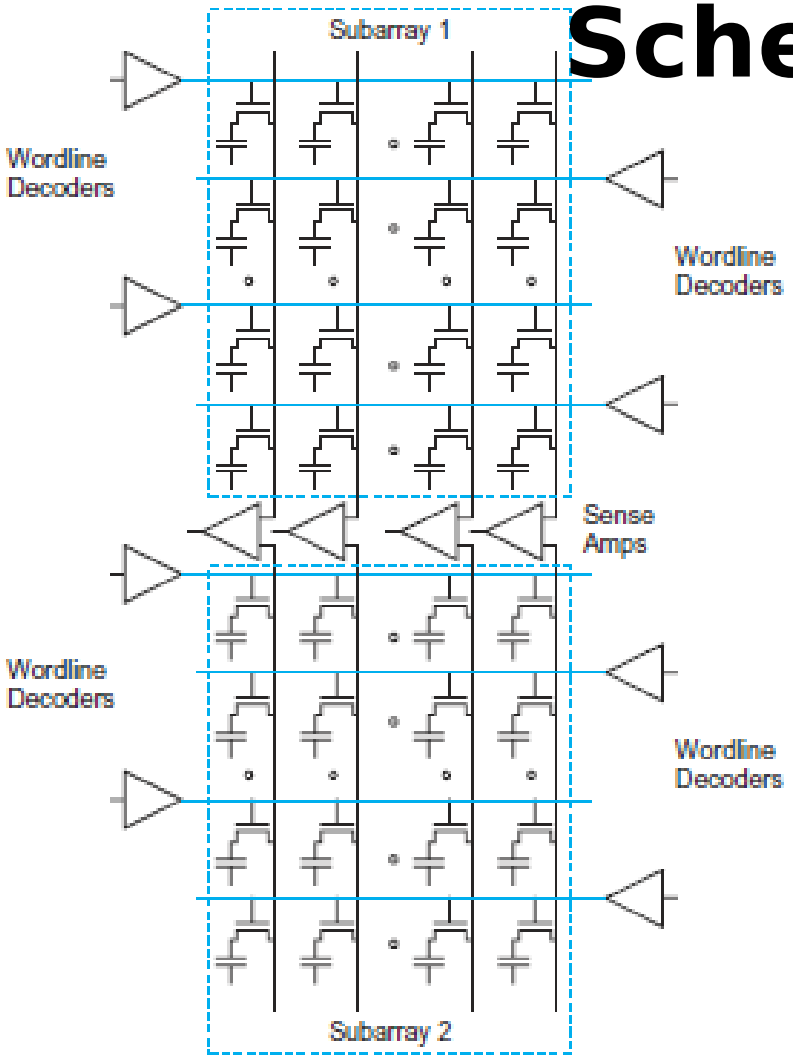


FIGURE 12.44 Open bitlines

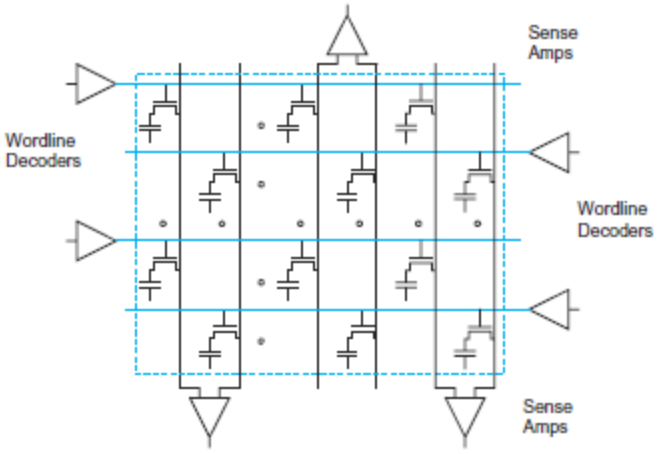


FIGURE 12.45 Folded bitlines

CMOS VLSI design - PEARSON

Folded Bitline Layout

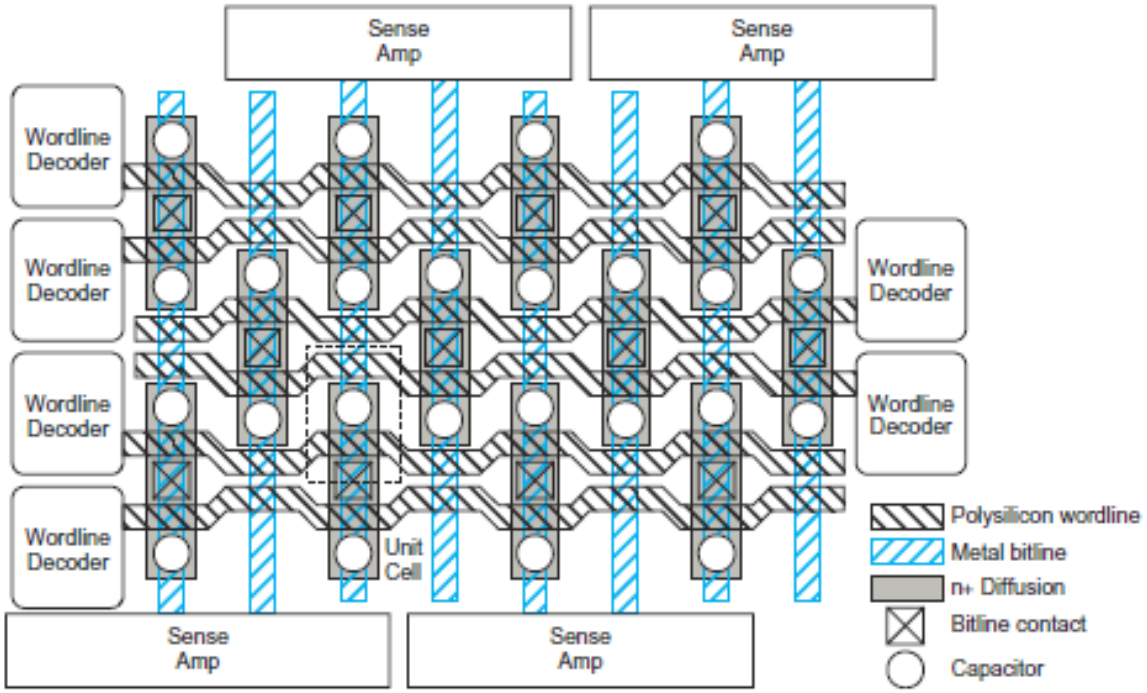


FIGURE 12.46 Layout of folded bitline subarray

Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
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- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example

Retention

Transfer Device and Storage Cap are NOT ideal devices: they LEAK
Leakage Mechanisms include: Ioff, Junction Leakage, GIDL,...
Junction Leakage Temperature Dependence = 2x/10C

Cell Charge needs to be replenished (Refreshed),
Median Retention Time:

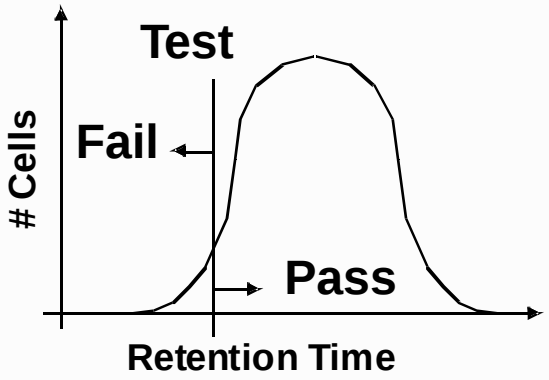
$$T = \frac{C\Delta V}{I_{leak}} = \frac{35fF \times 400mV}{2fA} = 7 \text{ seconds}$$

Where ΔV is acceptable loss
C is Cell Capacitance
I_{leak} is Total Leakage

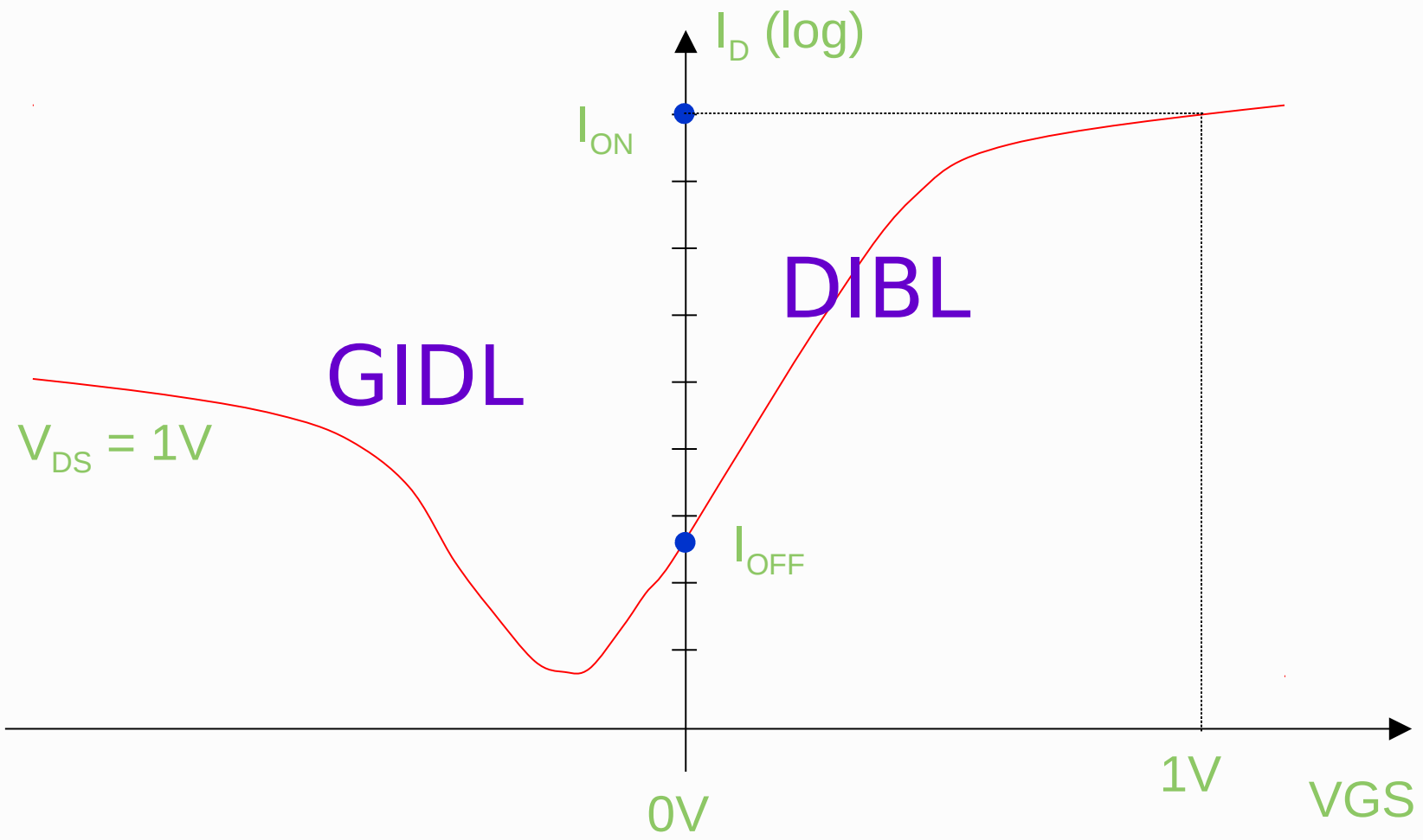
Retention Distribution has Tails created by Defects and Leaky Cells

Weak Cells Tested out (5x Guardband) and replaced with Redundancy

Customer issues periodic Refresh Cycle



Pass transistor leakage



Floating Body Effects

Body potential modulated by coupling and leakage

During write back, body voltage increases
⇒ Threshold voltage decreases ⇒ Better WRITE 1

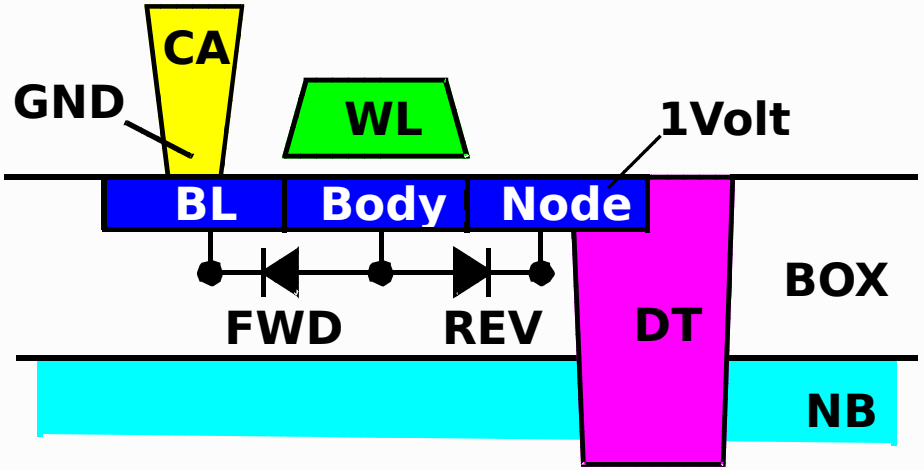
Degraded I_{off} / Retention if body floats high (body leakage)

⇒ GND pre-charge keeps body low

⇒ Eliminate long periods with BL high (limit page mode)

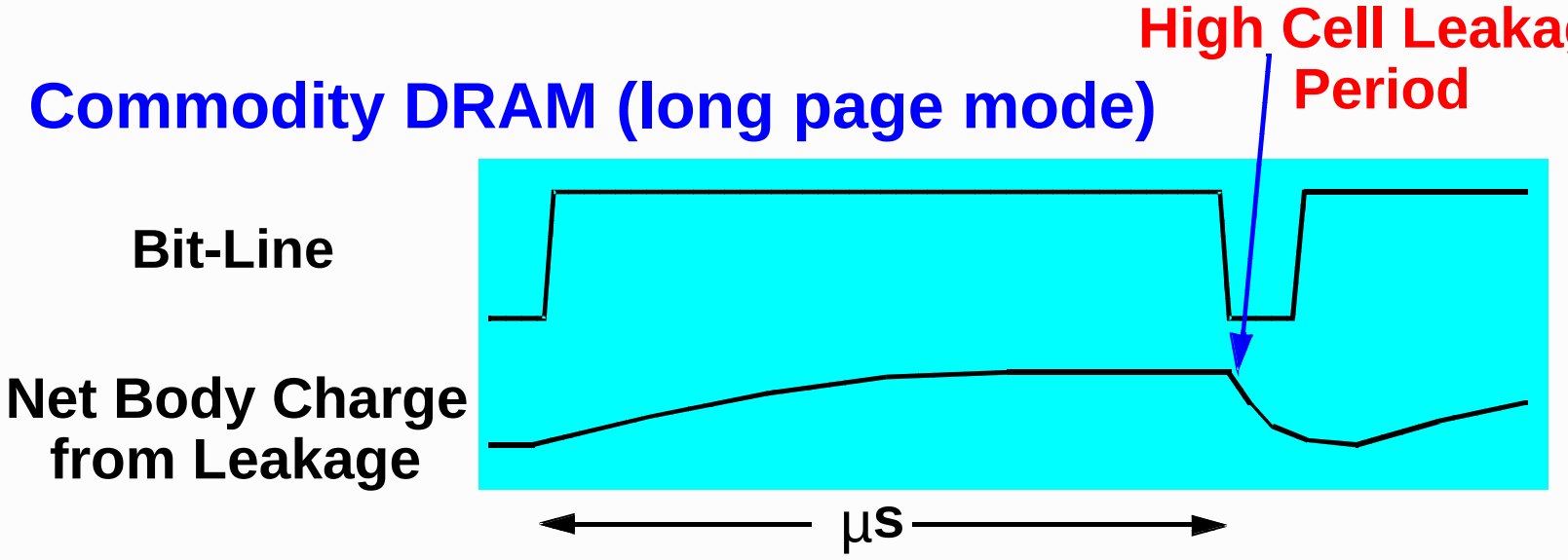
ILeak$_{FWD}$ > ILeak$_{REV}$

When BL = GND
Body⇒GND

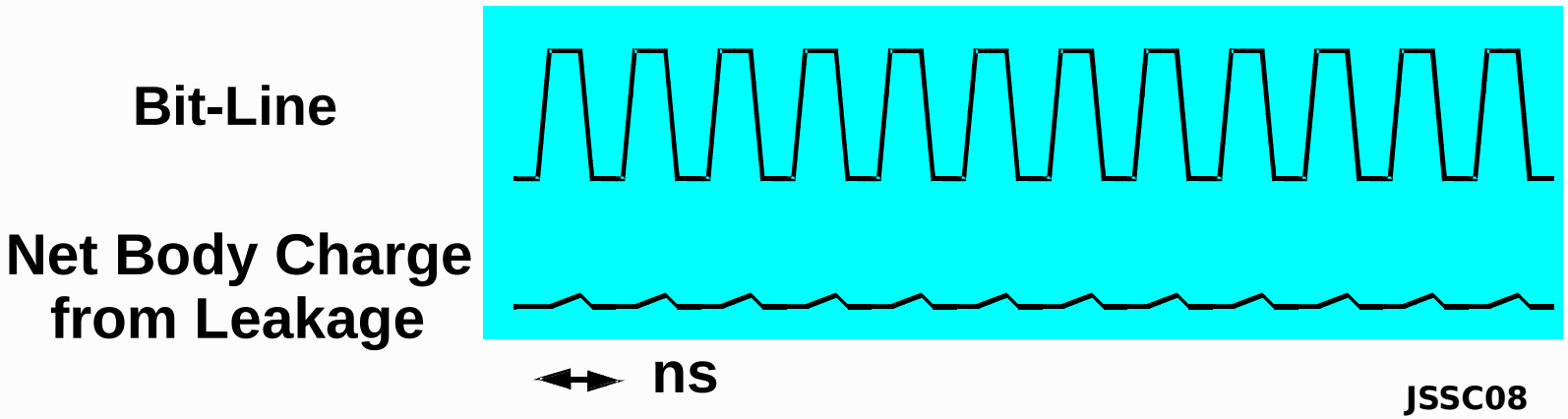


Array Body Charging

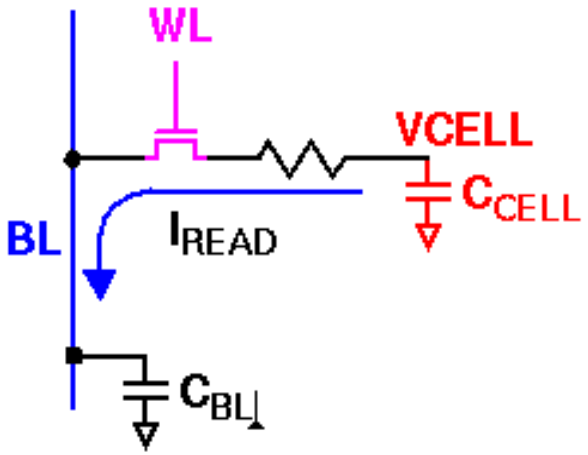
Commodity DRAM (long page mode)



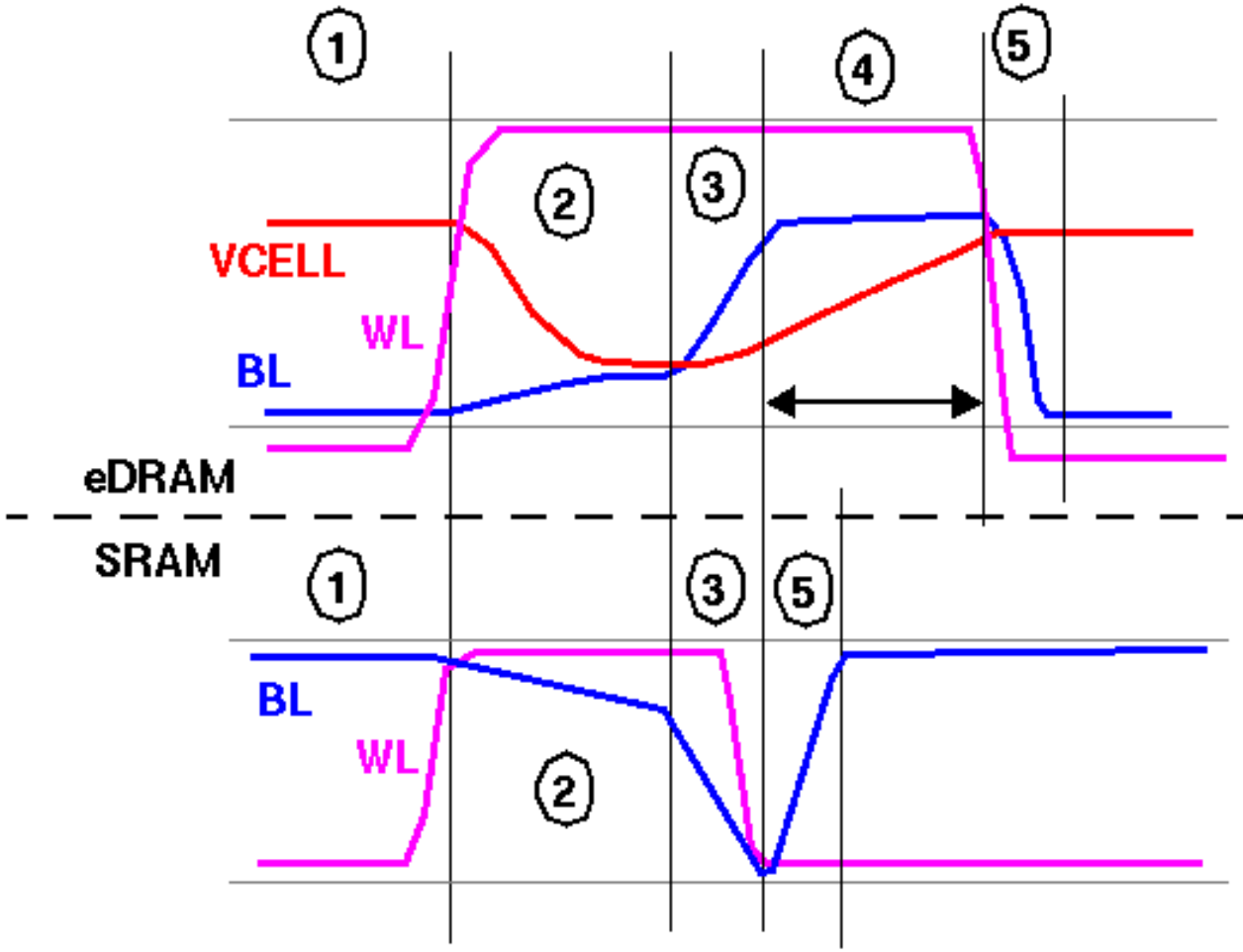
embedded DRAM (limited page mode)



eDRAM vs. SRAM Cycle-Time Comparison



1. WL Activation
2. Charge Transfer to Bit-Line
   (I_{READ} Similar to SRAM)
3. Amplification
4. Write-Back
5. Precharge

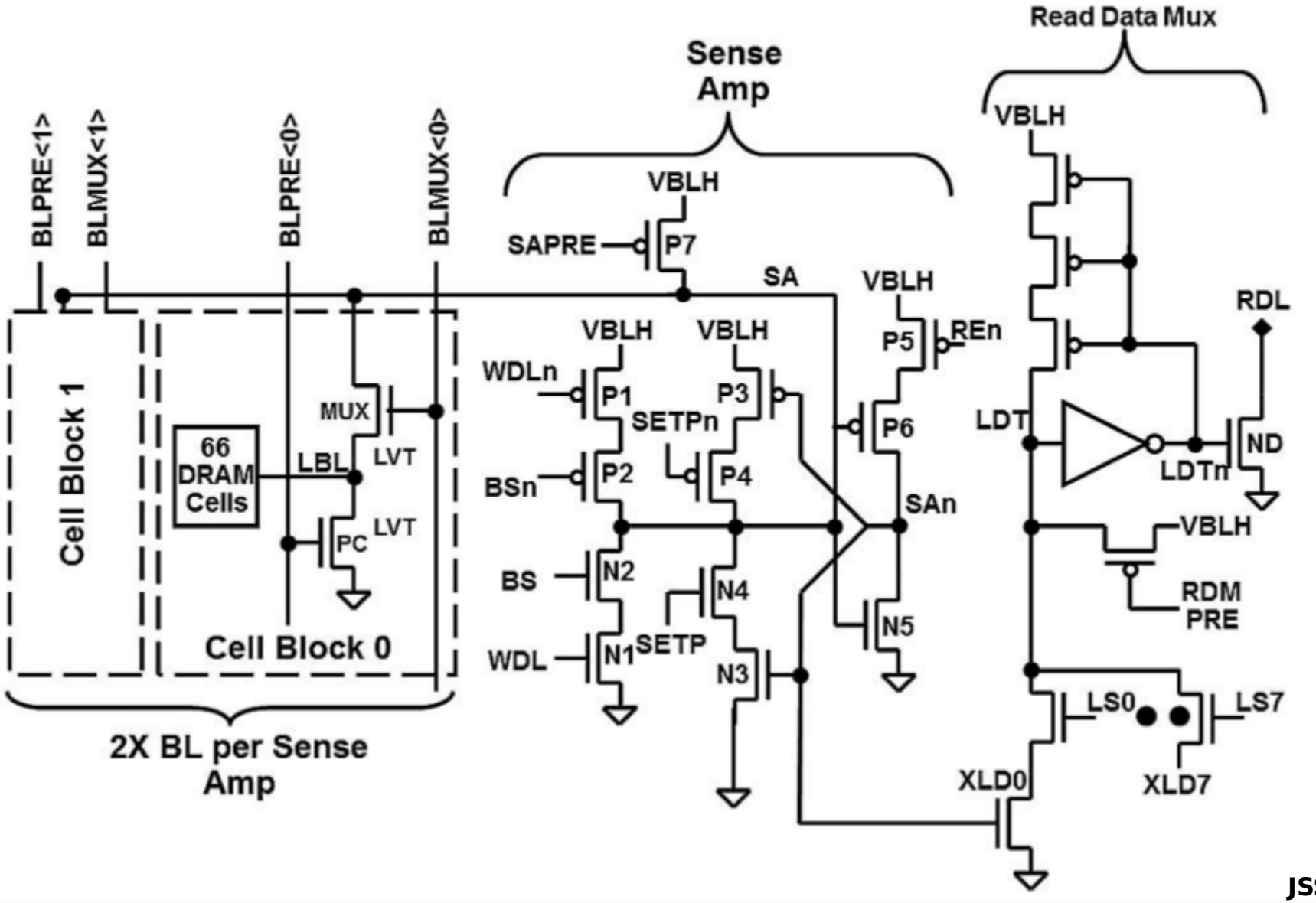


NET: SRAM Random Cycle will continue to lead!

Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
- Noise concerns
- Gated Feedback Sense Amplifier
- Challenges in eDRAM
- Understanding Timing diagram – An example

Gated Feedback Sense Amp



JSSC16

Question 3 (Feb 2 2017)

Q3. The logic one voltage level of BLMUX in a Gated Feedback Sense Amp (GSA) should be

- VDD
- VPP
- At least VDD + VT
- At most VPP - VT

Question 4 (Feb 2 2017)

Q4. SETPn and SETP are respectively used in a GSA to

- ○ Prevent early feedback and reduce leakage
- ○ Reduce leakage and prevent early feedback
- ○ Reduce leakage
- ○ Prevent early feedback

Question 5 (Feb 2 2017)

Q5. With regard to multiplexing BLs and sharing GSAs which of the following is true?

- Like in SRAM LBLs can be column multiplexed and shared with a GSA if the GSA is large enough
- Column multiplexing LBLs with the GSA saves area but is a minor advantage
- Depends on the layout symmetry
- Each LBL should necessarily be connected to a GSA

Question 6 (Feb 2 2017)

Q6. In a particular lot, the NFET is much slower and the PFET is much faster than expected. This will cause

- ○ Read 0 to be slower
- ○ Read 1 to be slower
- ○ Read 0 to be faster
- ○ Read 1 to be faster

Topics

- Introduction to memory
- DRAM basics and bitcell array
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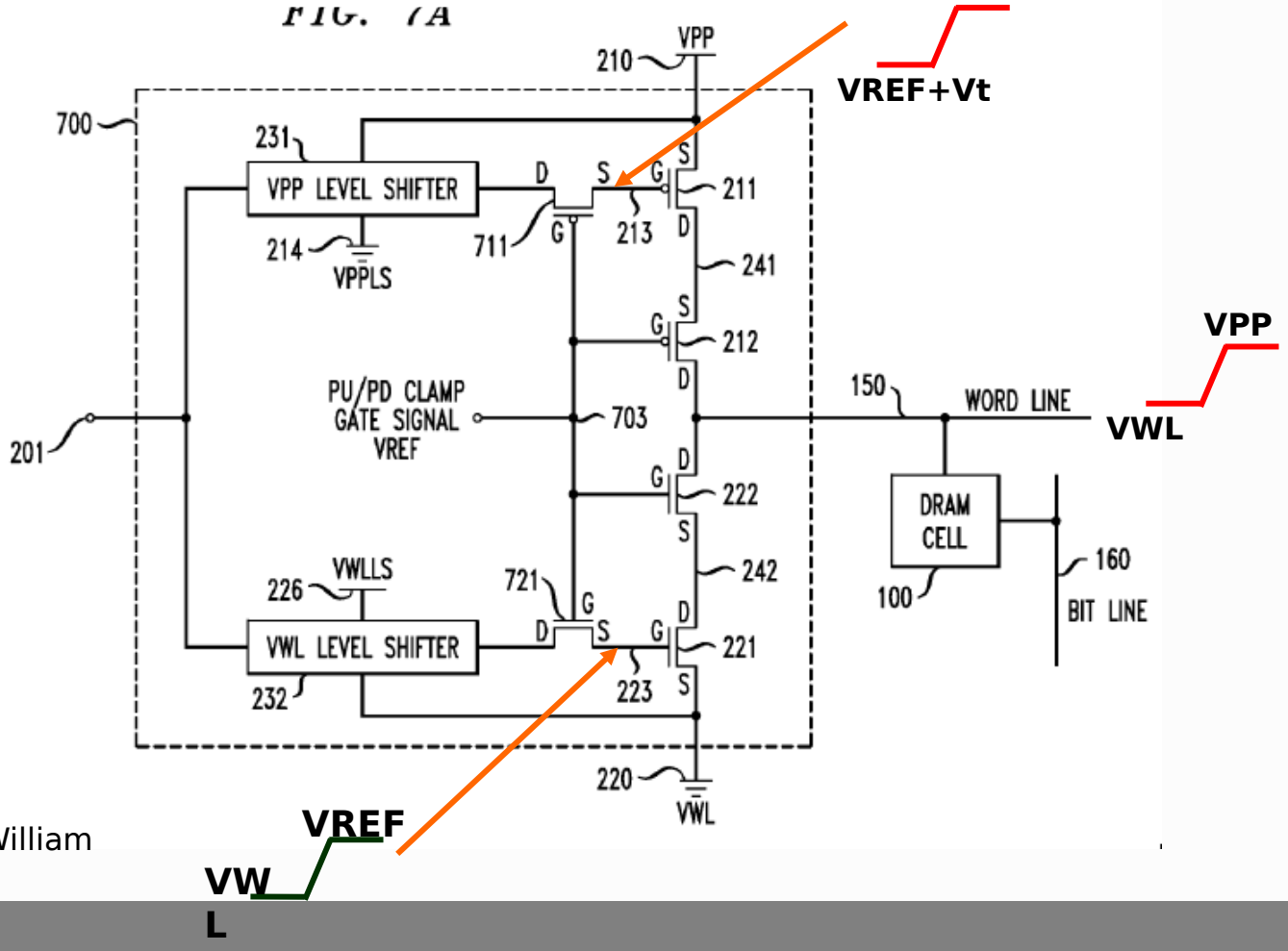
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example

WLDRV

Driver with Low voltage transistors Logic transistors

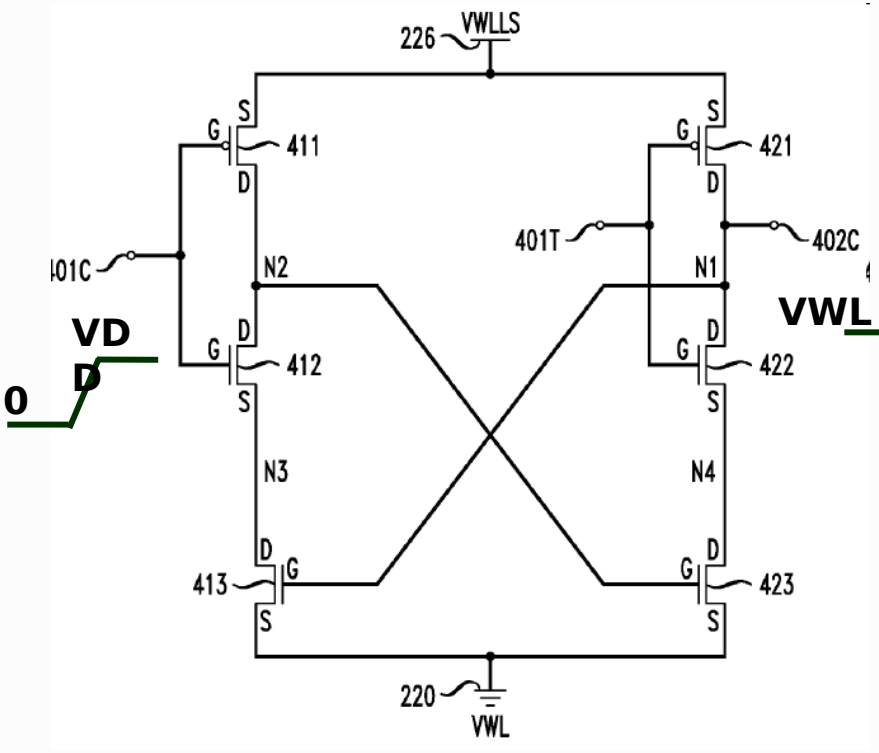
No thick gate oxide transistors required!!

Voltage across any two terminals should not exceed reliability limits

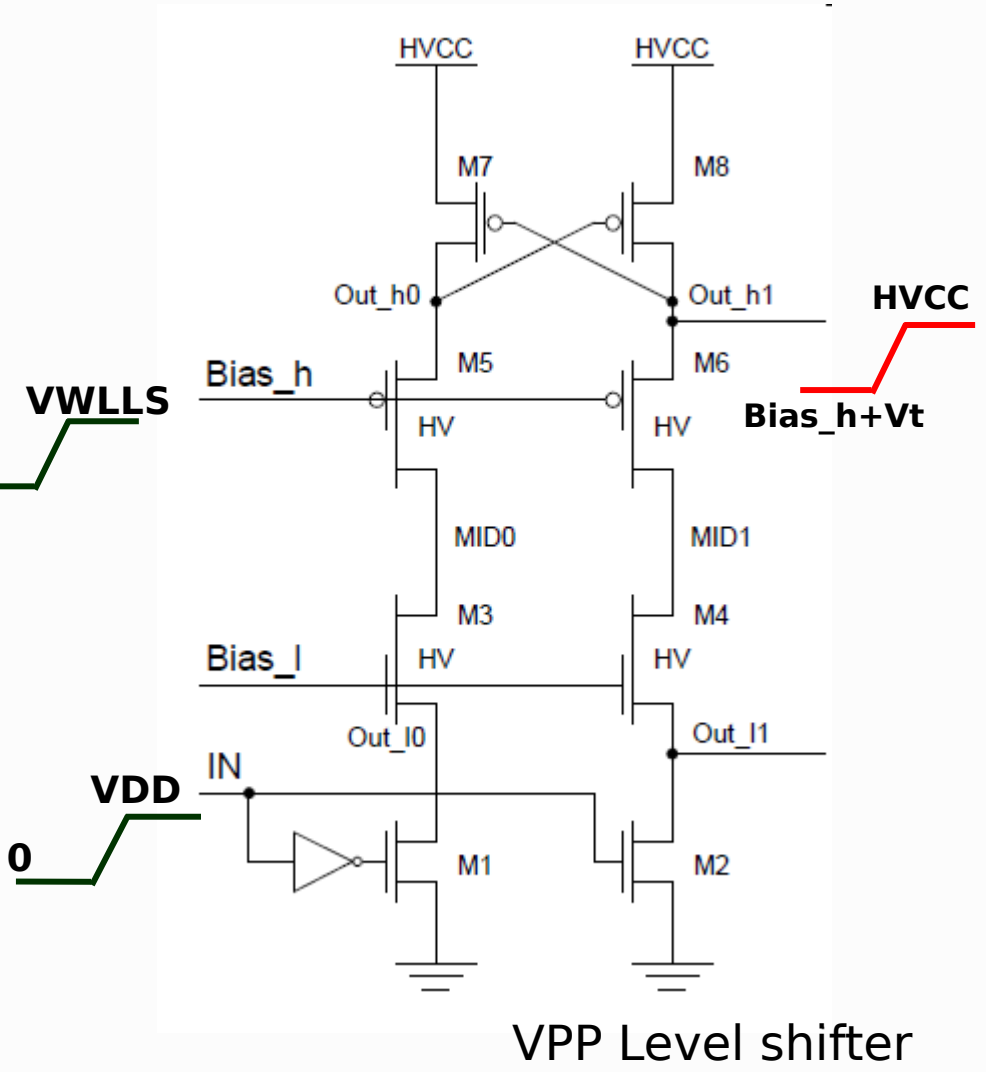


1. US patent No: 8,120,968 William Robert Reohr, John E Barth

LEVEL Shifter



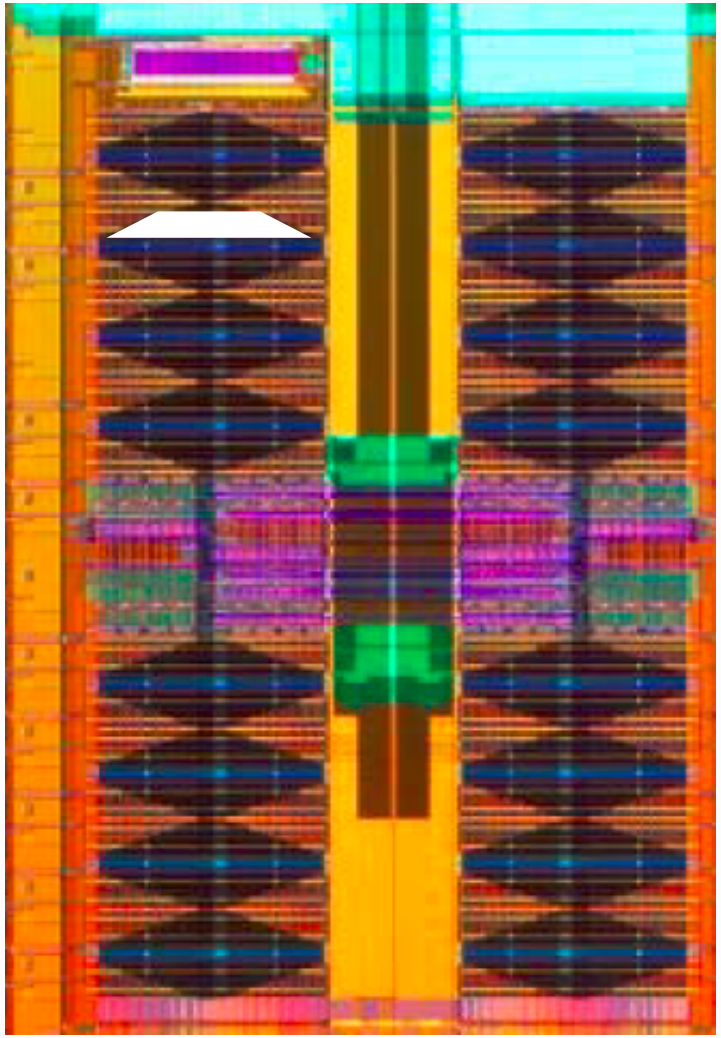
VWL Level shifter

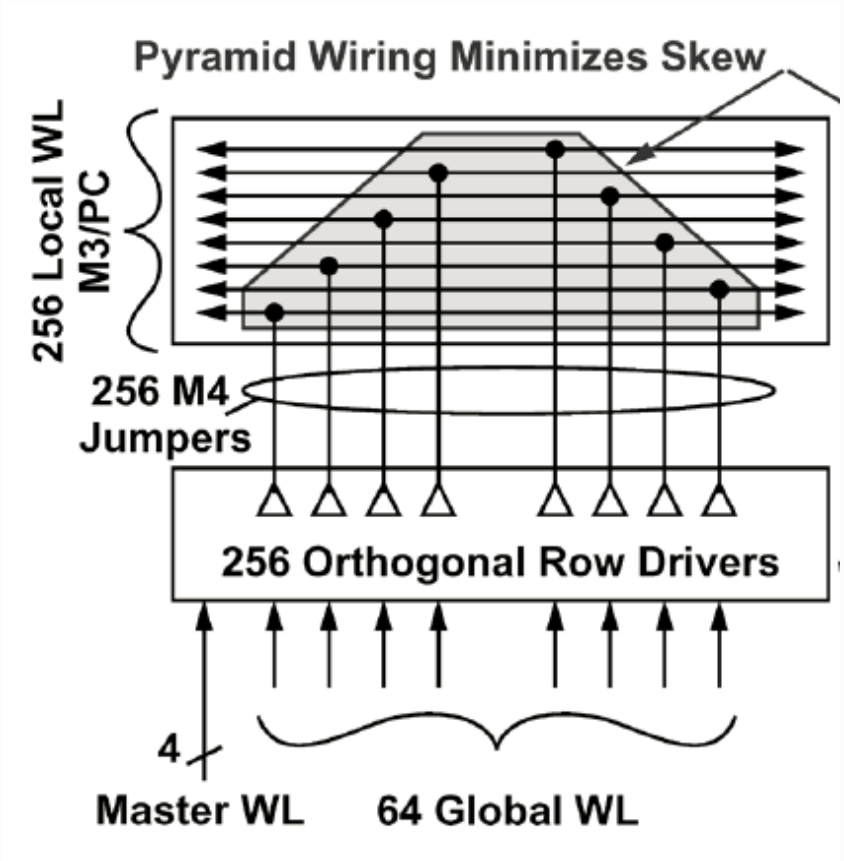


VPP Level shifter

1. US patent No: 8,120,968 – William Robert Reohr, John E Barth
2. A Low Voltage to High Voltage Level Shifter Circuit for MEMS Application – Dong Pan

Orthogonal WLD and pyramid wiring (M3/M4)





JSSC08

Question 7 (Feb 2 2017)

Q7. Applying a voltage swing of VPP to VWL (~2 V) across a standard NFET is not advisable because

- ○ It can break the device
- ○ Causes the VT of the device to reduce over time
- ○ Causes the VT of the device to increase over time
- ○ It's maybe a reliability concern depending on where it is placed in the layout

Topics

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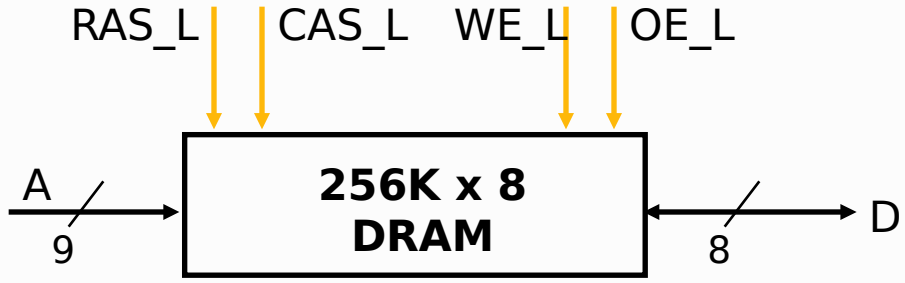
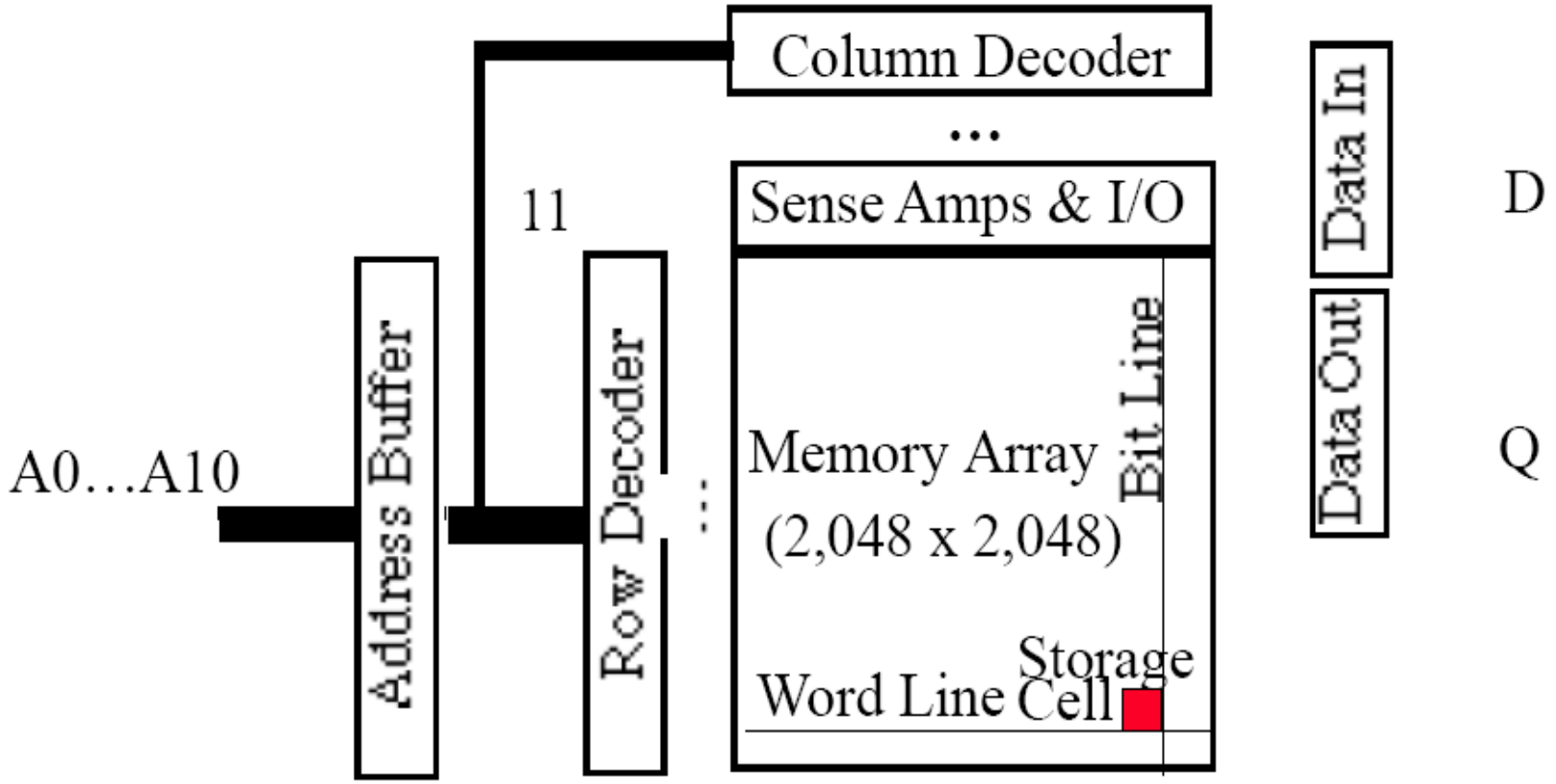
- Challenges in eDRAM
- Understanding Timing diagram – An example

Logic Diagram of a Typical DRAM



- Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
- Din and Dout are combined (D):
  - WE_L is asserted (Low), OE_L is disasserted (High)
    - D serves as the data input pin
  - WE_L is disasserted (High), OE_L is asserted (Low)
    - D is the data output pin
- Row and column addresses share the same pins (A)
  - RAS_L goes low: Pins A are latched in as row address
  - CAS_L goes low: Pins A are latched in as column address
  - RAS/CAS edge-sensitive

DRAM logical organization (4 Mbit)

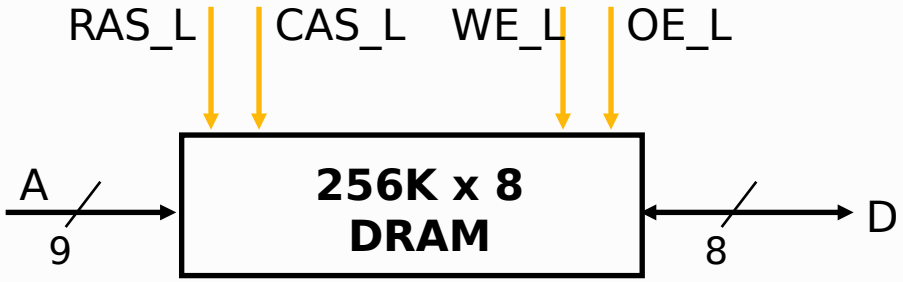


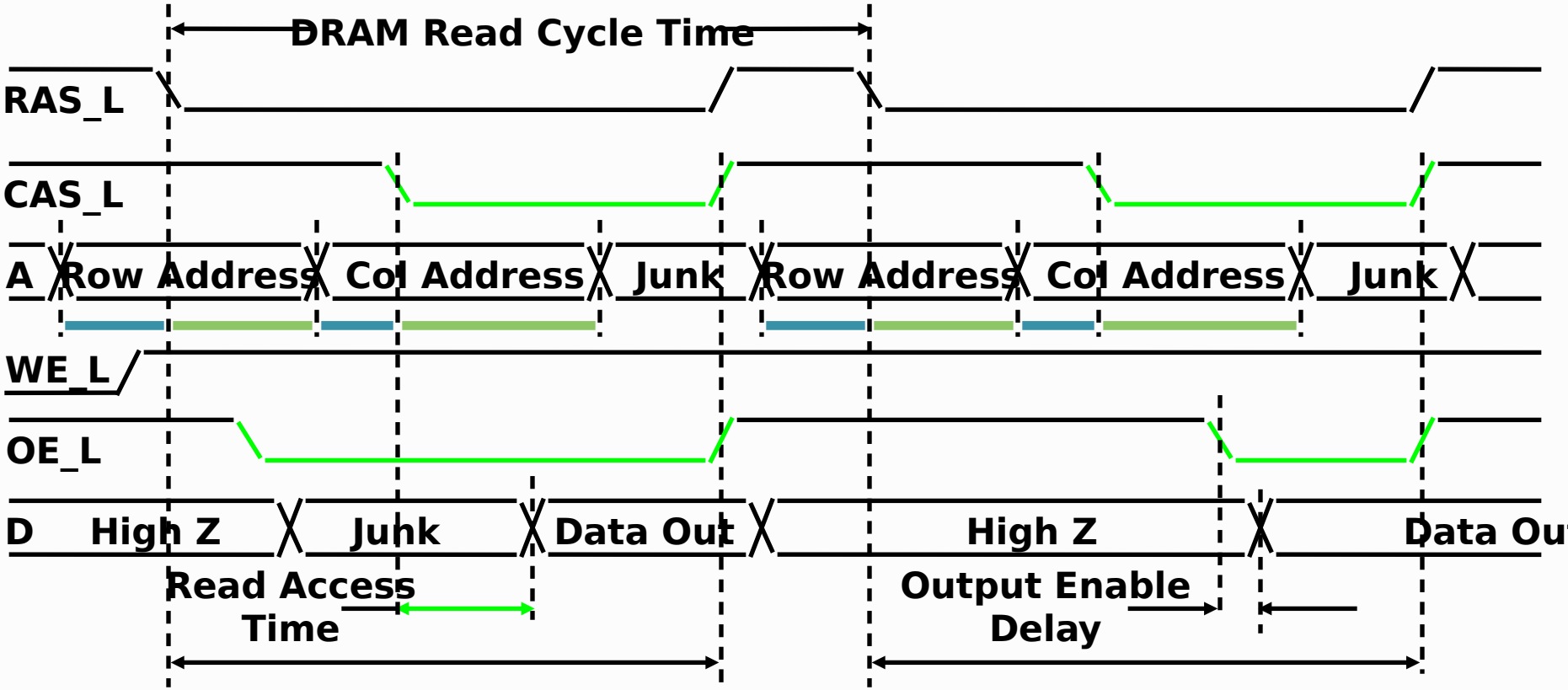
- **Square root of bits per RAS/CAS**

Din Dout can be clubbed together with a BiDi buffer

DRAM Read Timing

- Every DRAM access begins at:
  - The assertion of the RAS_L
  - 2 ways to read:
    early or late v. CAS

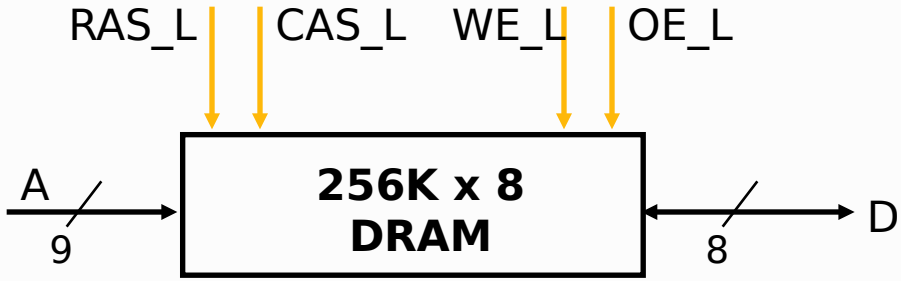


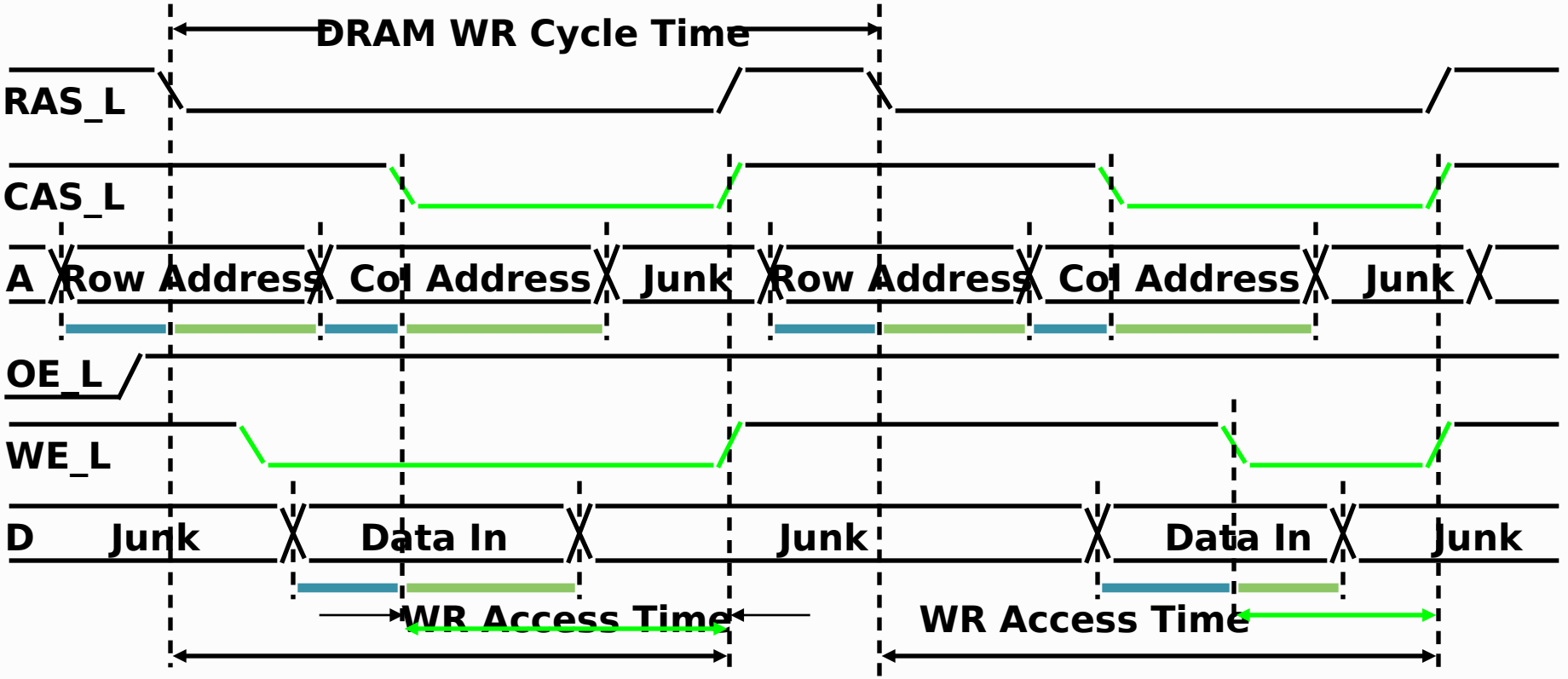


rly Read Cycle: OE_L asserted before CAS_L Late Read Cycle: OE_L asserted after CAS_

DRAM Write Timing

- Every DRAM access begins at:
  - The assertion of the RAS_L
  - 2 ways to write:
    early or late v. CAS





rly Wr Cycle: WE_L asserted before CAS_L

Late Wr Cycle: WE_L asserted after CAS_L

Conclusion

- Pulling more DRAM cache (L2,L3) inside the processor improves overall performance
- eDRAM design using logic process is a challenge
- Case study is done, covering many of the eDRAM design aspects

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