Advanced Topics in VLSI

EE6361

Jan 2017
Course Objectives

- Introduce students to some relevant advanced topics of current interest in academia and industry
- Make students aware of some advanced techniques
- Make students aware of work happening in India
Current Topics

- Embedded Memory Design
  - DRAMs + Yield Estimation (Janakriaman, IITM)
  - SRAMs (Rahul Rao, IBM India)
- TCAMs (Self Study)
- Electronic Design Automation for Circuits (Sridhar Rangarajan, IBM India)
Learning Objectives for EDRAM

- Explain the working of a (e)DRAM. What is Embedded mean?
- Explain the working of a feedback sense amplifier and modify existing designs to improve performance
- Calculate the voltage levels of operation of various components for an eDRAM
- Introduce stacked protect devices to reduce voltage stress of the WL driver
- Calculate the number of samples required to estimate yield to specified accuracy and confidence
- Explain the use of importance sampling to reduce the number of samples required in step 6
Learning Objectives for SRAM

- Articulate memory hierarchy and the value proposition of SRAMs in the memory chain + utilization in current processors
- Explain SRAM building blocks and peripheral operations and memory architecture (with physical arrangement)
- Articulate commonly used SRAM cells (6T vs 8T), their advantages and disadvantages
- Explain the operation of a non-conventional SRAM cells, and their limitations
- Explain commonly used assist methods
- Explain how variations impact memory cells
Learning Objectives for EDA

- Describe the role of CAD tools in VLSI Physical Design process.
- Explain various design phases and physical design flow
- Articulate the commonly used algorithms in physical design tools
- Detailed understanding of placement and routing techniques.
- Describe the role of physical synthesis in design closure
- Incremental synthesis and optimization and its role in physical design closure

If time permits

- Articulate as how static timing analysis works
- Articulate leakage and dynamic power modelling
Grading

- Assignments – 20%
- Self Study Seminar – 20%
- Quiz – 20%
- End Semester – 40%
Refresher
Refresher

- Inverter trip point and noise margins
- Short Channel Effect
  - Sub-threshold leakage
  - DIBL
  - GIDL
- Stacking Effect
- Pass transistors
- 6T SRAM basics
Review of SRAM

- Basic 6T SRAM cell
- Read and Write operation
  - Sizing of devices
- Sense Amps
6T SRAM

BLT

WL

BLC
6T SRAM Array

Slide 12

Introduction of eDRAM
SRAMs cannot be pre-charged to ground because

- The pull up PFET will malfunction
- The pass transistor is an NFET and hence will not allow a successful read ONE
- The pass transistor is an NFET and hence read ONE will be slow
- Who said you can’t precharge to ground?
6T SRAM Array

... In an SRAM, PD = Pull down NFET, PU = Pull up PFET and PT = Pass transistor

- PD > PT > PU
- PD > PU > PT
- PU > PT > PD
- Size doesn't matter!
Embedded DRAM

Janakiraman V
Assistant Professor
Electrical Department
IIT Madras
Topics

- Introduction to memory
- DRAM basics and bitcell array
- eDRAM operational details (case study)
- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example
- References
Acknowledgement

- Raviprasad Kuloor (Course slides were prepared by him)
- John Barth, IBM SRDC for most of the slides content
- Madabusi Govindarajan
- Subramanian S. Iyer
- Many Others
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Memory Classification revisited

Memory Arrays

Random Access Memory
- Volatile Memory (RAM)
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)

- Nonvolatile Memory (ROM)
  - Mask ROM
  - Programmable ROM (PROM)
  - Erasable Programmable ROM (EPROM)

Serial Access Memory
- Serial In Parallel Out (SIPO)
- Parallel In Serial Out (PISO)

- Shift Registers
- Queues
  - First In First Out (FIFO)
  - Last In First Out (LIFO)

Content Addressable Memory (CAM)
- Electrically Erasable Programmable ROM (EEPROM)
- Flash ROM
Motivation for a memory hierarchy – infinite memory

Cycles per Instruction (CPI) = Number of processor clock cycles required per instruction

CPI[∞ cache]
Finite memory speed

CPI = CPI[∞ cache] + FCP

Finite cache penalty
Locality of reference – spatial and temporal

**Temporal**
If you access something now you’ll need it again soon e.g. *Loops*

**Spatial**
If you accessed something you’ll also need its neighbor e.g. *Arrays*

*Exploit this to divide memory into hierarchy*
Cache size impacts cycles-per-instruction

Logic-based eDRAM: Origins and rationale for use

R. E. Matick
S. E Schuster

IBM J. RES. & DEV. VOL. 49 NO. 1 JANUARY 2005

CPU

L1 cache
mr$_1$

L2 cache

Misses

L2 hits / I × T$_2$ cycles per hit

Hits

No. of L2 hits per instruction
mr$_1$ − mr$_2$

Finite cache penalty

DELAY / I for L2 hits + Delay / I for L3 hits + Delay / I for L4 hits ...

FCP

(mr$_1$ − mr$_2$) T$_2$ + (mr$_2$ − mr$_3$) T$_3$ + (mr$_3$ − mr$_4$) T$_4$ + ...

Cycles per instruction = Hits per instruction × cycles per hit

L3 cache

Misses

L3 hits / I × T$_3$ cycles per hit

Hits

No. of L3 hits per instruction
mr$_2$ − mr$_3$

L4 cache

Hits

L4 hits / I × T$_4$ cycles per hit

No. of L4 hits per instruction
mr$_3$ − mr$_4$

Access rate reduces: Slower memory is sufficient
Cache size impacts cycles-per-instruction

For a 5GHz processor, scale the numbers by 5x
Technology choices for memory hierarchy

Chart: J. Barth

Cost

Performance

- NOR FLASH: \( \sim 9F^2 \)
- NAND FLASH: \( \sim 4.5F^2 \)
- DRAM: 6-8\( F^2 \)
- SRAM
- Hard Disk
- Tbits/in\(^2\)
- Hard Disk

Hard Disk

Chart: J. Barth
eDRAM L3 cache

Move L2, L3 Cache inside of the data hungry processor
Higher hit rate → Reduced FCP
Embedded DRAM Advantages

**Memory Advantage**
- 2x Cache can provide > 10% Performance
- ~3x Density Advantage over eSRAM
- 1/5x Standby Power Compared to SRAM
- Soft Error Rate 1000x lower than SRAM
- Performance ? DRAM can have lower latency !
- IO Power reduction

**Deep Trench Capacitor**
- Low Leakage Decoupling
- 25x more Cap / µm² compared to planar
- Noise Reduction = Performance Improvement
- Isolated Plate enables High Density Charge Pump
Cache performance – SRAM vs. DRAM

Chart: Matick & Schuster, op. cit.
Embedded DRAM Performance

45nm eDRAM vs. SRAM Latency

- eDRAM Total Latency
- SRAM Total Latency
- eDRAM Wire/Repeater Delay
- SRAM Wire/Repeater Delay

Memory Block Size Built With 1Mb Macros

Barth ISSCC 2011
Comparing SRAM and eDRAM which of the following is true?

- eDRAM can be faster than SRAM for small size memories
- SRAM is more susceptible to SEUs
- SRAM process of manufacturing is more complicated
- Stand by power in SRAM is lower
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Memory Arrays are composed of Row and Columns

Most DRAMs use 1 Transistor as a switch and 1 Cap as a storage element (Dennard 1967)

Single Cell Accessed by Decoding One Row / One Column (Matrix)

Row (Word-Line) connects storage Caps to Columns (Bit-Line)

Storage Cap Transfers Charge to Bit-Line, Altering Bit-Line Voltage
1T1C DRAM Cell Terminals

Voltage Levels?
1T1C DRAM Cell Terminals

Word-Line (VWL to VPP Swing)

Bit-Line (0 to VDD)

Cap (0 to VDD)

Back Bias (VBB - Bulk Only)

VWL: GND or Negative for improved leakage

VPP: 1.5V up to 3.5V depending on Technology

VBB: Typically Negative to improve Leakage

Not practical on SOI

IBM J RES & DEV 2005
DRAM cell Cross section

- Store their contents as charge on a capacitor rather than in a feedback loop.
- 1T dynamic RAM cell has a transistor and a capacitor.

CMOS VLSI design - PEARSON
Storing data ‘1’ in the cell

Vgs for pass transistor reduces as bitcell voltage rises, increasing Ron

Why there is a reduction in cell voltage after WL closes?
Experiment
MIM Cap v/s Trench

- Stack capacitor requires more complex process
- M1 height above gate is increased with stacked capacitor
  - M1 parasitics significantly change when wafer is processed w/o eDRAM
  - Drives unique timings for circuit blocks processed w/ and w/o eDRAM
- Logic Equivalency is compromised – **Trench is Better Choice**
Classical DRAM Organization

- RAM Cell Array
  - Each intersection represents a 1-T DRAM Cell
- Column Selector & I/O Circuits
  - word (row) select
  - bit (data) lines
- Row Decoder
  - row address
- Column Address
  - data

CMOS VLSI design - PEARSON
FIGURE 12.43 DRAM subarray
Trench cell layout and cross-section
In a certain eDRAM process VDD=800mV and the pass transistor has a nominal VTH of 200mV with the worst case VTH variation 50mV. VPP should be

- [ ] At least 800mV
- [ ] At least 1050 mV
- [ ] At most 550 mV
- [ ] At most 1050 mV
References so far


DRAM Read, Write and Refresh

- **Write:**
  1. Drive bit line
  2. Select row

- **Read:**
  1. Precharge bit line
  2. Select row
  3. Cell and bit line share charges
    - Signal developed on bitline
  4. Sense the data
  5. Write back: restore the value

- **Refresh**
  1. Just do a dummy read to every cell & auto write-back
Cell transfer ratio

Uncharged

Charged

$C_{BL}$

$C_{CELL}$

$V_{INITIAL}$

$V_{FINAL}$
Cell Charge Transfer

\[
\Delta V = (V_{bl} - V_{cell}) \left[ \frac{C_{cell}}{C_{bl} + C_{cell}} \right]
\]

Transfer ratio
Bits per Bit-Line v/s Transfer Ratio

TR = Transfer Ratio = \( \frac{C_{cell}}{C_{cell}+C_{bl}} \)

1. 2x Faster Charge Transfer (90%)
   \( t = 2.3 \cdot R_{dev} \cdot (C_{bl} \cdot C_{cell}) / (C_{bl} + C_{cell}) \)

2. 2.3x More Signal

3. 10% More Write Back
Array Segmentation Refers to WL / BL Count per Sub-Array

**Longer Word-Line (More Bit-Lines per Word-Line)**
- Slower but more area efficient – Less Decoders and drivers

**Longer Bit-Line (more Word-Lines per Bit-Line)**
- Less Signal (Higher Bit-Line Capacitance = Lower Transfer Ratio)
- More Power (Bit-Line CV is Significant Component of DRAM Power)
- Slower Performance (Higher Bit-Line Capacitance = Slower Sense Amp)
- More Area Efficient (Fewer Sense Amps)

**Number of WLs Activated determines Refresh Interval and Power**
- All Cells on Active Word-Line are Refreshed
- All Word-Lines must be Refreshed before Cell Retention Expires
- 64ms Cell Retention / 8K Word Lines = 7.8us between refresh cycles
- Activating 2 Word-Lines at a time = 15.6us, 2x Bit-Line CV Power
Depending on signal developed SA architecture is chosen

**Direct sensing**
- Requires large signal development
- An inverter can be used for sensing
- Micro sense amp (uSA) is another option

**Differential sense amp**
- Can sense low signal developed

This is choice between area, speed/performance
The diffusion capacitance of the pass transistor is 100 aF. If metal capacitance is negligible, in order to achieve a transfer ratio of at least 0.7 with 33 cells connected to a BL, the cell capacitance should be

- [ ] At least 7.7 fF
- [ ] At least 7.7 pF
- [ ] At most 7.7 fF
- [ ] At most 7.7 pF
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DRAM Operation Details (Case Study)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier (John Barth/IBM)
Micro Sense Architecture

- Hierarchical Direct Sense
- Short Local Bit-Line (LBL)
  - 33 Cells per LBL
- 8 Micro Sense Amps (µSA) per Global Sense Amp (GSA)
- Write Bit-Line (WBL)
  Uni-Directional
- Read Bit-Line (RBL)
  Bi-Directional
Micro Sense Hierarchy – Three levels

- GSA
- µSA

Data Sense Amp (DSA)

- Local Data (M2)
- Global Data (M4)

Global Bit (M2)

JSSC11
3T uSA operation

**Pre-charge**
WL is low. WBL and RBL both pre-charged to HIGH. Next GSA drives WBL low. **LBL floats to GND level**

**Read “0”**
LBL remains LOW. RBL is HIGH. Sensed as a “0”

**Read “1”**
LBL is HIGH. Turns on RH, pulls RBL LOW. + feedback as pFET FB turns ON. Sensed as a “1”

**Write “1”**
GSA pulls RBL to GND. FB pFET turns ON
Happens while WL rises (direct write)

**Write “0”**
WBL is HIGH, PCW0 ON. Clamps LBL to GND
As WL activates.
Micro Sense Amp Simulations

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 1, JANUARY 2008

A 500 MHz Random Cycle, 1.5 ns Latency, SOI Embedded DRAM Macro Featuring a Three-Transistor Micro Sense Amplifier
Layout Floor plan of Array+SA

GSA Should fit into the bitcell width or n*bitcell width
Thus, distributed GSA on two sides of bitcell array
Column Interleave

- 1 of 8 Column Select Lines (CSL)
- Fire Early for Write
- Fire Late to Support Concurrent Cache Directory Lookup
Q6. In a 3T micro sense amp, sensing a one is controlled is directly controlled by the trip point of

- NFET RH
- Pre-charge NFET (PC)
- Pull up PFET (FB)
- Pass transistor of the cell being read
Q7. The problem with the 3T micro sense family is that

- It is slow to sense a ZERO
- It cannot accommodate more than 33 cells per LBL
- It consumes too much dynamic and leakage power
- It is too slow to sense a ONE
LAYOUT of array

WL POLY

WL M3

WL POLY

WL M3

RBL0
LBL0
WBL0
RBL1
LBL0
WBL1
Single Ended Sense – Twist not effective
Line to Line Coupling must be managed
Q2. In a 3T micro sense amp, in stand by mode, the following leakage current is a serious concern

- Through PCW0
- Through RH
- Through FB
- Stand by leakage is not a concern
Micro Sense Coupling Mechanisms

1. Write ‘1’ Couples **WBL** below Ground Increasing RH leakage during Refresh ‘0’
2. Write ‘0’ Couples **RBL** above VDD Delaying Feedback during Refresh ‘1’
3. Read ‘1’ Couples Half-Selected LBL Below GND Increasing Array Device Sub-VT Leakage
Micro Sense Evolution

1. Write Zero (W0)
2. Read Head (RH)
3. Feed-Back (FB)
4. PFET Header (PH)
   - LBL Power Gate
   - LBL Leakage
5. Pre-Charge (PC)
   - WBL Power (Write ‘0’ Only)
6. NFET Footer (NF)
   - RBL Leakage
   - Decompose Pre-Charge and Read Enable (MWL_RE)

Power Reduction
Traded for Transistor Count

Increased Transistor Count

Barth, ISSCC’07
Klim, VLSI’07
JSSC11
Micro Sense Architecture (µSA)

3 Transistors

LBL(M1)

Cell(20fF)

Local BL 32 Cells

Global BL 8 µSA

Secondary Sense Amp

Sett

Seqn

Ldlc

Ldlt

Lbll(M1)

WBL(M2)

RBL(M2)

WBL(12fF)

RBL(12fF)

32 Cells

Cell(20fF)

µSA

Global BL 8 µSA

Local BL 32 Cells

Micro Sense

WBL(M2)

RBL(M2)

WBL(12fF)

RBL(12fF)
Data Sense Amp (DSA)

- LDC LDT (Local Data to/from GSA)
- WDT/WDC Driven from Lower Voltage Domain
- P0/P1 Provide Improved Voltage Level Shifting
- RDC (Read Data)

WDC (Write 0)
WDT (Write 1)
ENABLE
Micro Sense Advantage

Fast Performance of Short Bit-Line
Area Overhead of 4x Longer Bit-Line

<table>
<thead>
<tr>
<th>Bits/BL</th>
<th>256</th>
<th>128</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sense Amp</td>
<td>10%</td>
<td>20%</td>
<td>19%</td>
</tr>
<tr>
<td>Reference Cells</td>
<td>2.3%</td>
<td>4%</td>
<td>-</td>
</tr>
<tr>
<td>Twist Region</td>
<td>2%</td>
<td>2.6%</td>
<td>-</td>
</tr>
<tr>
<td>Second Sense Amp</td>
<td>-</td>
<td>-</td>
<td>8%</td>
</tr>
<tr>
<td>Total</td>
<td>14.3%</td>
<td>26.6%</td>
<td>27%</td>
</tr>
</tbody>
</table>

Same Overhead
Array utilization

Utilization = \frac{\text{Cell Area}}{\text{Mbits/mm}^2}

Cell Area

W

L

D

S

A

IO + Predecode + Redundancy
Access Shmoo

1.5ns Access @1V 85C

4ns Access @600mV
Redundancy

Notebook

Page 111

Extra Page R05

eFuse based repair table

(see page R05)
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- Noise concerns
- Wordline driver (WLDRV) and level translators (LT)
- Challenges in eDRAM
- Understanding Timing diagram – An example
Noise

coupling and Local Process Variation effectively degrades signal

External Noise (Wire or Sx) Reduced to Common Mode by Folding

Line to Line Coupling Limited by Bit-Line Twisting

$V_t$ and Mis-Match Limited by Longer Channel Length

Overlay Mis-Alignment Limited by Identical Orientation

Capacitive Mis-Match Limited by careful Physical Design (Symmetry)
Interleaved Sense Amp w/ Bit-Line Twist

Local Array

1 of 8 Column Decode

Column Decode

Data Bit 0
Data Bit N
Data Bit 127

Write Local Read

CMOS VLSI design - PEARSON
Open and Folded Bitline Schematic
Folded Bitline Layout

FIGURE 12.46 Layout of folded bitline subarray
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Retention

Transfer Device and Storage Cap are NOT ideal devices: they LEAK
Leakage Mechanisms include: Ioff, Junction Leakage, GIDL,…
Junction Leakage Temperature Dependence = 2x/10°C

Cell Charge needs to be replenished (Refreshed),
Median Retention Time:

\[ T = C \Delta V = 35 \text{fF} \times 400 \text{mV} = 7 \text{ seconds} \]

Where \( \Delta V \) is acceptable loss
C is Cell Capacitance
\( I_{\text{leak}} \) is Total Leakage

Retention Distribution has Tails
created by Defects and Leaky Cells

Weak Cells Tested out (5x Guardband)
and replaced with Redundancy

Customer issues periodic Refresh Cycle
Pass transistor leakage

$V_{DS} = 1V$

$I_{ON}$

$I_{OFF}$

$V_{GS} = 0V$

$I_D (\log)$

DIBL

GIDL
Floating Body Effects

Body potential modulated by coupling and leakage

During write back, body voltage increases
⇒ Threshold voltage decreases ⇒ Better WRITE 1

Degraded $I_{\text{off}}$ / Retention if body floats high (body leakage)
⇒ GND pre-charge keeps body low
⇒ Eliminate long periods with BL high (limit page mode)

$\text{IL}_{\text{FWD}} > \text{IL}_{\text{REV}}$

When BL = GND
Body ⇒ GND

1Volt

JSSC08
Array Body Charging

Commodity DRAM (long page mode)

Bit-Line

Net Body Charge from Leakage

µs

embedded DRAM (limited page mode)

Bit-Line

Net Body Charge from Leakage

ns

High Cell Leakage Period

JSSC08
eDRAM vs. SRAM Cycle-Time Comparison

1. WL Activation
2. Charge Transfer to Bit-Line
   \(I_{READ}\) Similar to SRAM
3. Amplification
4. Write-Back
5. Precharge

NET: SRAM Random Cycle will continue to lead!
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- Gated Feedback Sense Amplifier
- Challenges in eDRAM
- Understanding Timing diagram – An example
Gated Feedback Sense Amp
Q3. The logic one voltage level of BLMUX in a Gated Feedback Sense Amp (GSA) should be

- [ ] VDD
- [ ] VPP
- [ ] At least VDD + VT
- [ ] At most VPP - VT
Q4. SETPn and SETP are respectively used in a GSA to

- Prevent early feedback and reduce leakage
- Reduce leakage and prevent early feedback
- Reduce leakage
- Prevent early feedback
Q5. With regard to multiplexing BLs and sharing GSAs which of the following is true?

- Like in SRAM LBLs can be column multiplexed and shared with a GSA if the GSA is large enough
- Column multiplexing LBLs with the GSA saves area but is a minor advantage
- Depends on the layout symmetry
- Each LBL should necessarily be connected to a GSA
Q6. In a particular lot, the NFET is much slower and the PFET is much faster than expected. This will cause

- Read 0 to be slower
- Read 1 to be slower
- Read 0 to be faster
- Read 1 to be faster
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WLDRV

Driver with Low voltage transistors → Logic transistors
No thick gate oxide transistors required!!
Voltage across any two terminals should not exceed reliability limits

1. US patent No: 8,120,968 → William Robert Reohr, John E Barth
LEVEL Shifter

VWL Level shifter

VPP Level shifter

1. US patent No: 8,120,968 — William Robert Reohr, John E Barth
2. A Low Voltage to High Voltage Level Shifter Circuit for MEMS Application — Dong Pan
Orthogonal WLD and pyramid wiring (M3/M4)
Q7. Applying a voltage swing of VPP to VWL (~2 V) across a standard NFET is not advisable because

- It can break the device
- Causes the VT of the device to reduce over time
- Causes the VT of the device to increase over time
- It’s maybe a reliability concern depending on where it is placed in the layout
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- Understanding Timing diagram – An example
• Control Signals (RAS_L, CAS_L, WE_L, OE_L) are all active low
• Din and Dout are combined (D):
  – WE_L is asserted (Low), OE_L is disasserted (High)
    • D serves as the data input pin
  – WE_L is disasserted (High), OE_L is asserted (Low)
    • D is the data output pin
• Row and column addresses share the same pins (A)
  – RAS_L goes low: Pins A are latched in as row address
  – CAS_L goes low: Pins A are latched in as column address
  – RAS/CAS edge-sensitive
DRAM logical organization (4 Mbit)

- A0…A10
- Address Buffer
- Row Decoder
- Column Decoder
- Sense Amps & I/O
- Memory Array (2,048 x 2,048)
- Word Line
- Storage Cell

° Square root of bits per RAS/CAS

Din Dout can be clubbed together with a BiDi buffer
DRAM Read Timing

- Every DRAM access begins at:
  - The assertion of the RAS_L
  - 2 ways to read:
    early or late v. CAS

- DRAM Read Cycle Time
- RAS_L
- CAS_L
- Row Address
- Col Address
- Junk
- Row Address
- Col Address
- Junk
- WE_L
- OE_L
- High Z
- Data Out
- Read Access Time
- Output Enable Delay

Early Read Cycle: OE_L asserted before CAS_L
Late Read Cycle: OE_L asserted after CAS_L
DRAM Write Timing

- Every DRAM access begins at:
  - The assertion of the RAS_L
  - 2 ways to write: early or late v. CAS

256K x 8 DRAM

RAS_L  CAS_L  WE_L  OE_L

A → 9 8 → D

DRAM WR Cycle Time

Early Wr Cycle: WE_L asserted before CAS_L
Late Wr Cycle: WE_L asserted after CAS_L

• Every DRAM access begins at:
  - The assertion of the RAS_L
  - 2 ways to write: early or late v. CAS
Conclusion

• Pulling more DRAM cache (L2, L3) inside the processor improves overall performance
• eDRAM design using logic process is a challenge
• Case study is done, covering many of the eDRAM design aspects
References


References


