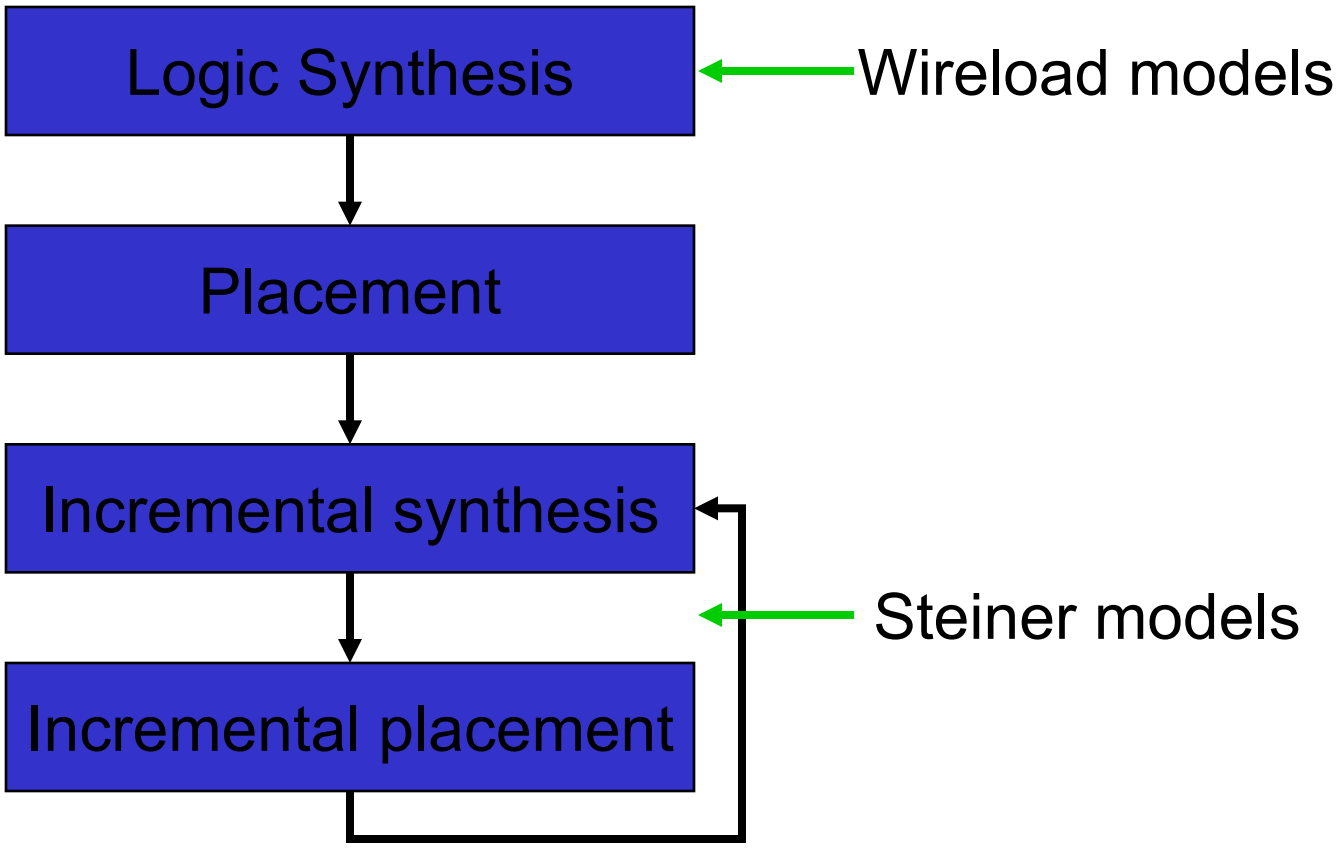
Physical Synthesis

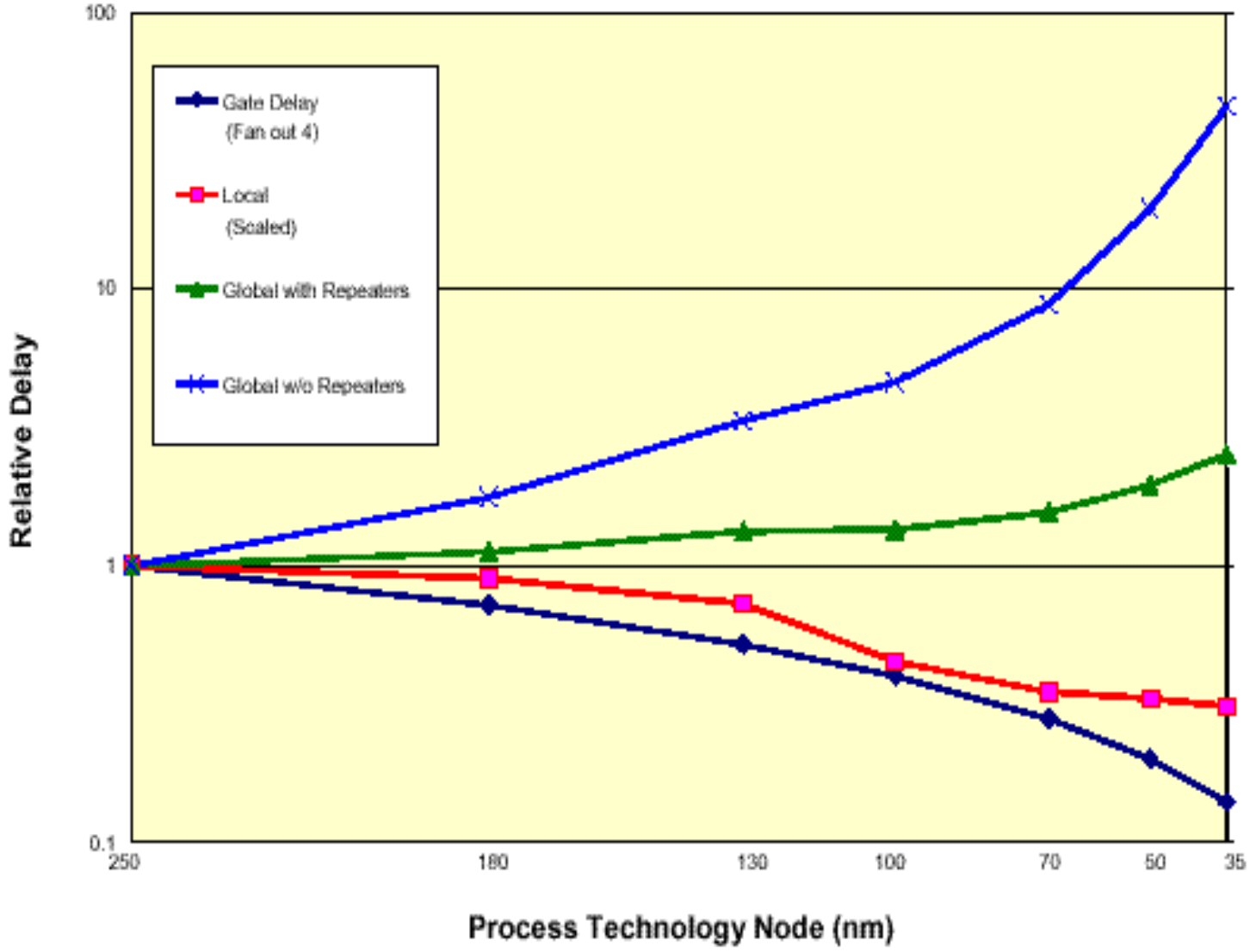
What's Physical Synthesis

- A design satisfies timing constraint after logic synthesis will not necessarily meet timing constraints after P&R due to wire delays
- Physical synthesis has been emerged as a necessary weapon for design closure.
  - Begins with mapped netlist generated by logic synthesis
  - Generates a new optimized netlist and a corresponding layout
  - Objective are combination:
    - Timing, area, power and routability
- Think of this as a wrapper around traditional P&R where synthesis based optimization are interwoven with placement & routing.

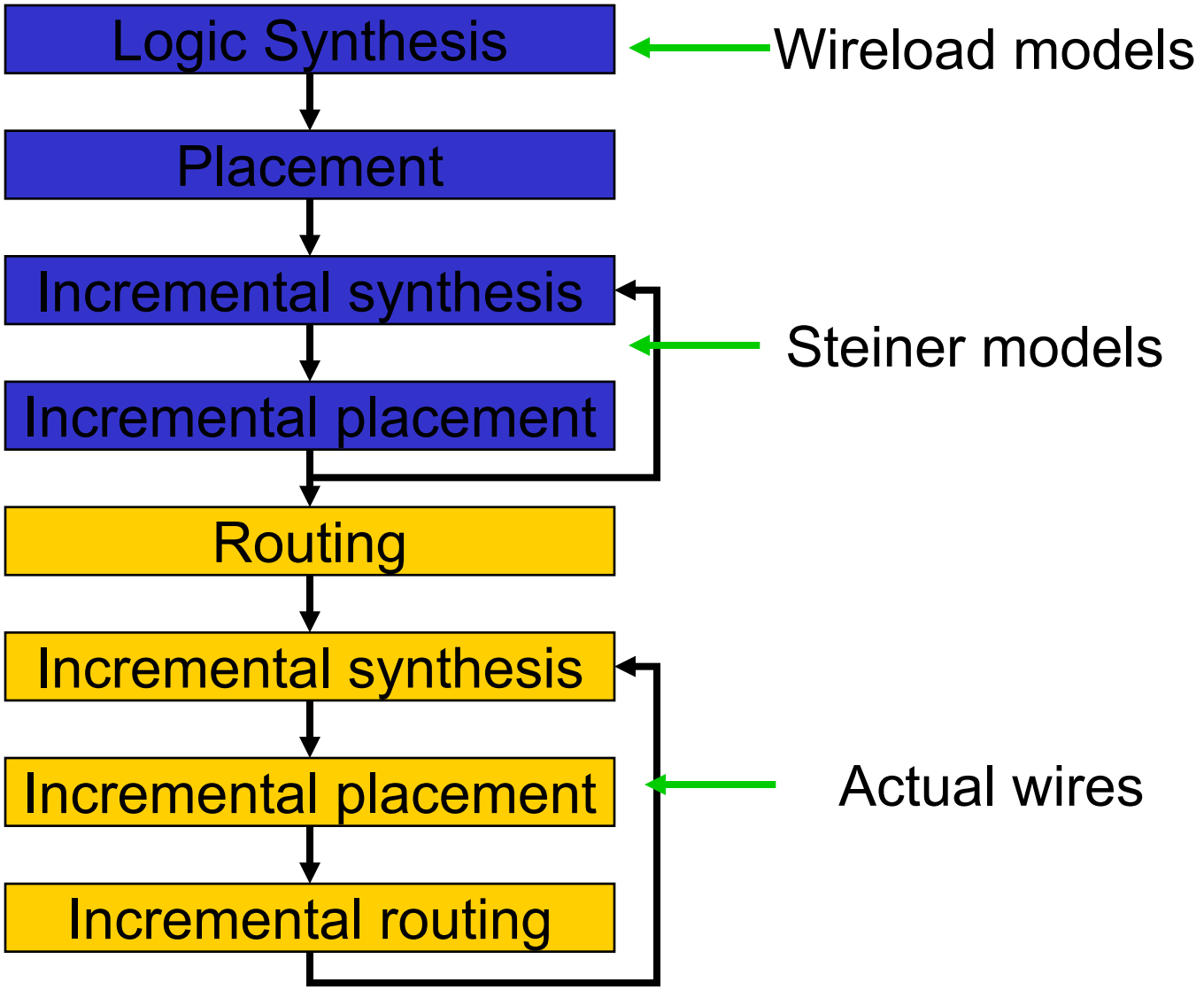
What Does Physical Synthesis Mean?



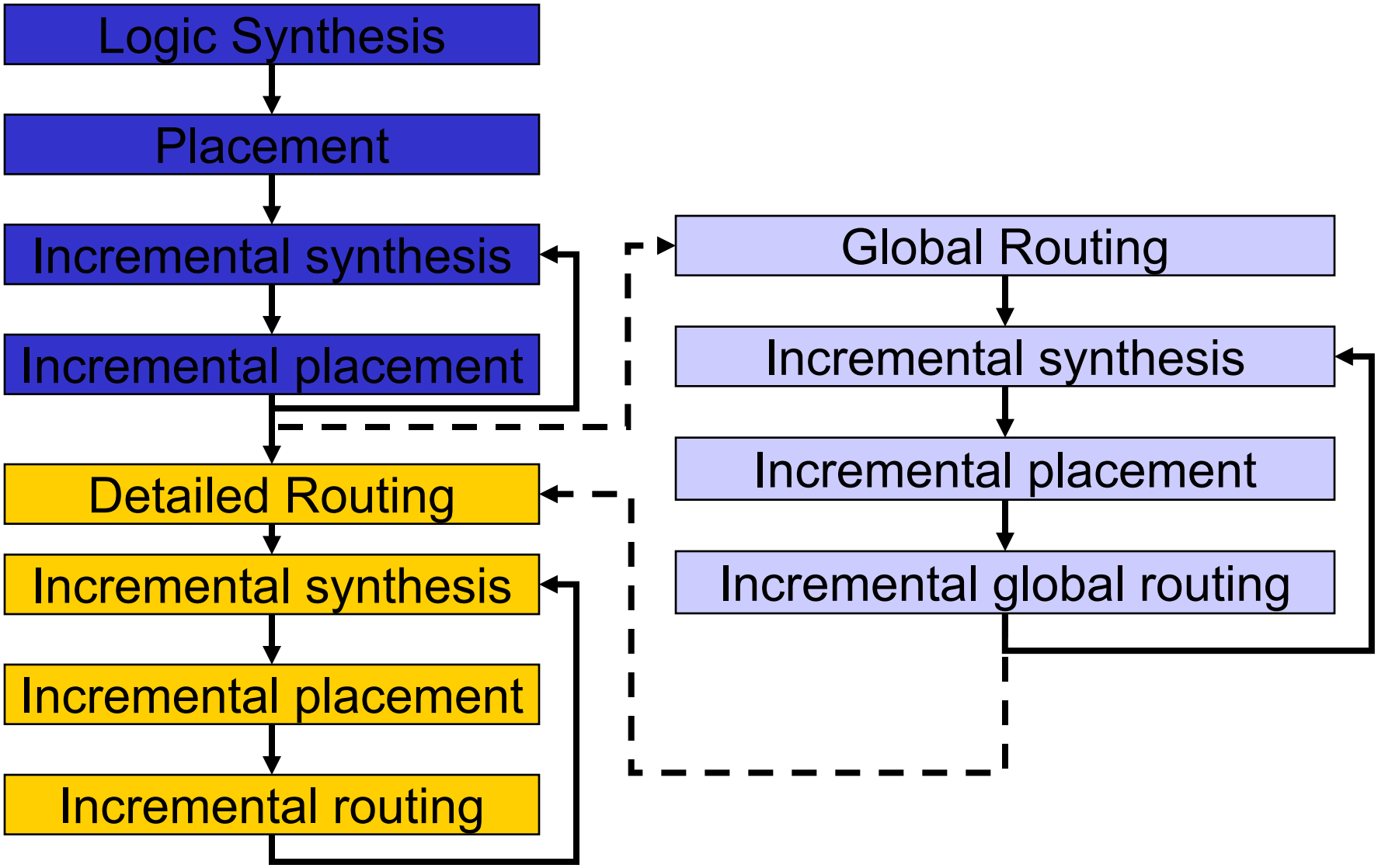
Global Interconnect Dominance



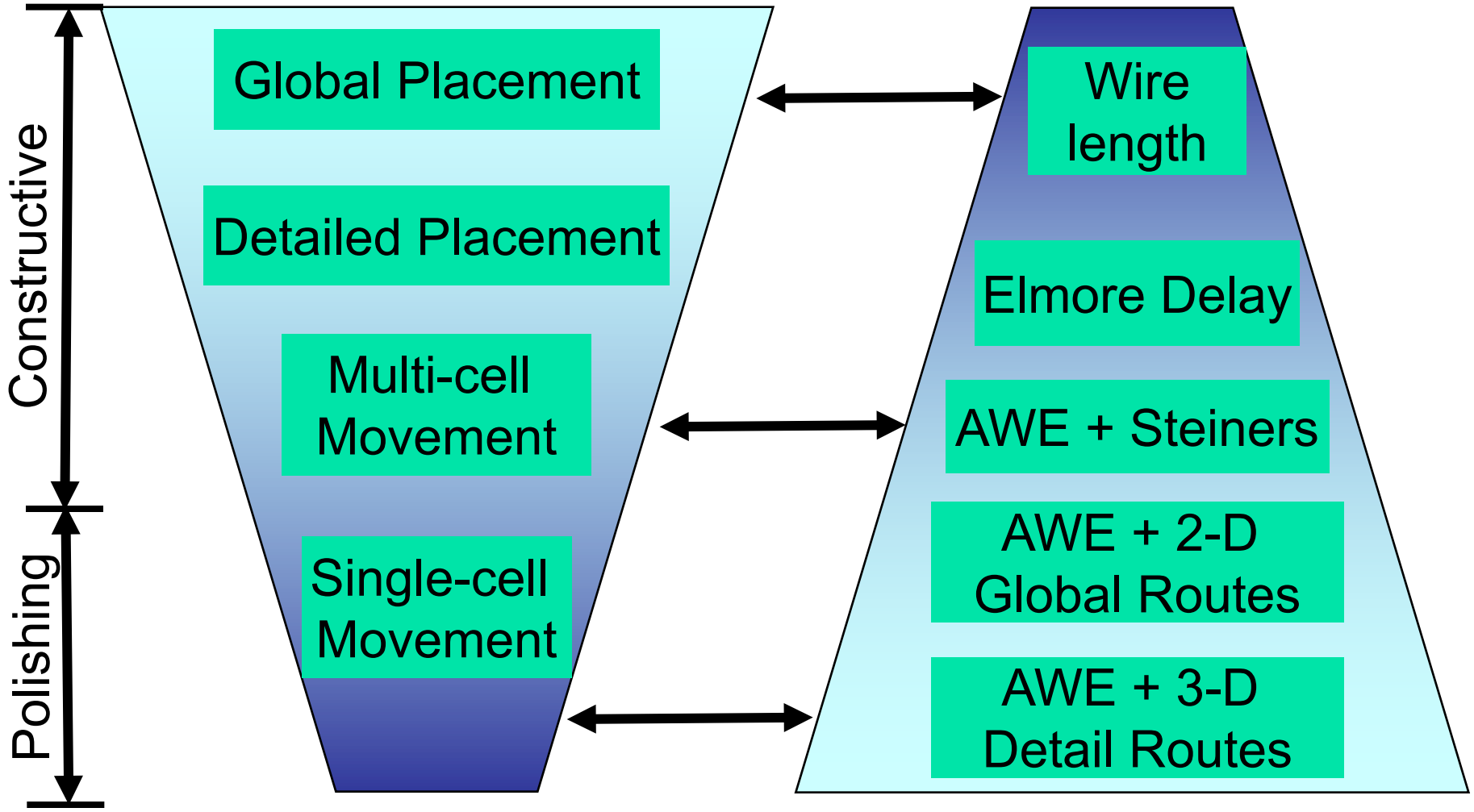
Physical Synthesis with Real Wires



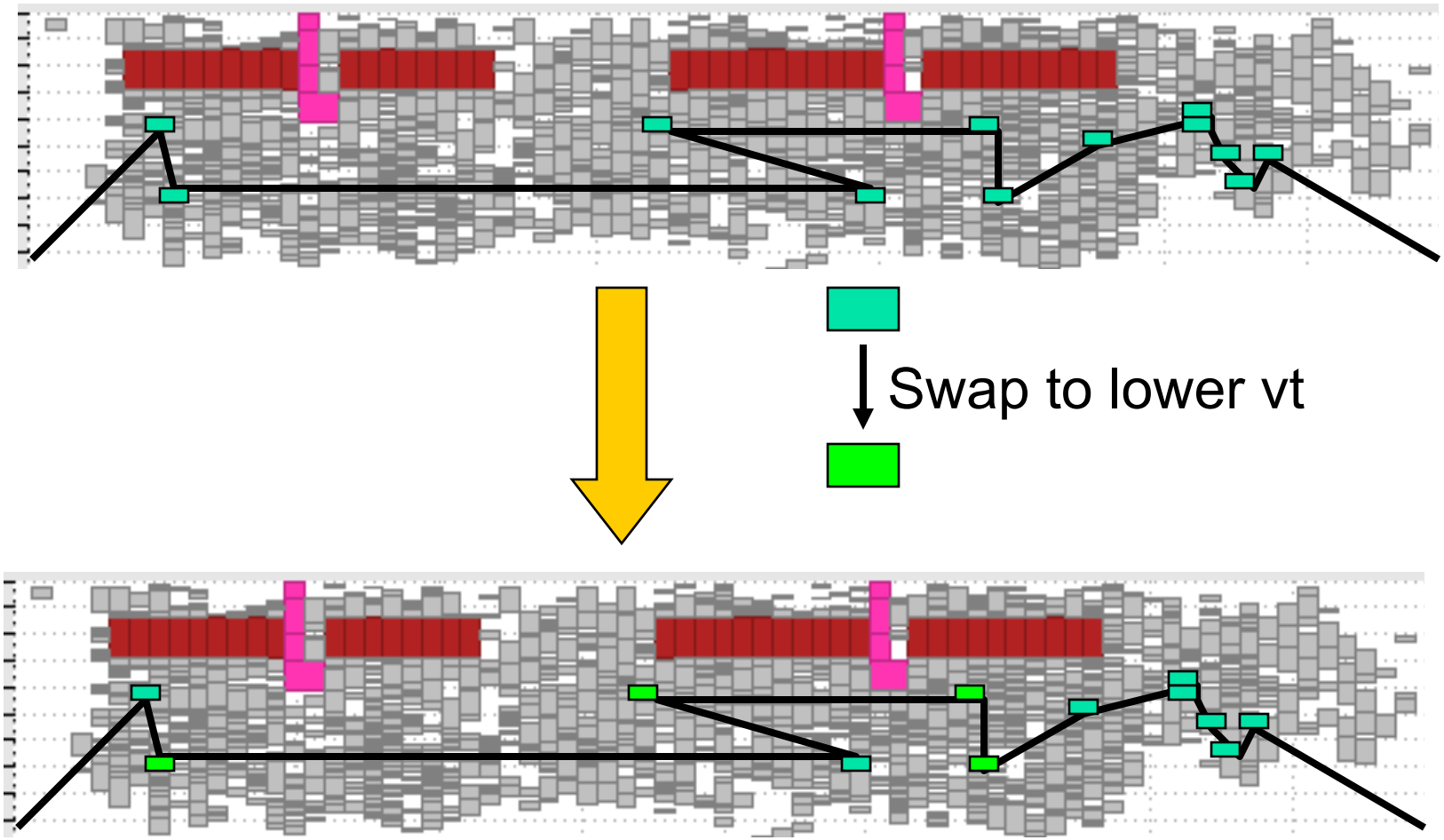
Physical Synthesis with Global Wires



Variable Optimization and Accuracy



What Is Incremental Synthesis?

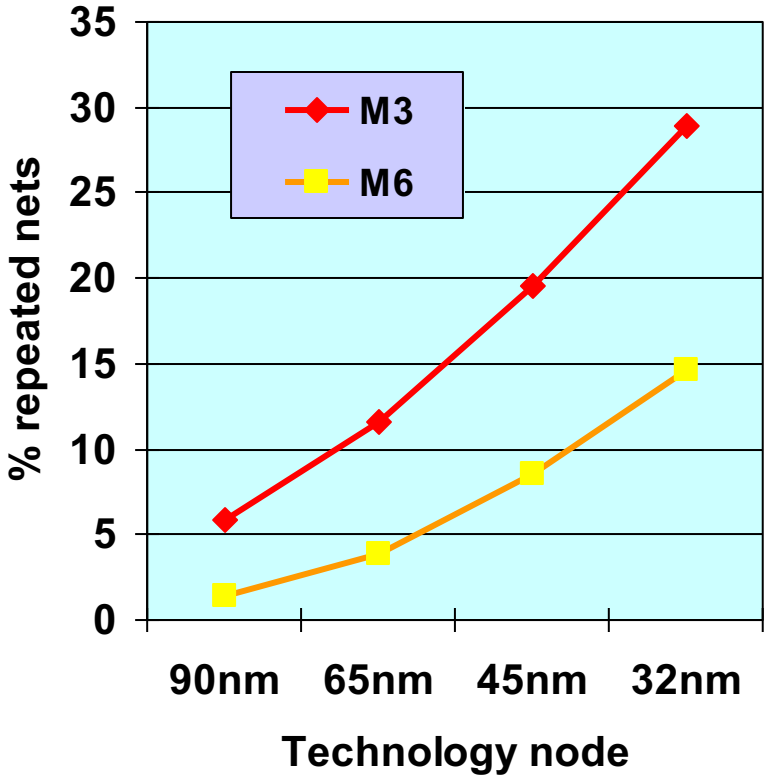


Example Incremental Synthesis Transforms

- Buffering or repeater insertion
- Layer assignment
- Gate sizing or repowering
- Vt swapping
- Cell movement
- Inverter absorption / inverter decomposition
- Cloning
- Inverter / buffer deletion
- Composition / decomposition

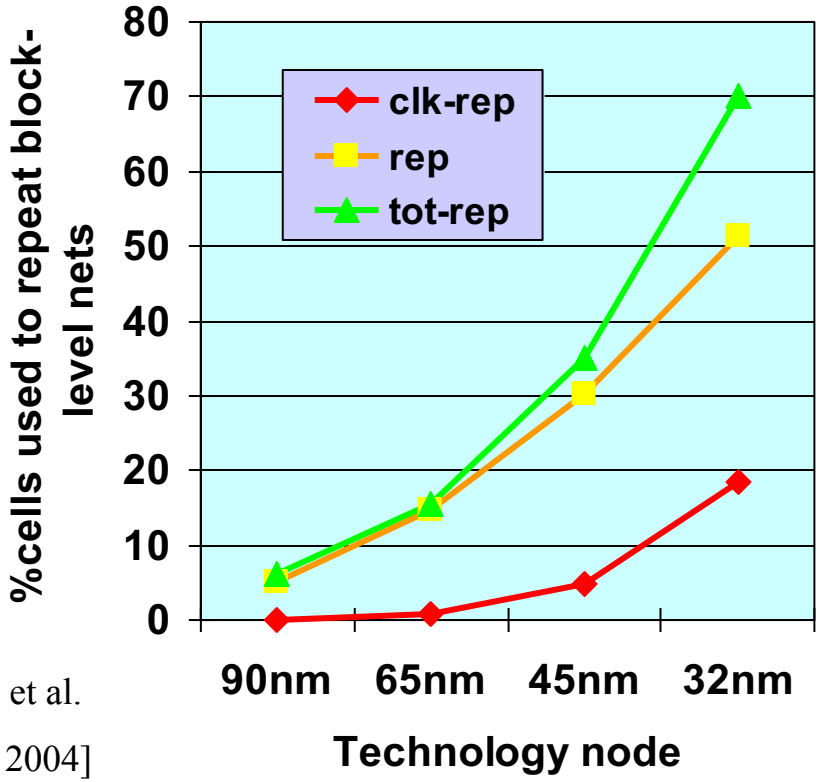
Buffer Insertion

- Buffer insertion and sizing is one of the most effective method for reducing interconnect delay and achieving timing closure.



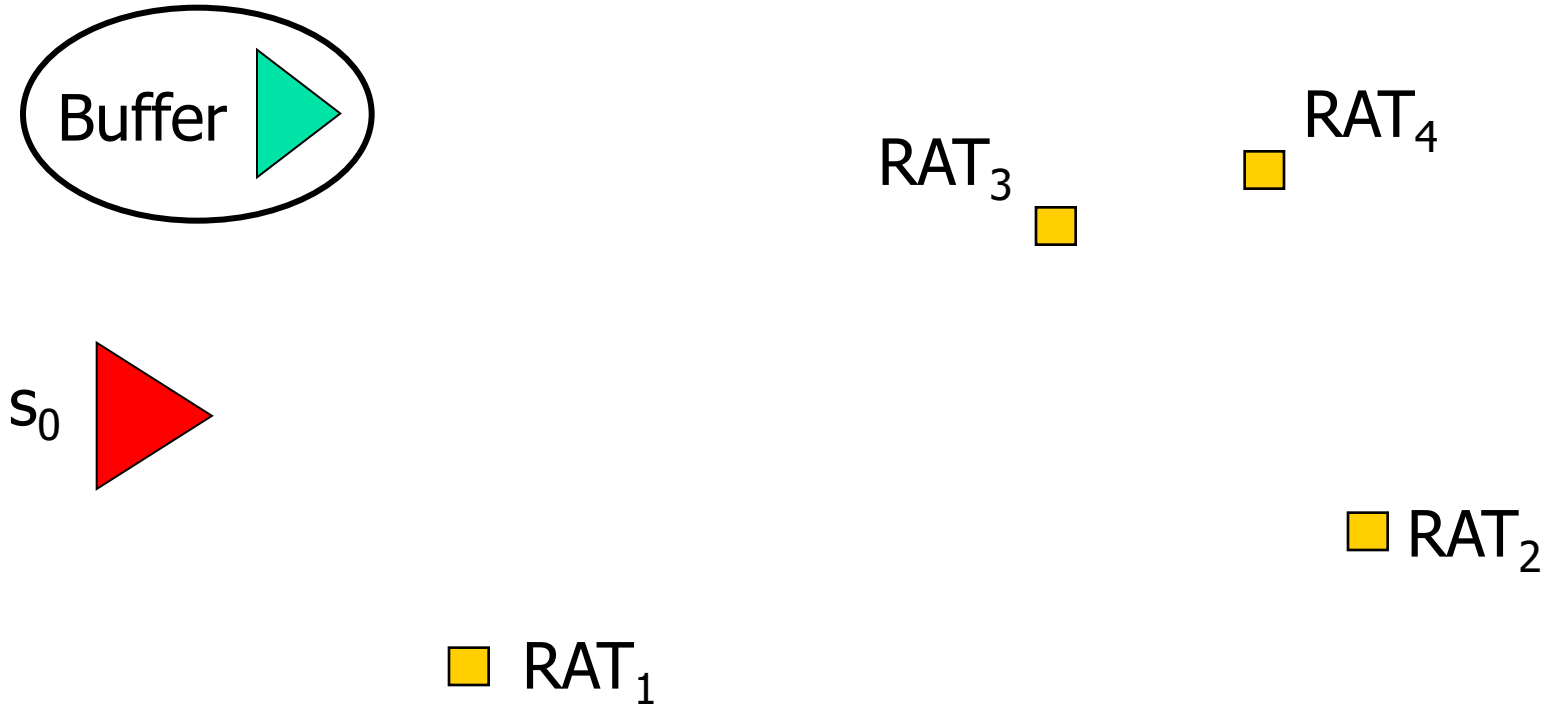
Saxena, et al.

[TCAD 2004]



Simple Buffer Insertion Problem

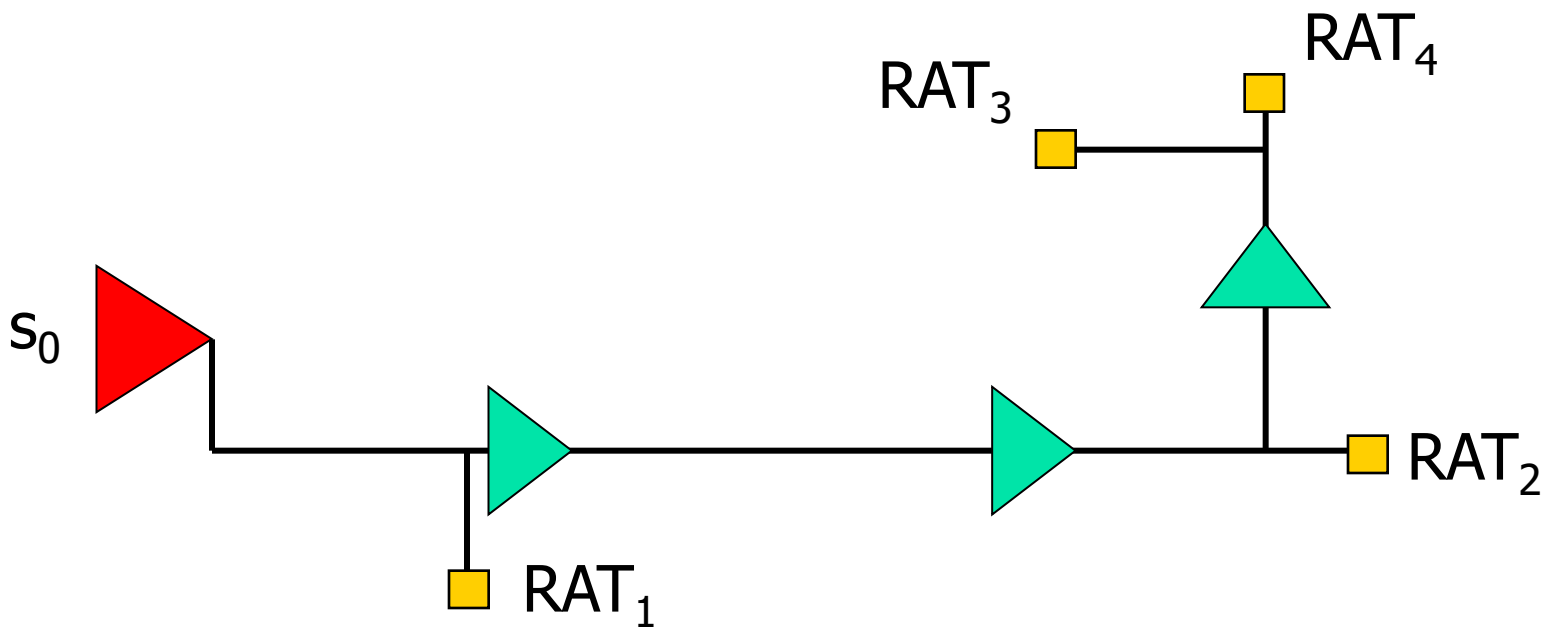
Given: Source and sink locations, sink capacitances and RATs, a buffer type, source delay rules, unit wire resistance and capacitance



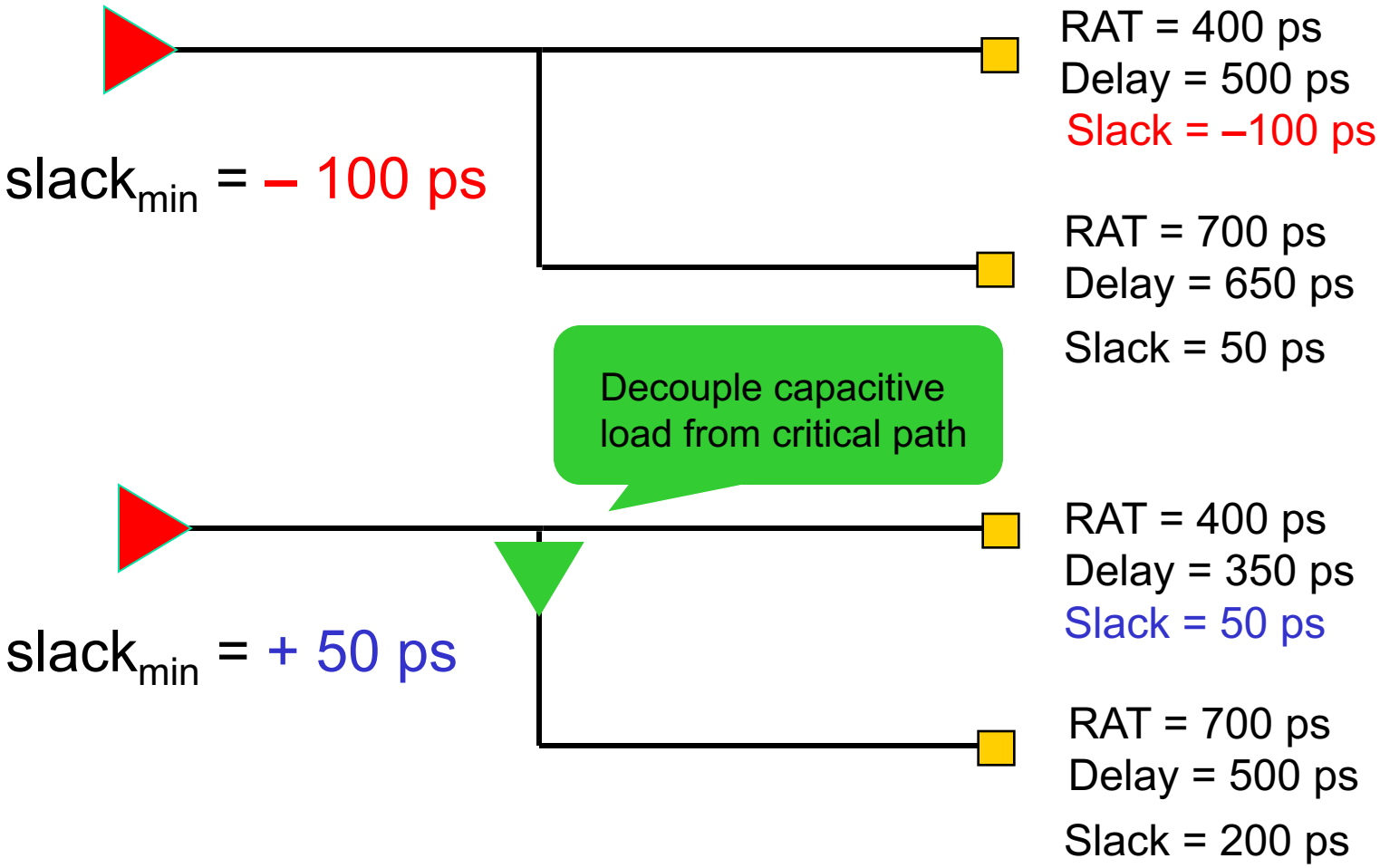
Simple Buffer Insertion Problem

Find: Buffer locations and a routing tree such that slack at the source is minimized

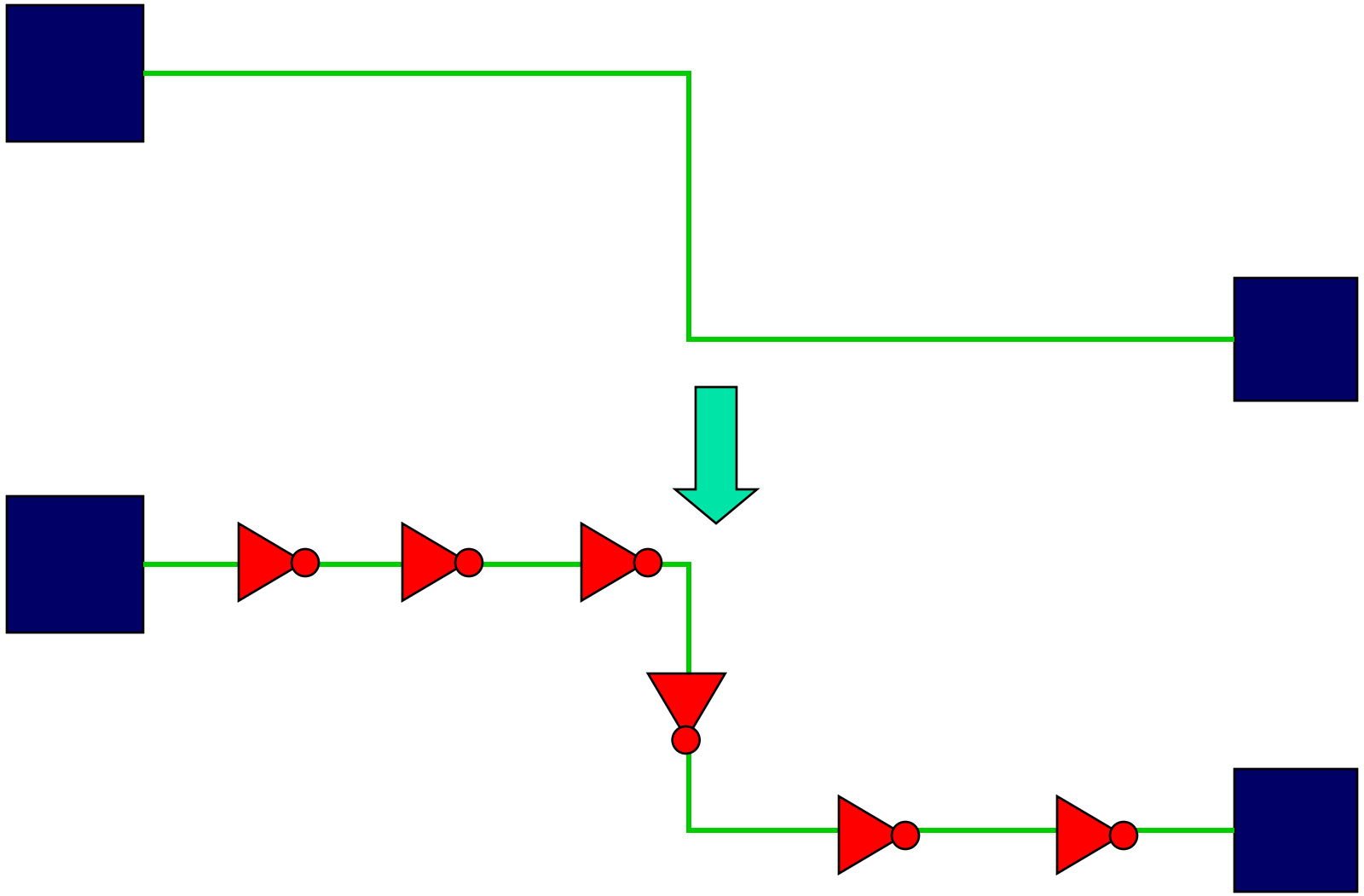
$$q(s_0) = \min_{1 \le i \le 4} \{RAT(s_i) - delay(s_0, s_i)\}$$



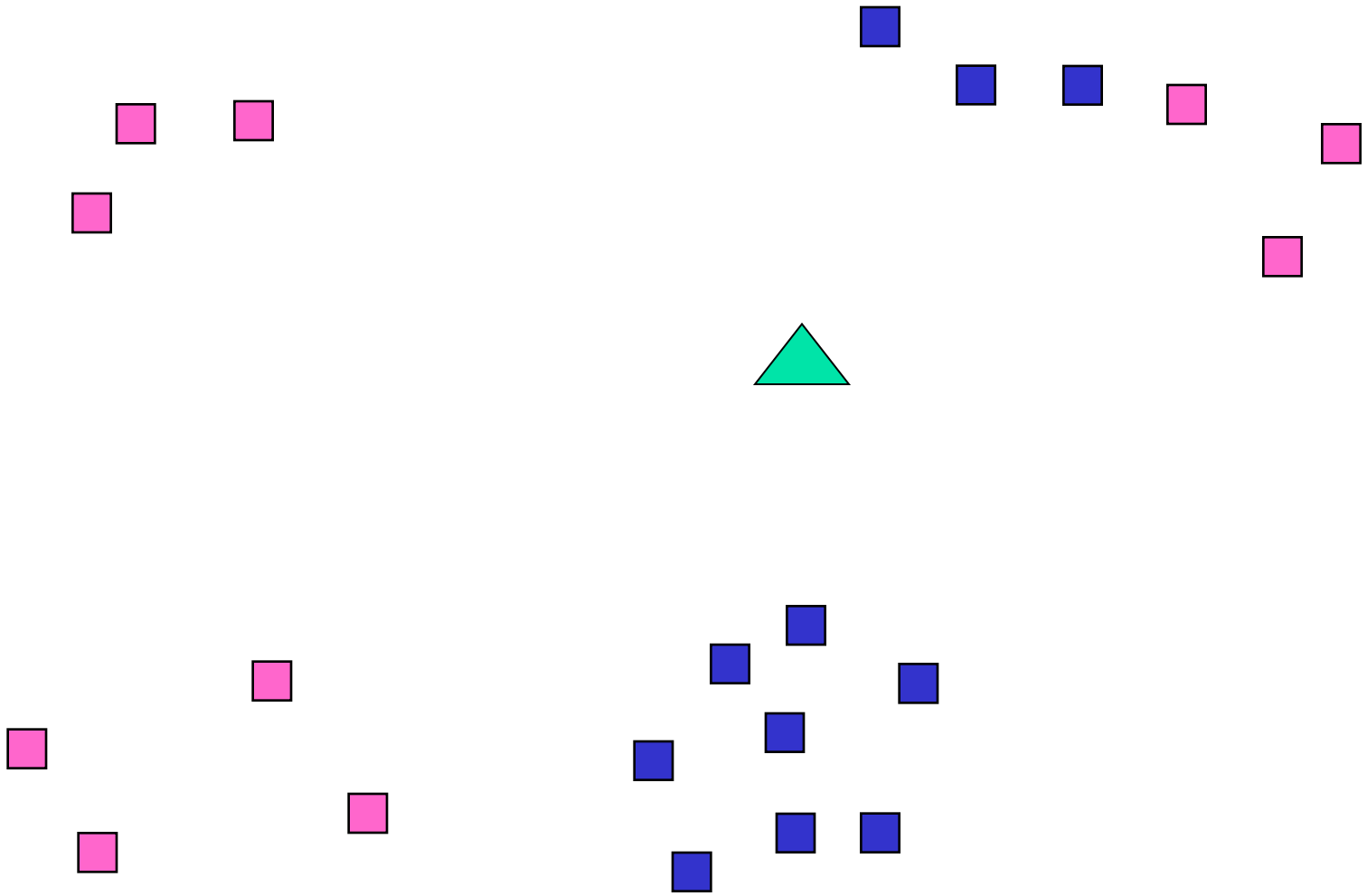
Slack Example



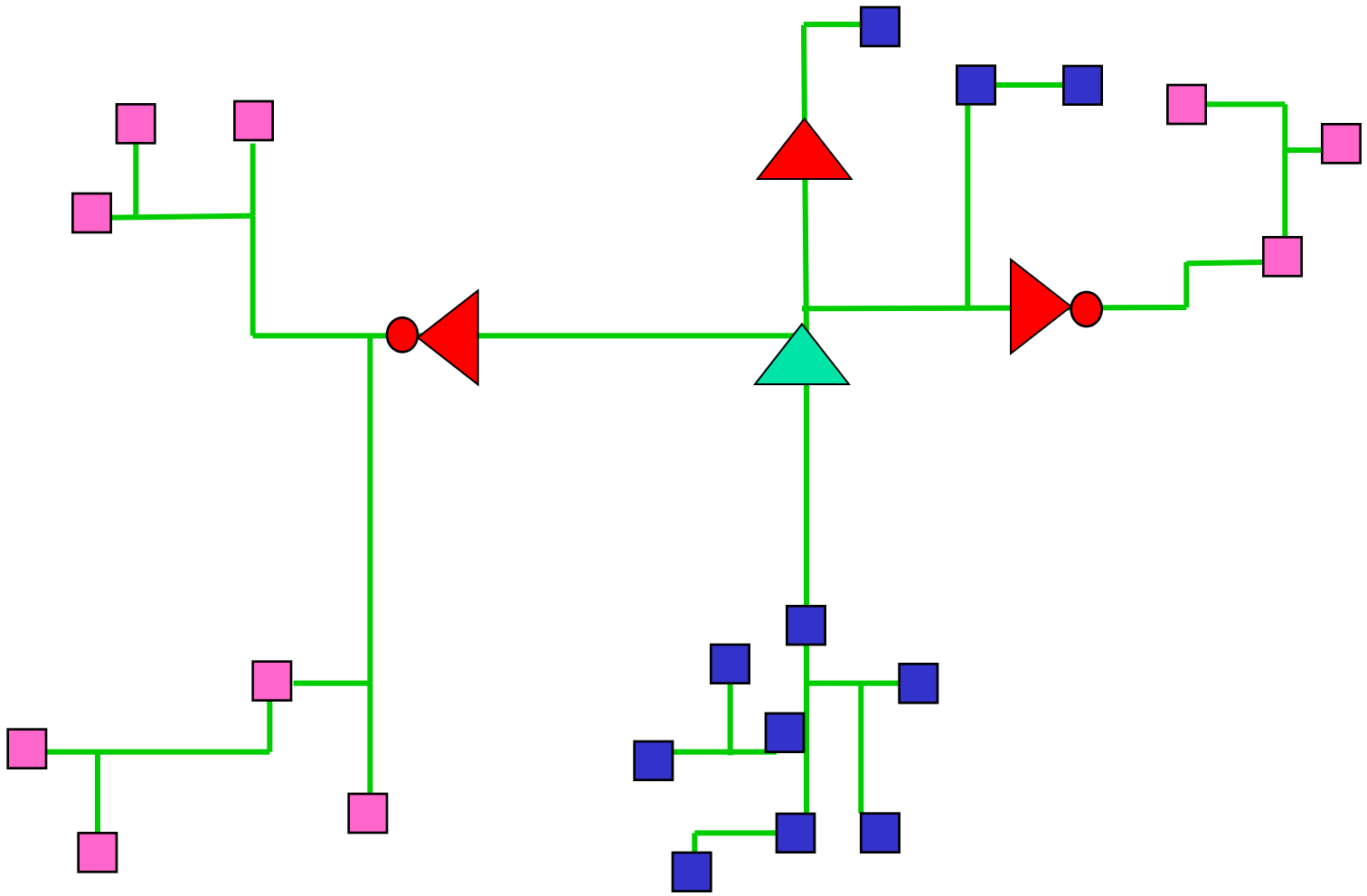
Buffering Long Nets



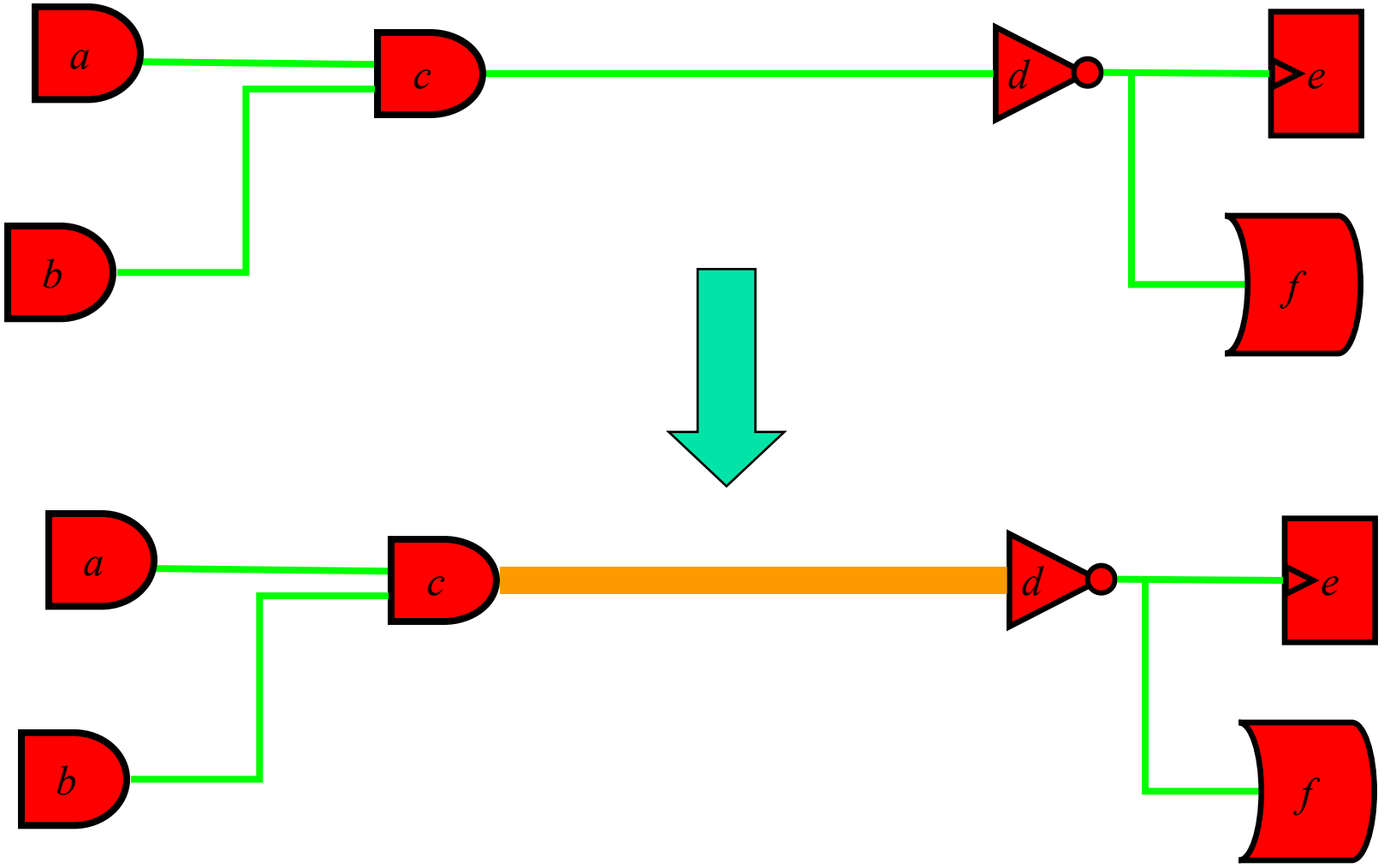
Buffering a Nets to Reduce Fanout (Before)



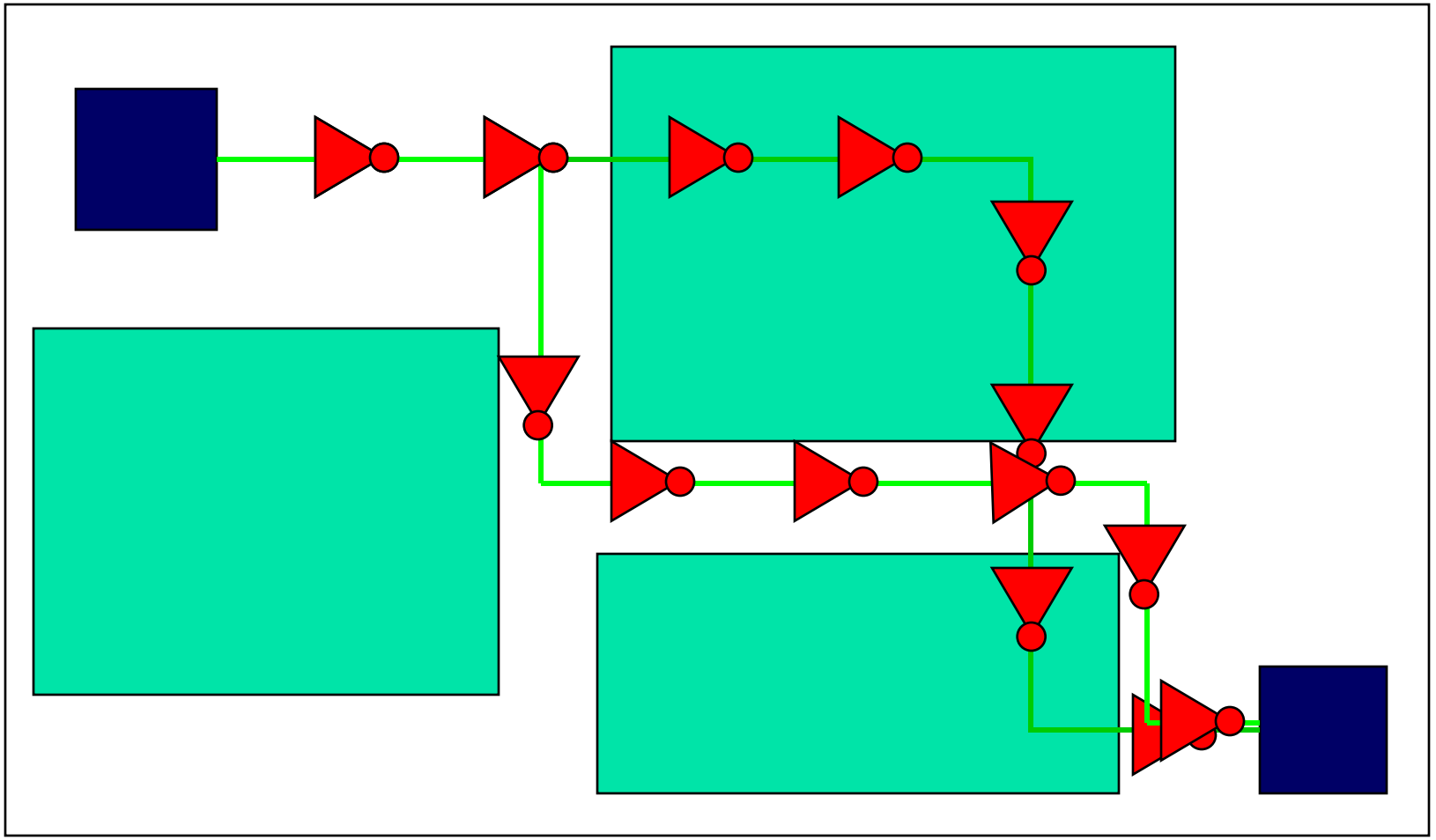
Buffering a Net to Reduce Fanout (After)



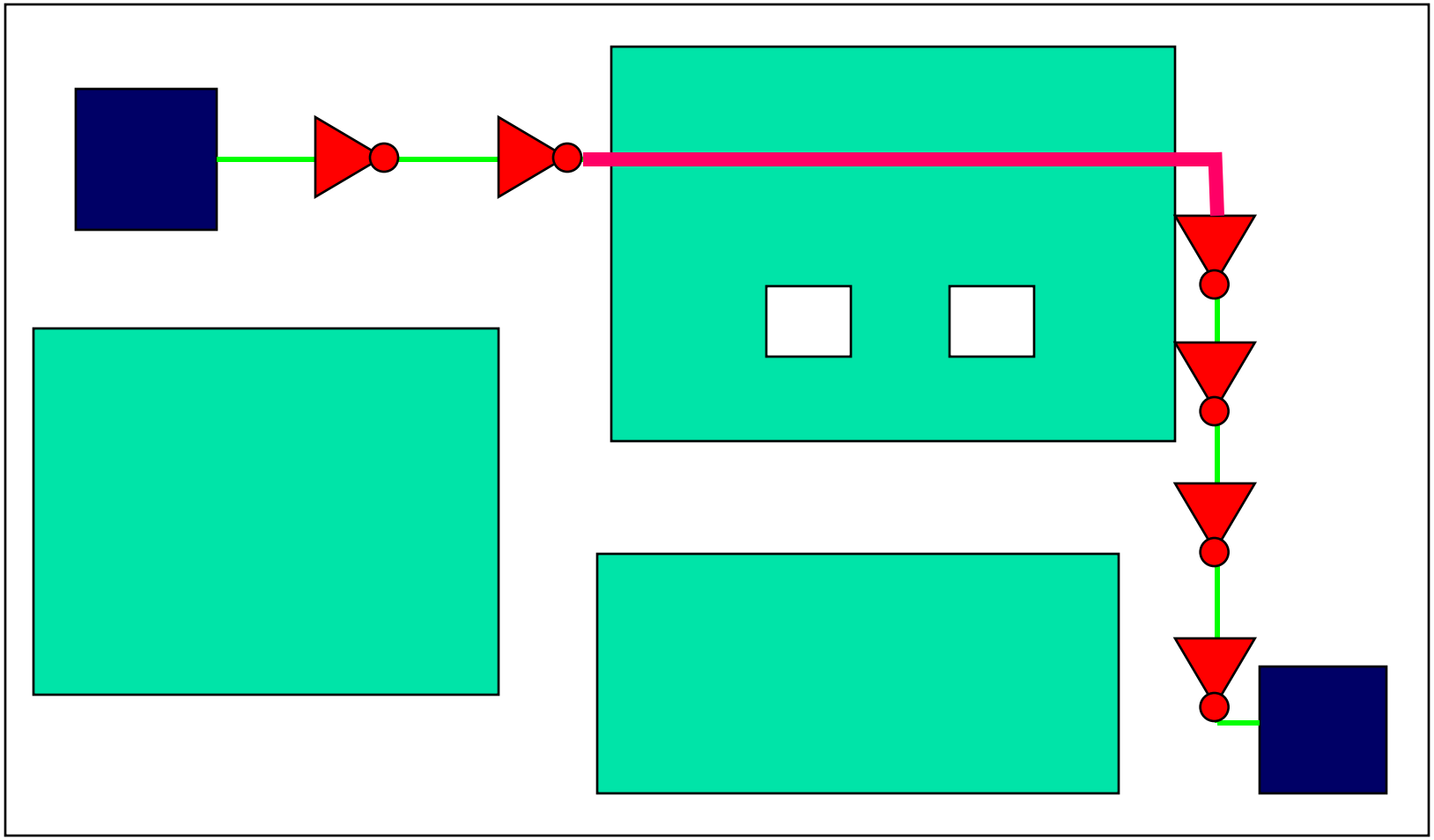
Layer Assignment



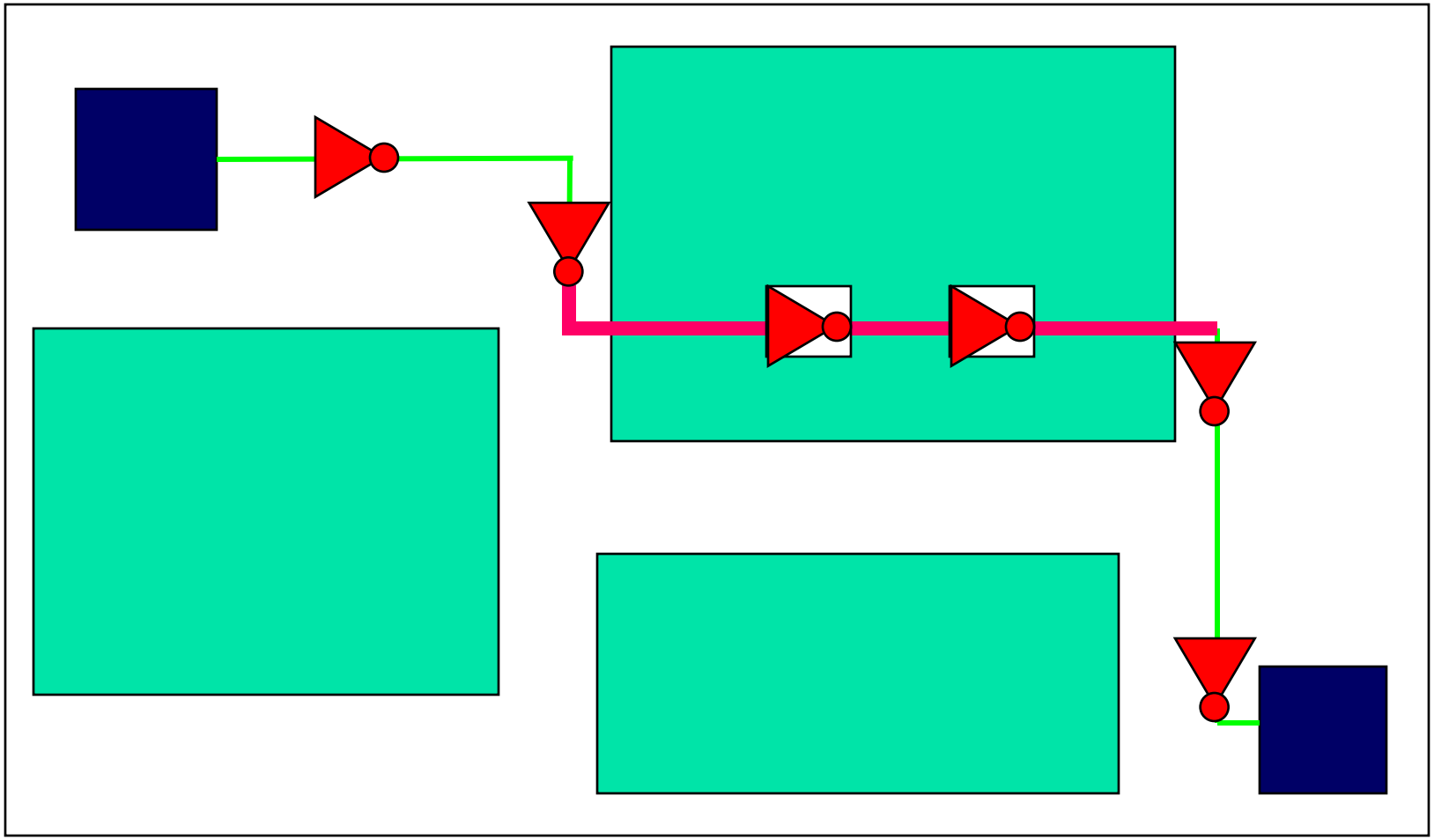
What is Wire (Interconnect) Synthesis?



What Does Wire Synthesis Really Mean?

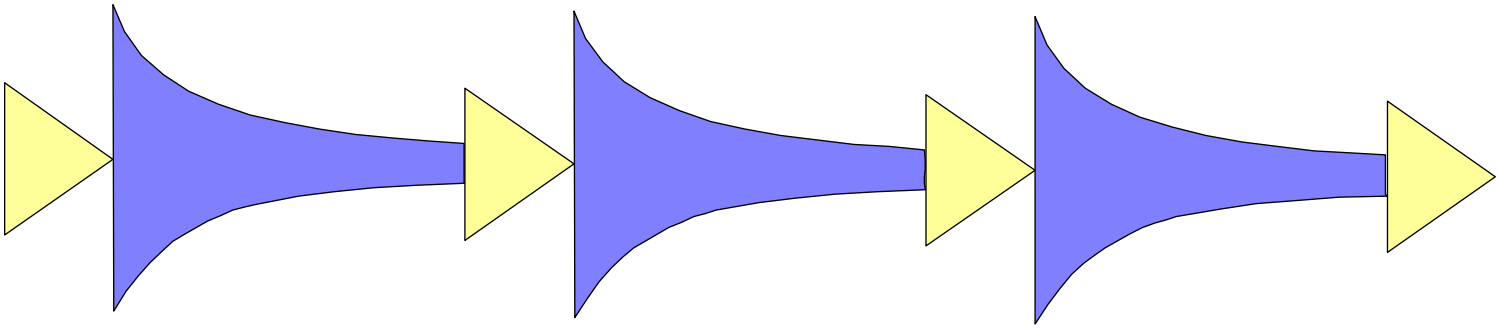


What Does Wire Synthesis Really Mean?

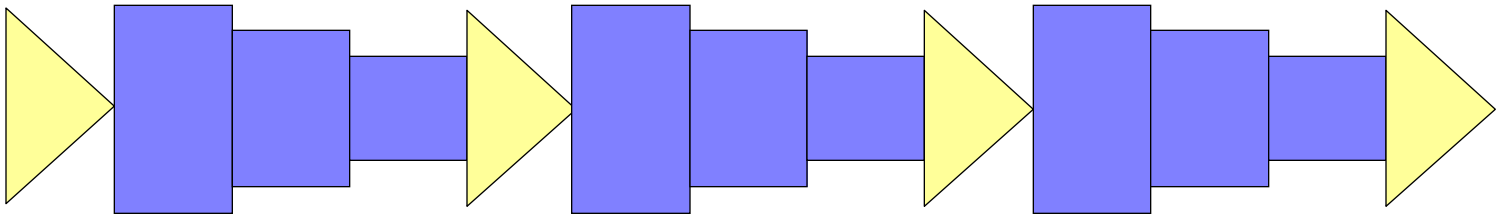


The Academics: Wire Synthesis in the 1990s

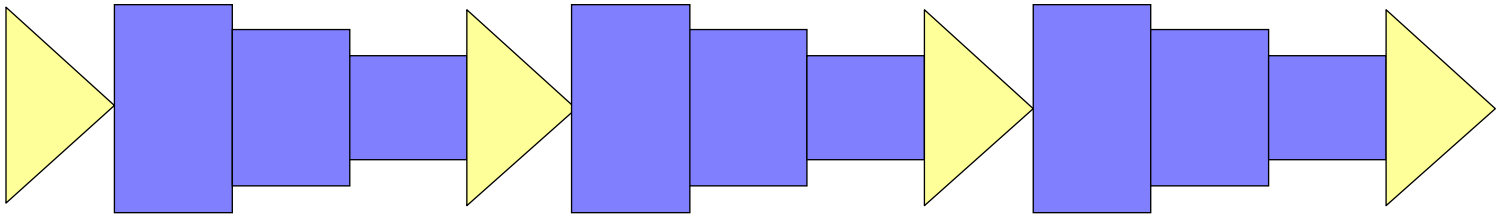
Optimal Wire Shape



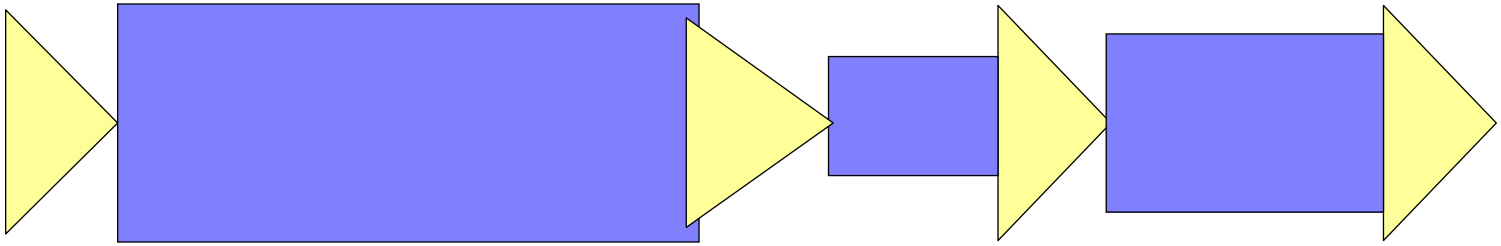
Simultaneous Buffering and Wire Tapering



Was Wire Tapering Worthwhile?

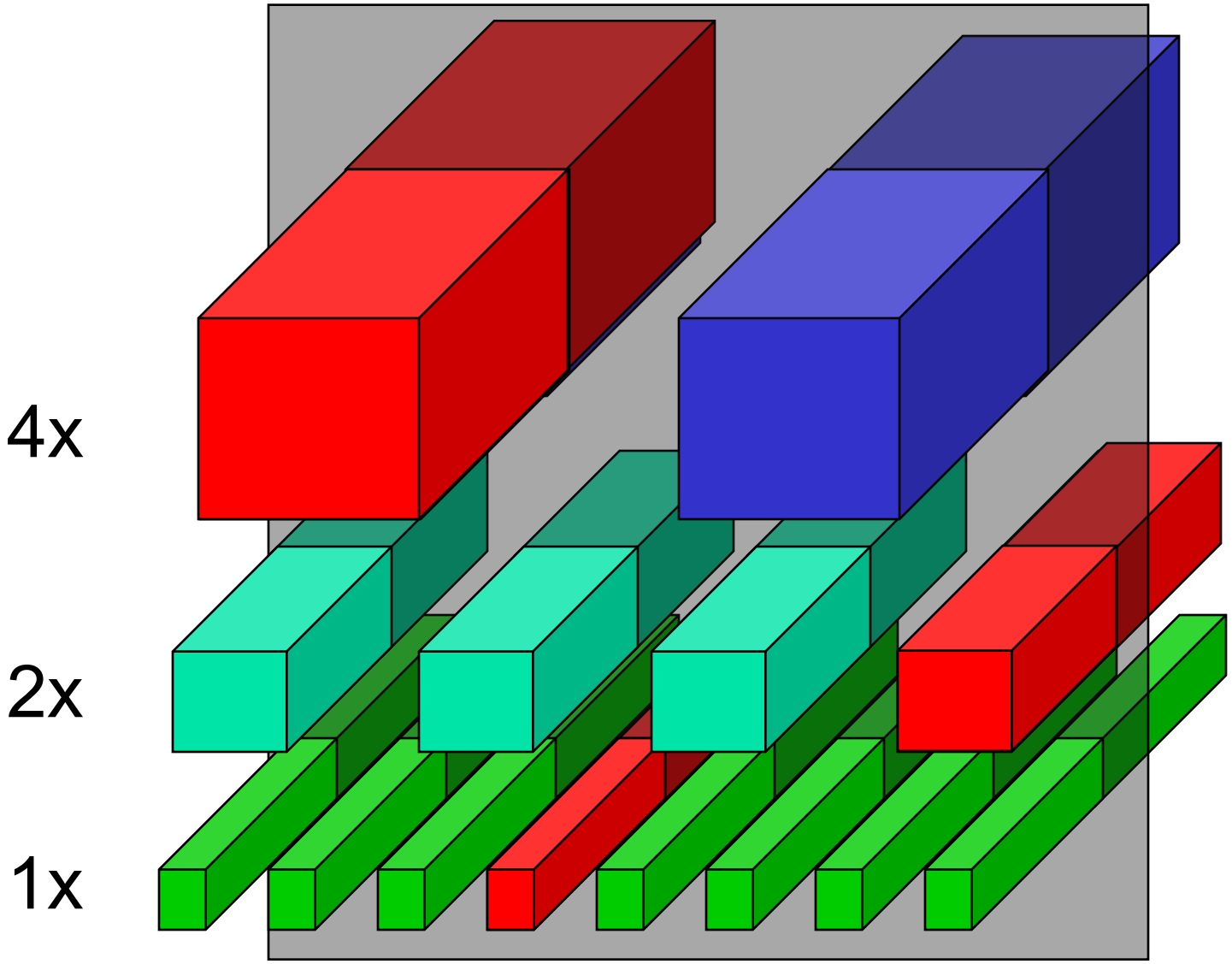


- Routers could not handle these structures well if at all
- Even if they could, routability would suffer

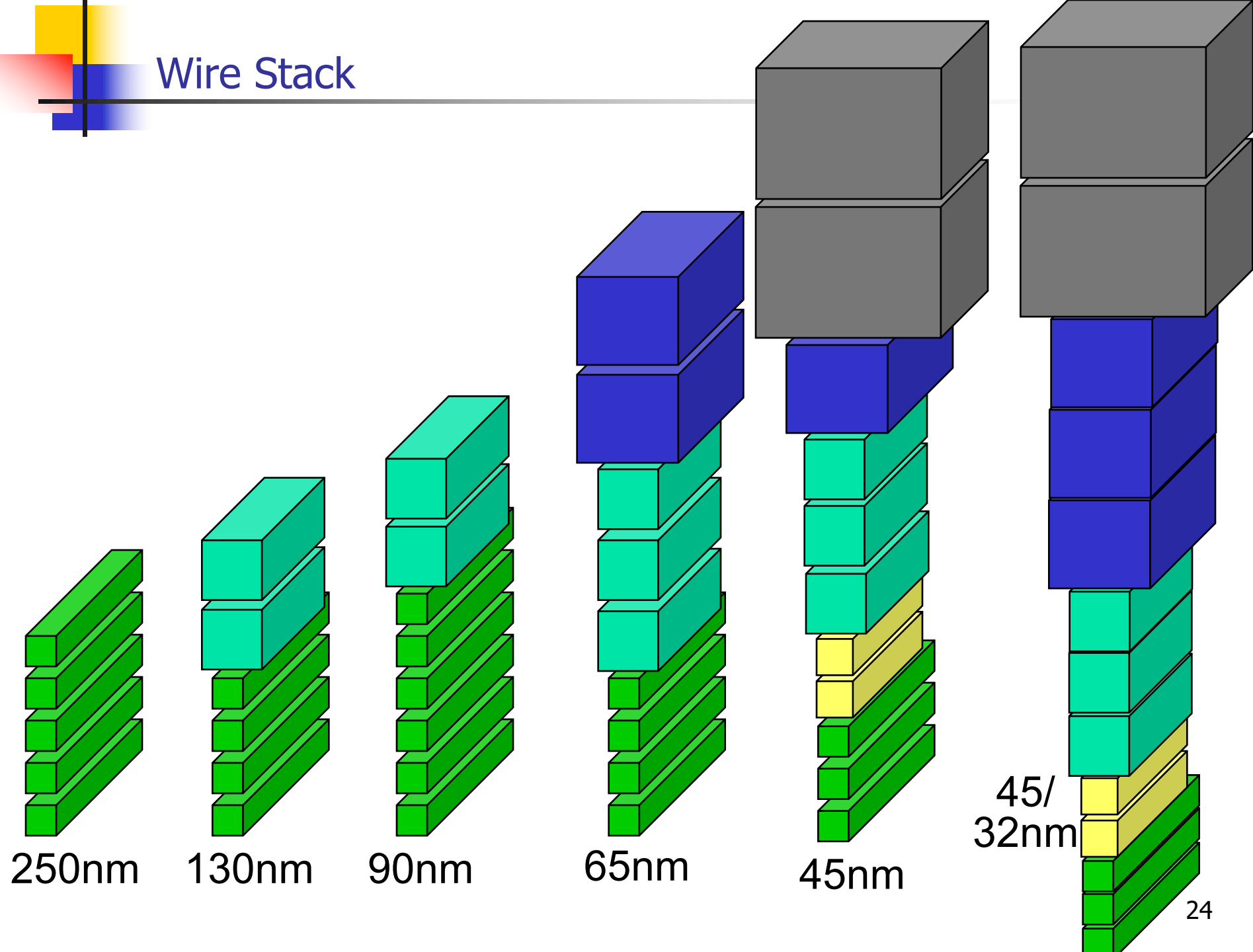


- With simultaneous buffering, results close to tapering
- Theoretical formula: 3.5% difference in optimal cases

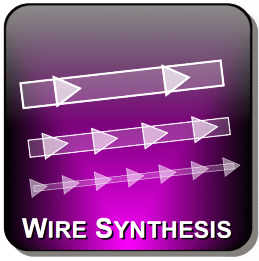
Performing Layer Assignment



Wire Stack



Metal RC Characteristics



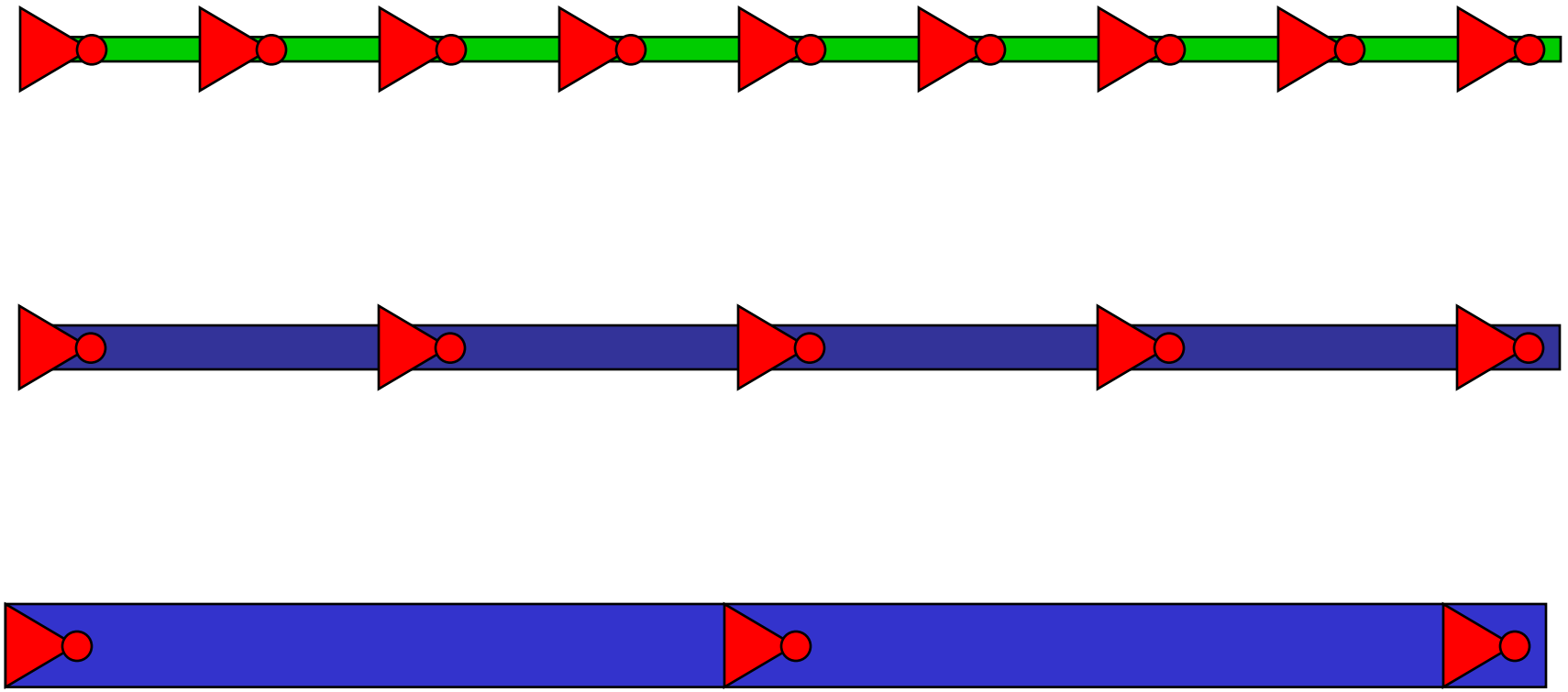
cu65	Width (micron)	Resistance (kohm/mm)	Capacitance (ff/mm)
1x (M3)	0.1	1.82	192
2x (B1)	0.2	0.37	209
4X (EA)	0.4	0.10	232

cu45	Width (micron)	Resistance (kohm/mm)	Capacitance (ff/mm)
1x (M2)	0.07	2.824	219
1.3x (C1)	0.1	1.773	201
2x (B1)	0.14	0.710	180
10X (UB)	0.8	0.024	216

cu32	Resistance (kohm/mm)	Capacitance (ff/mm)
1x (M4)	5.758	235
2x (B1)	1.171	208
16X (MA)	0.024	276

Technology	45 nm		32 nm	
Layers	2x layer	10x layer	2x layer	16x layer
Time of Flight (ps/mm)	104	51	243	148
Optimal Buff Dist (mm)	0.52	2.94	0.36	1.39

Buffering on Different Layers (M2, B1, EA)



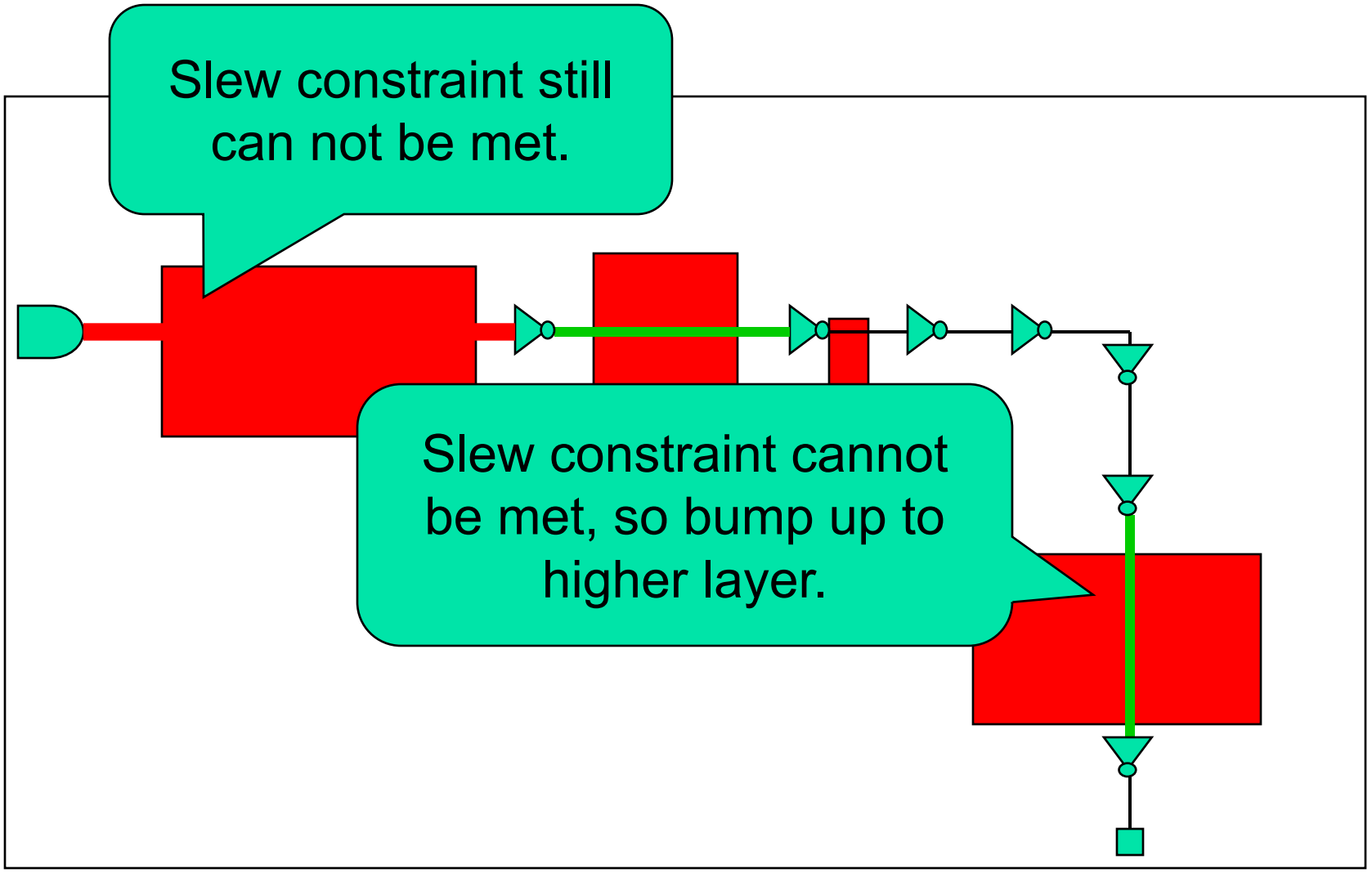
- Signals can travel about 2x and 3.5X further and obtain 2x and 3x delay reduction, respectively for the 2x and 4x layers.

Buffer Reach Length

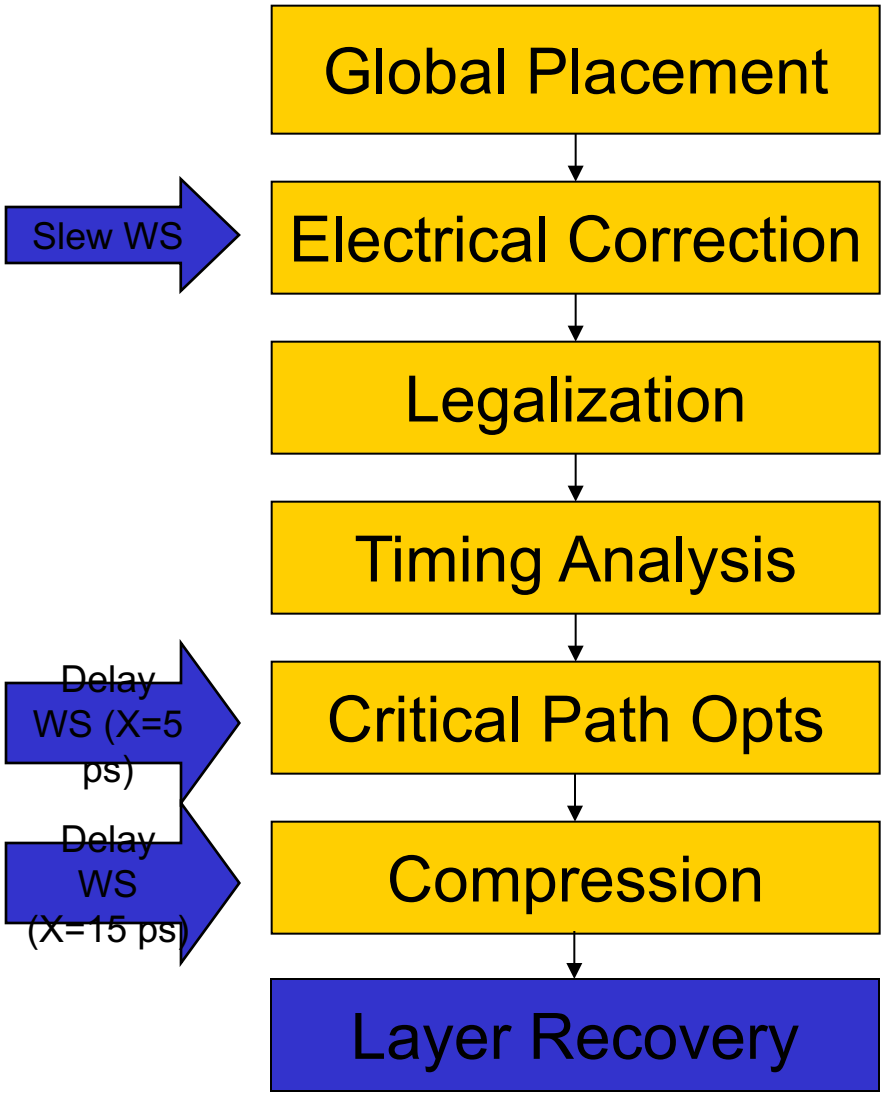
	45 nm		32 nm	
	2x layer	10x layer	2x layer	16x layer
Slew reach	1.7 mm	2.9 mm	0.5 mm	0.7 mm
Optimal timing	0.52 mm	2.9 mm	0.35 mm	1.38 mm

- Plane and wire code constraints:
  - Define the routing layers range: B1 to UB;
  - Define the wire width and space for certain layer range: 2X spacing and width from M1 to B3;

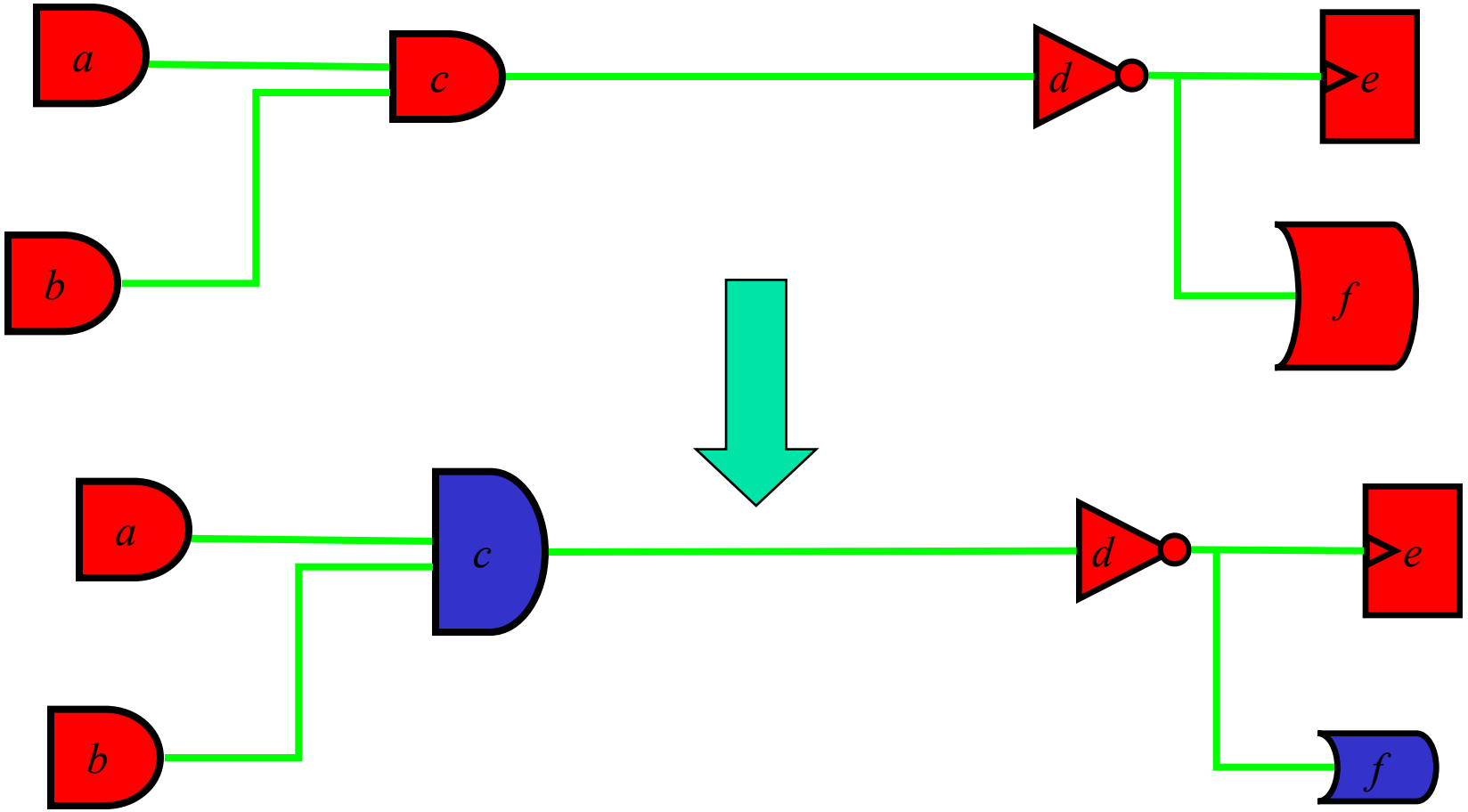
Slew Based Wire Synthesis



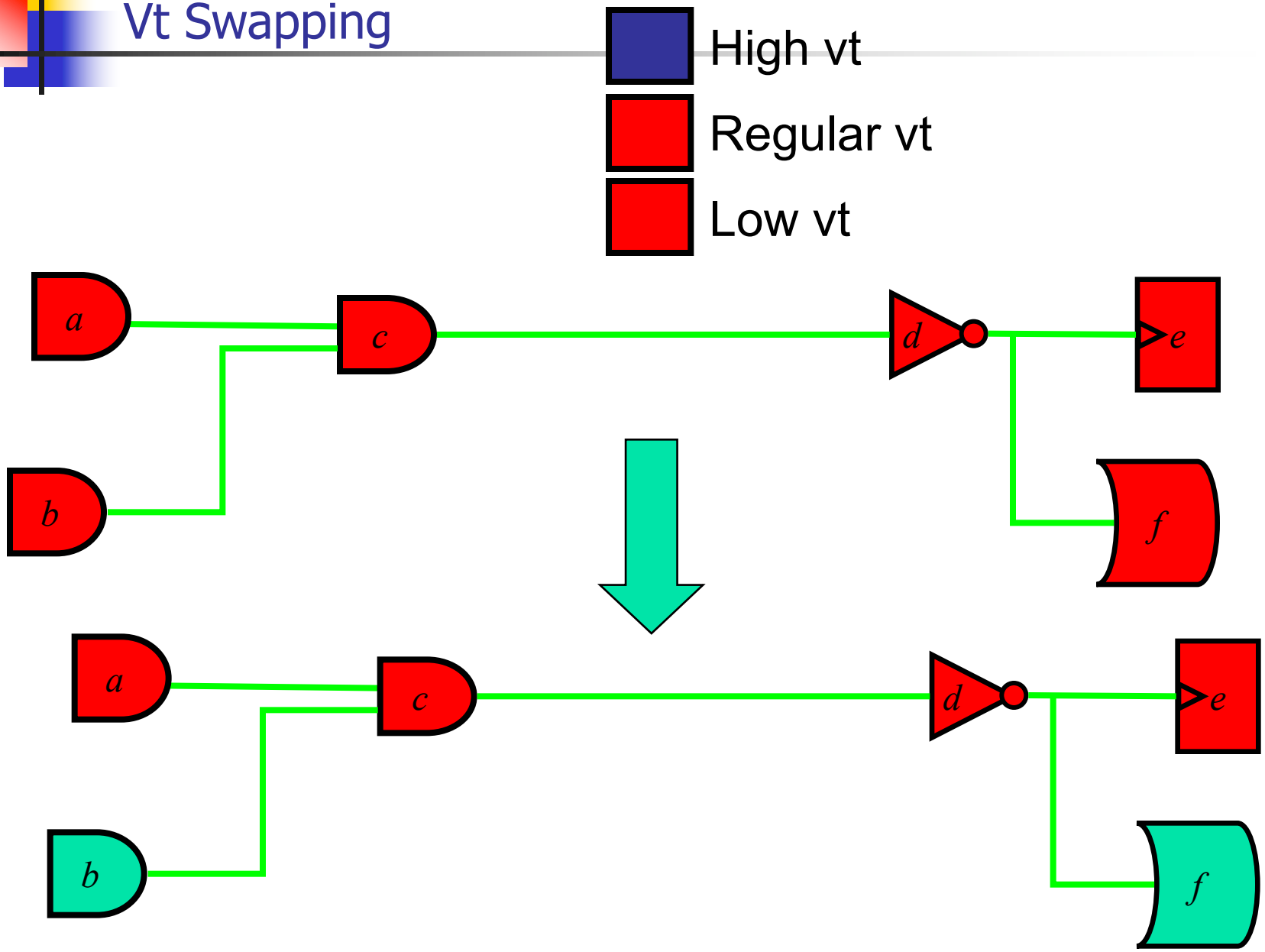
Wire Synthesis



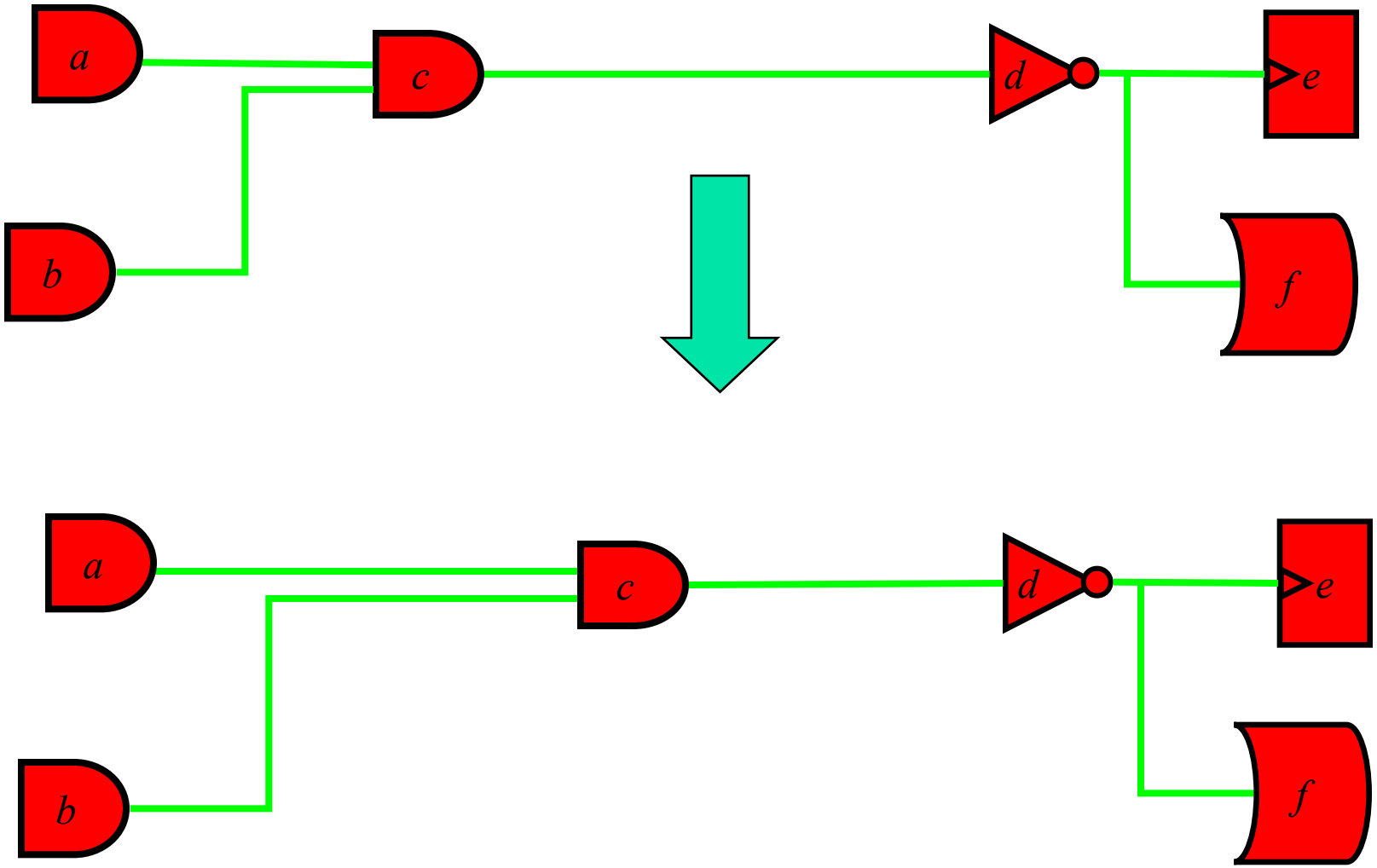
Gate Sizing or Repowering



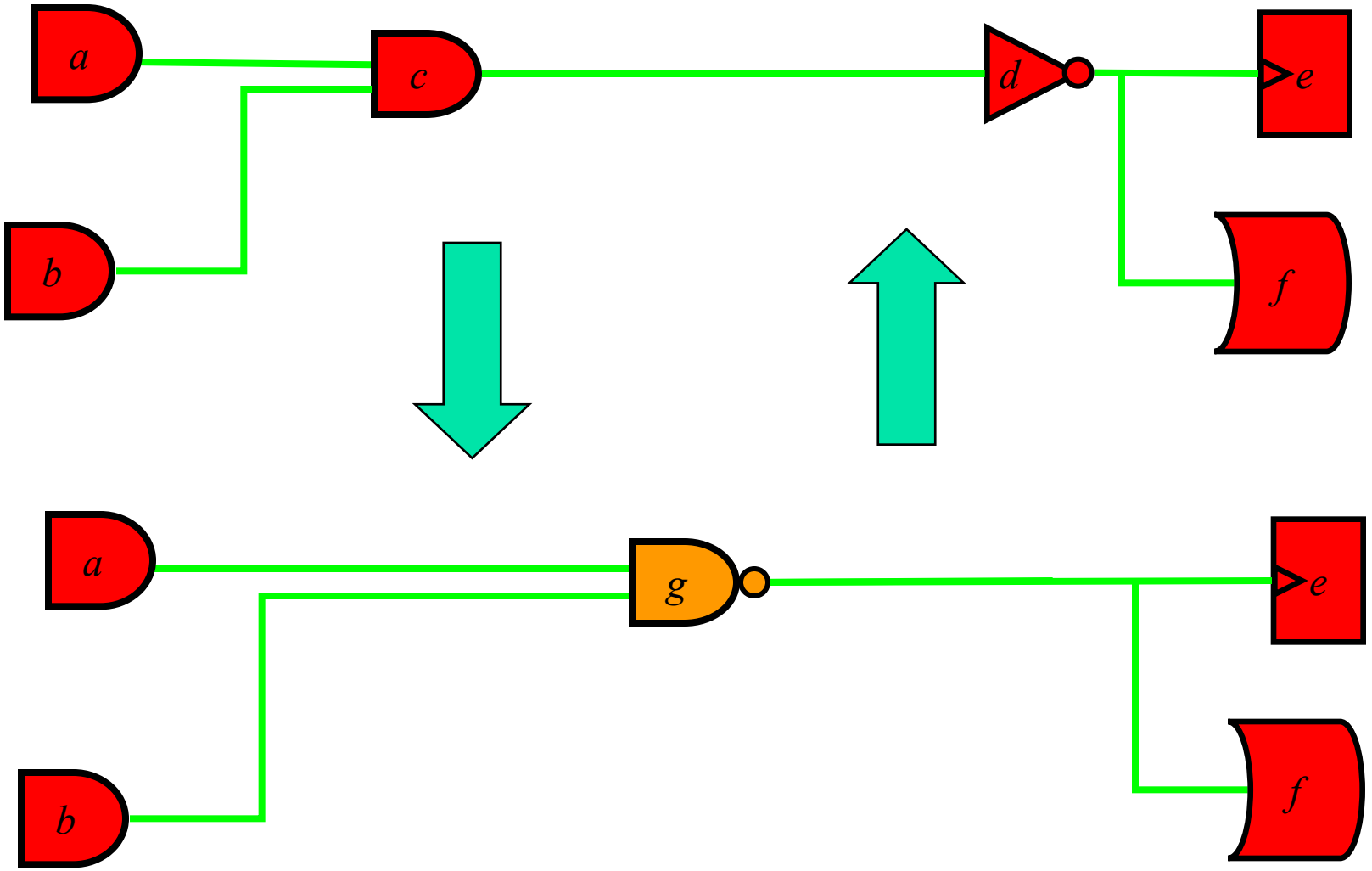
Vt Swapping



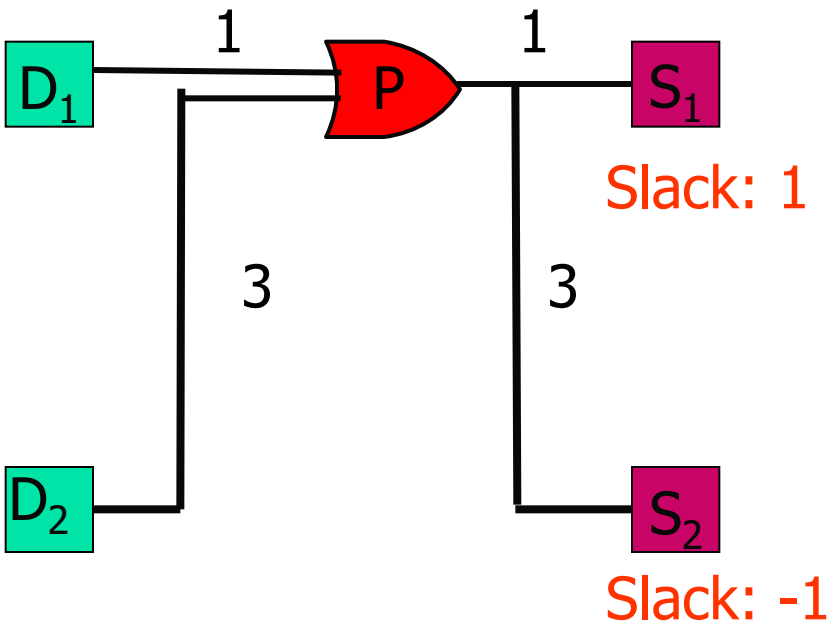
Cell Movement

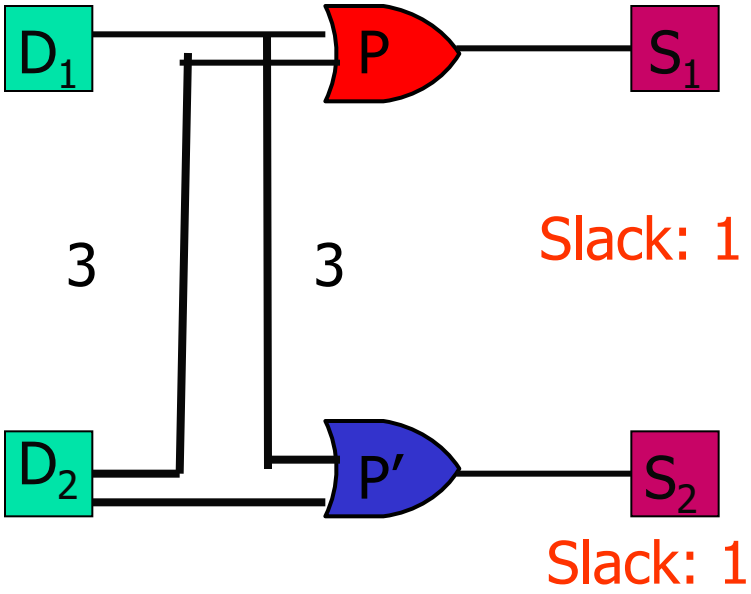


Inverter Absorption / Decomposition



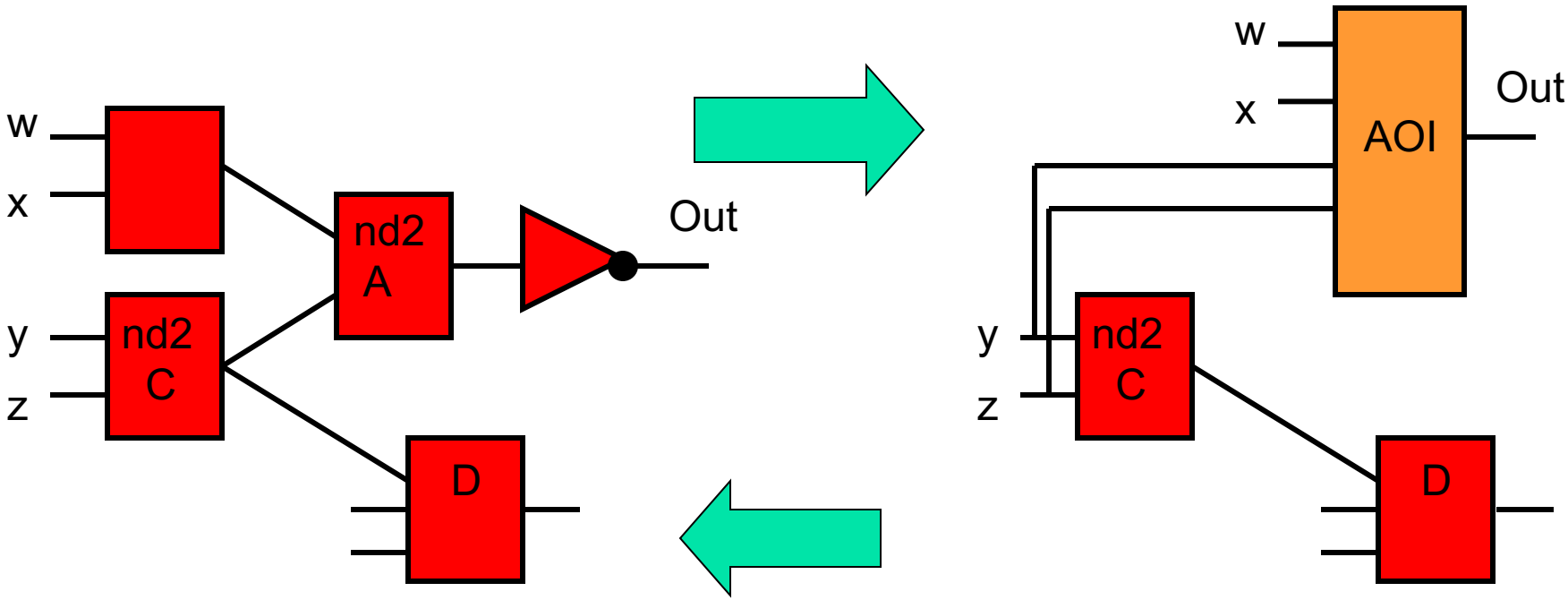
Cloning





Courtesy: Zhuo Li / David Papa

Composition / Decomposition

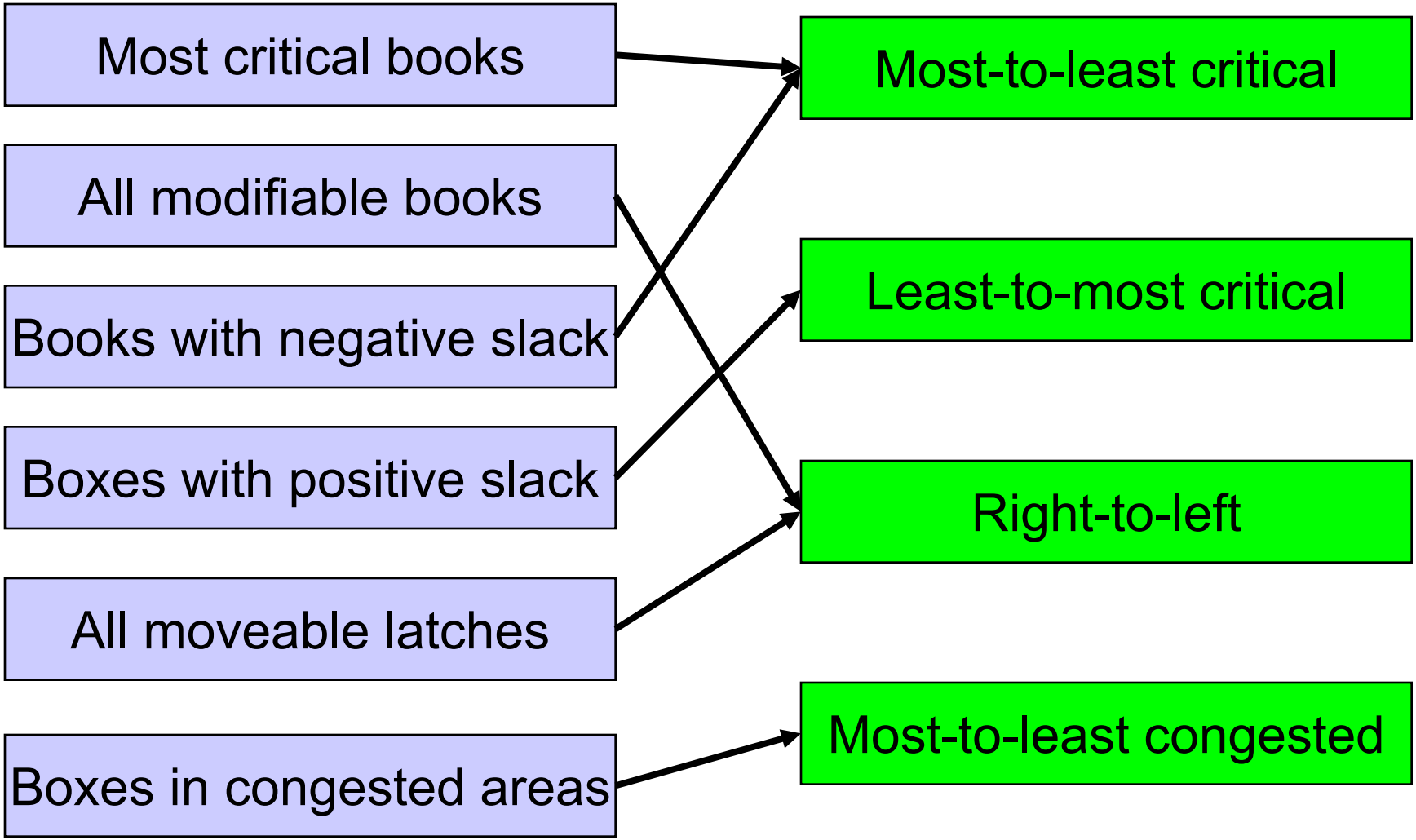


Courtesy: Louise Trevillian

Object Selection

- Most critical books
- All modifiable books
- Books with negative slack
- Boxes with positive slack
- All moveable latches
- Boxes in congested areas

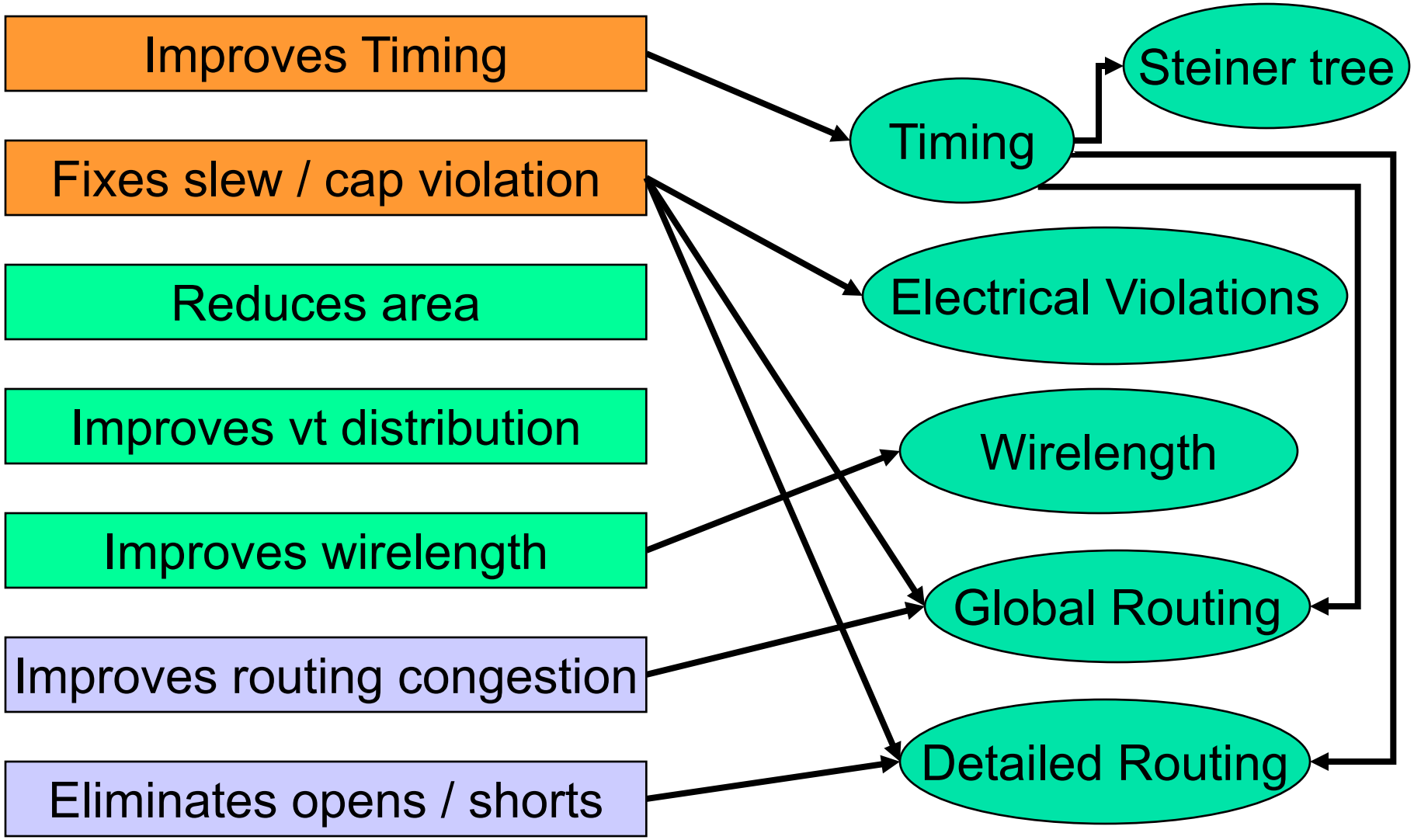
Object Ordering



Success Metrics

- Improves Timing
- Fixes slew / cap violation
- Reduces area
- Improves vt distribution
- Improves wirelength
- Improves routing congestion
- Eliminates opens / shorts

Success Metrics Require Incremental Computation



Example: Critical Path Optimization

Selection: boxes with negative slack

Order: Most-to-least critical

Transform: logic decomposition

Success: timing improves +
No slew and capacitance violations +
tolerable area increase

Example Area Recovery

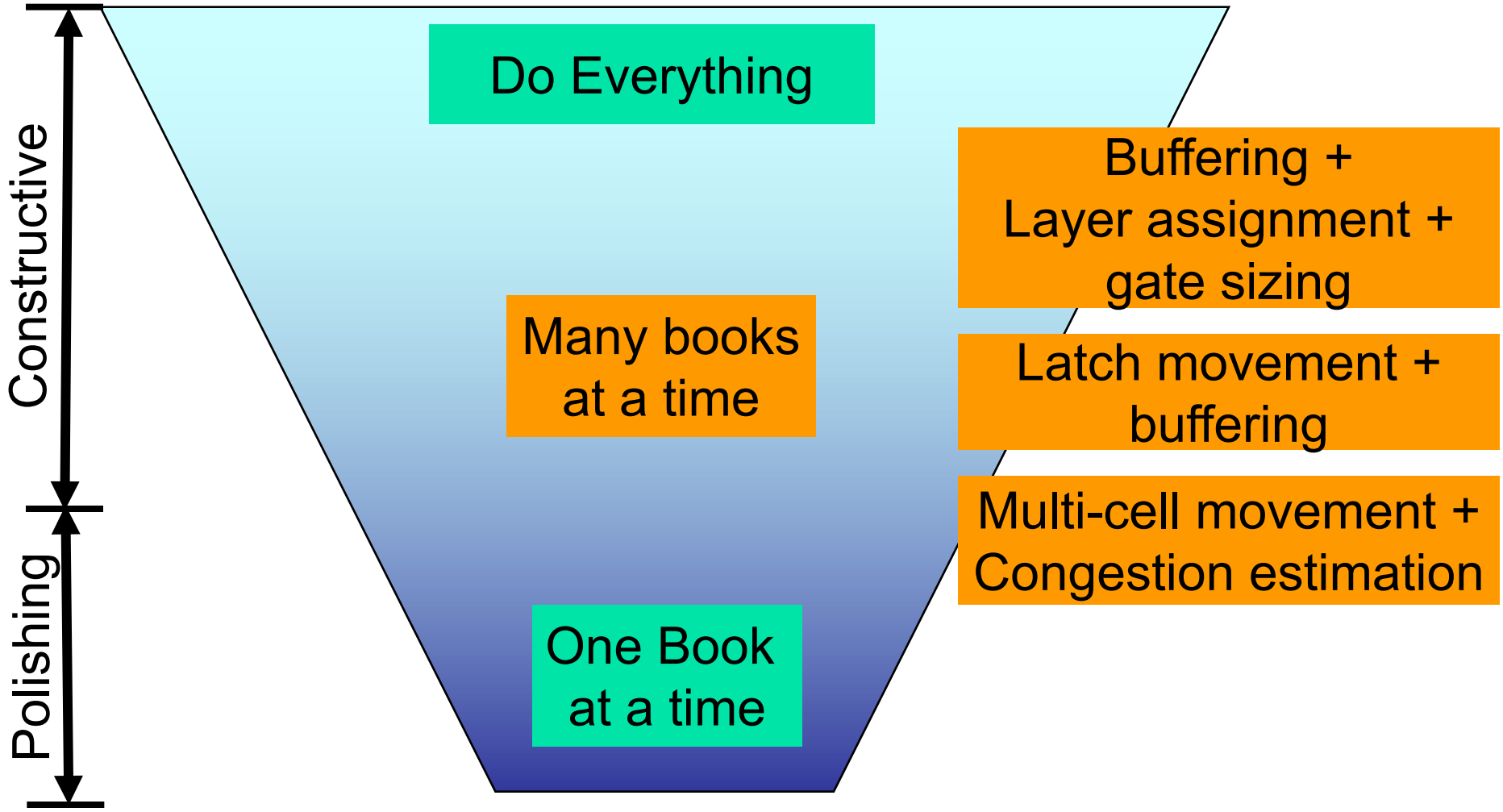
Selection: boxes with positive slack

Order: Least-to-most critical

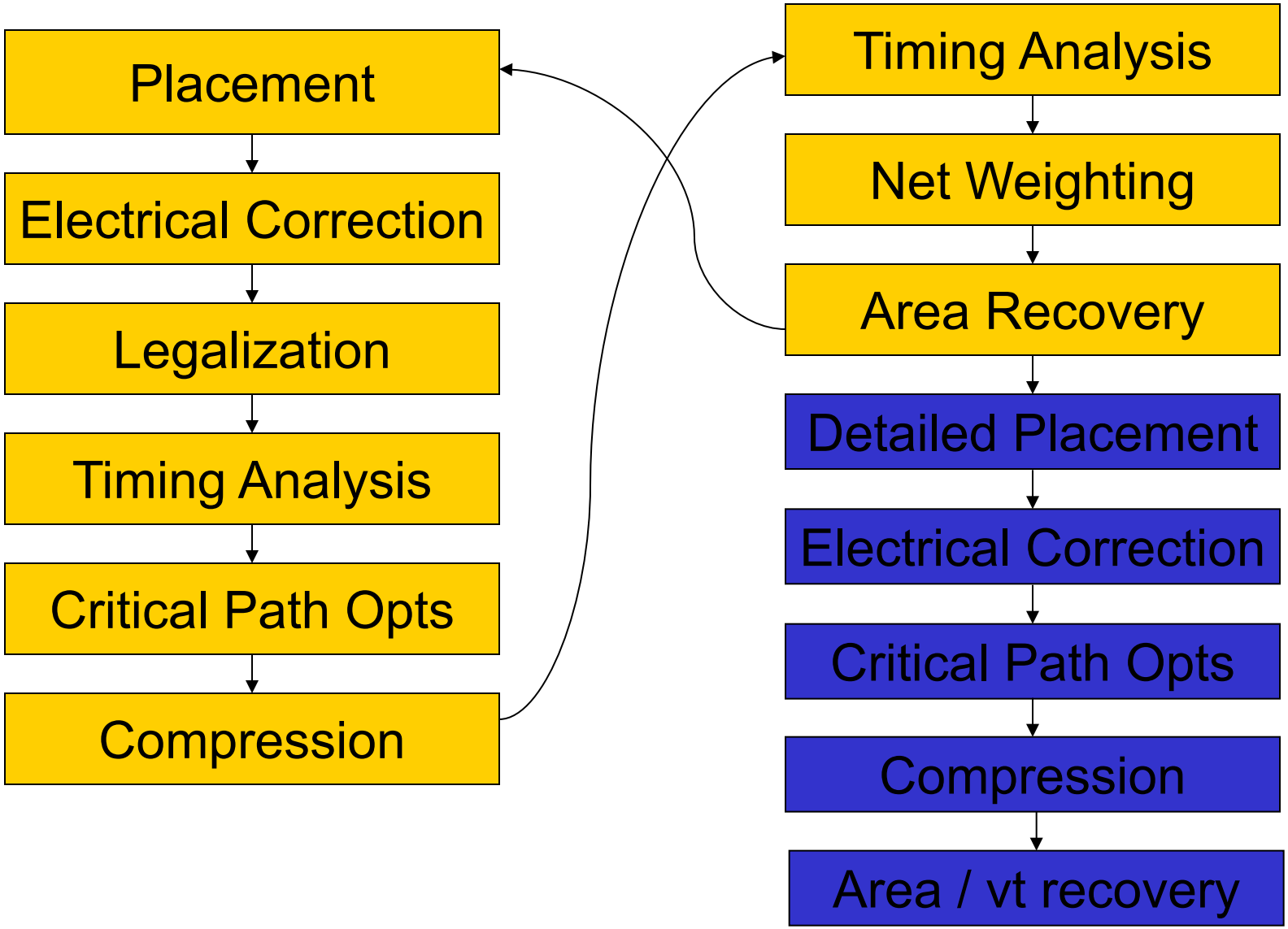
Transform: repowering / buffer deletion

Success: area improves +
Timing does not become negative +
No slew and capacitance violations

Variable Optimization and Accuracy



Basic Physical Synthesis Flow



Trends in Physical Synthesis

- Historically all about timing
- Now: physical effects of routing paramount
  - Switching from Steiners to detailed routes disruptive
  - Must model wires earlier in the flow
- Parallelization
- Higher densities