Floorplanning

Presented By:
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IBM STG India Enterprise Systems Development

Chip Planning

- Introduction

- Floorplanning Algorithms
  - Floorplan Sizing
  - Cluster Growth
  - Simulated Annealing

- Power and Ground Routing
  - Design of a Power-Ground Distribution Network
  - Planar Routing

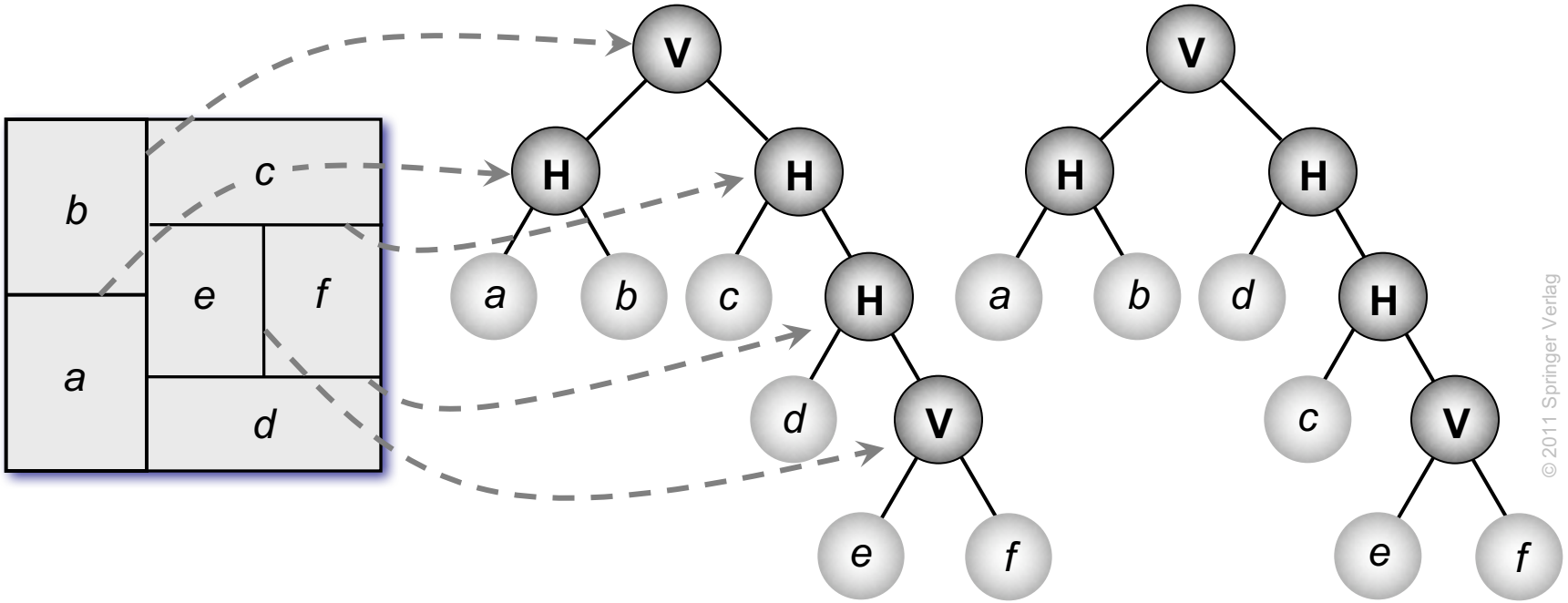
    Mesh Routing

Optimization Goals

- Area and shape of the global bounding box
  - Global bounding box of a floorplan is the minimum axis-aligned rectangle that contains all floorplan blocks.
  - Area of the global bounding box represents the area of the top-level floorplan
  - Minimizing the area involves finding (x,y) locations, as well as shapes, of the individual blocks.
- Total wirelength
  - Long connections between blocks may increase signal propagation delays in the design.
- Combination of area $area(F)$ and total wirelength $L(F)$ of floorplan F
  - Minimize $\checkmark \cdot area(F) + (1 - \checkmark) \cdot L(F)$
    where the parameter $0 \leq \checkmark \leq 1$ gives the relative importance between $area(F)$ and $L(F)$
- Signal delays
  - Static timing analysis is used to identify the interconnects that lie on critical paths.

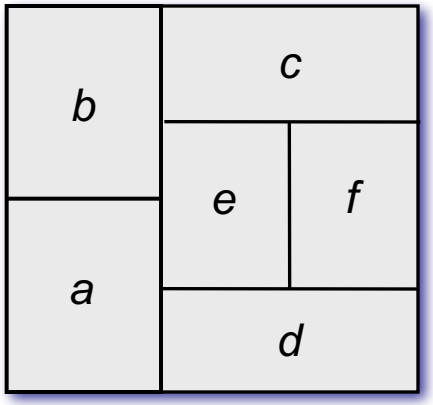
Introduction

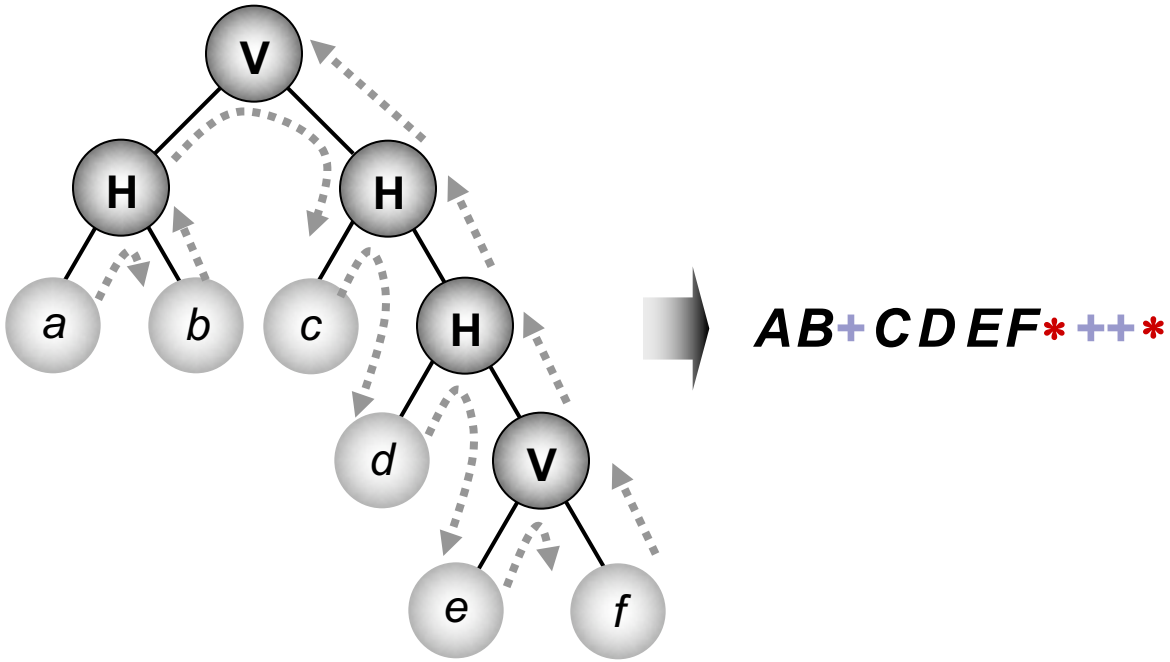
Slicing floorplan and two possible corresponding slicing trees



Introduction

Polish expression

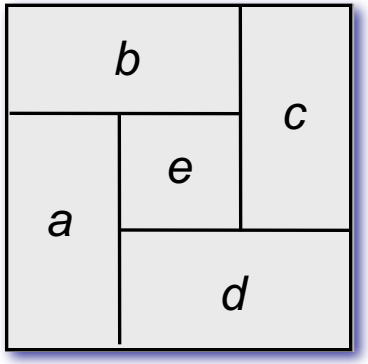


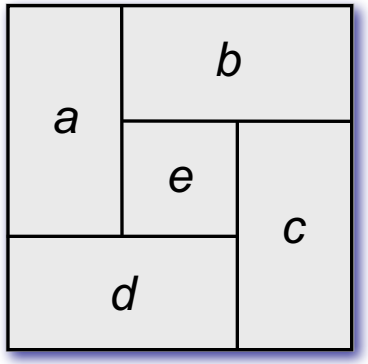


- Bottom up: **V** → * and **H** → +
- Length 2*n*-1 (*n* = Number of leaves of the slicing tree)

Introduction

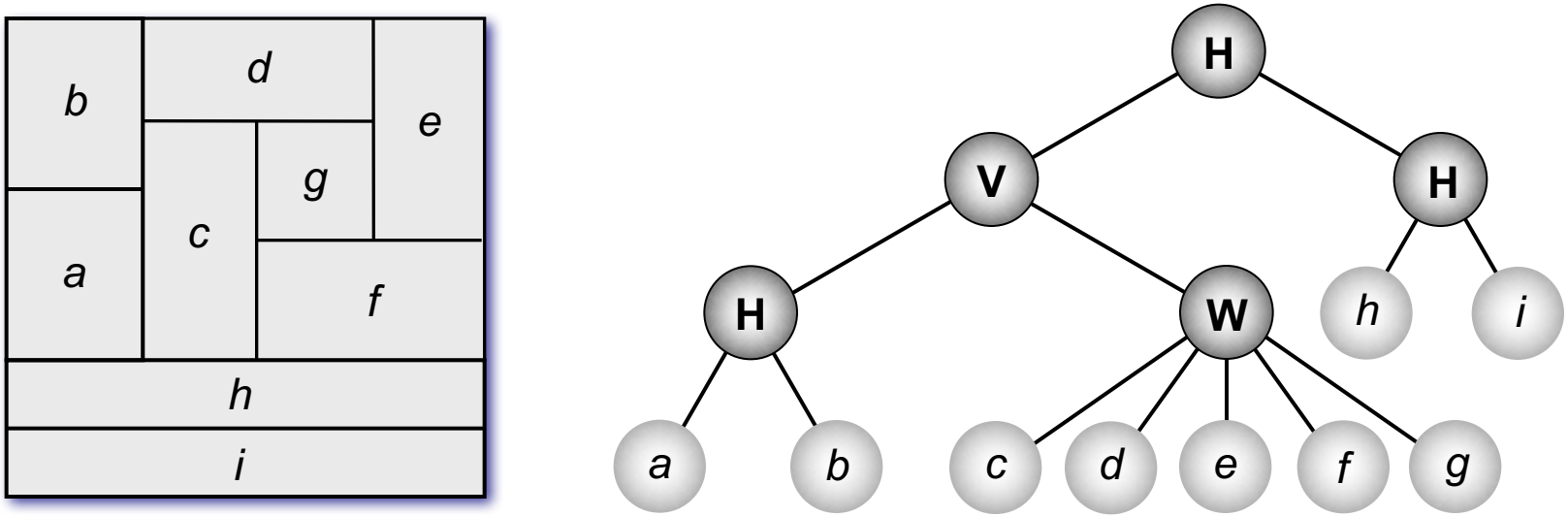
Non-slicing floorplans (wheels)





Introduction

Floorplan tree: Tree that represents a hierarchical floorplan



H — Horizontal division (objects to the top and bottom)

V — Vertical division (objects to the left and right)

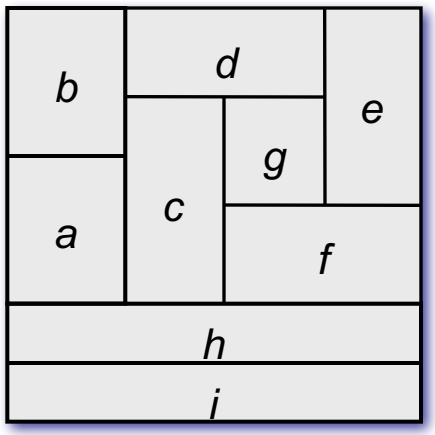
W — Wheel (4 objects cycled around a center object)

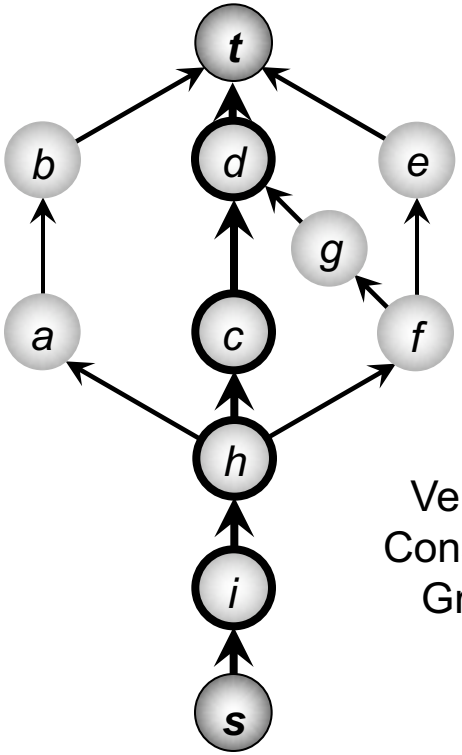
Introduction

- In a vertical constraint graph (VCG), node weights represent the heights of the corresponding blocks.
  - Two nodes v_i and v_j, with corresponding blocks m_i and m_j, are connected with a directed edge from v_i to v_j if m_i is below m_j.
- In a horizontal constraint graph (HCG), node weights represent the widths of the corresponding blocks.
  - Two nodes v_i and v_j, with corresponding blocks m_i and m_j, are connected with a directed edge from v_i to v_j if m_i is to the left of m_j.
- The longest path(s) in the VCG / HCG correspond(s) to the minimum vertical / horizontal floorplan span required to pack the blocks (floorplan height / width).
- A constraint-graph pair is a floorplan representation that consists of two directed graphs – *vertical constraint graph* and *horizontal constraint graph* – which capture the relations between block positions.

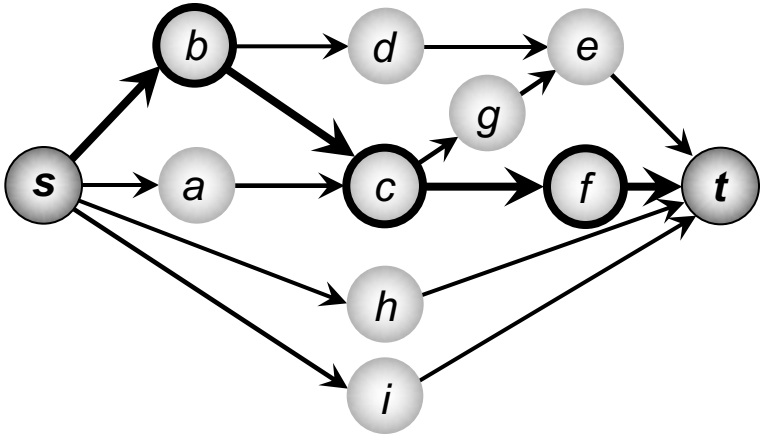
Introduction

Constraint graphs





Vertical Constraint Graph



Horizontal Constraint Graph

Floorplanning Algorithms

Common Goals

- To minimize the total length of interconnect, subject to an upper bound on the floorplan area

or

- To simultaneously optimize both wire length and area

Otten, R.: Efficient Floorplan Optimization. Int. Conf. on Computer Design, 499-502, 1983

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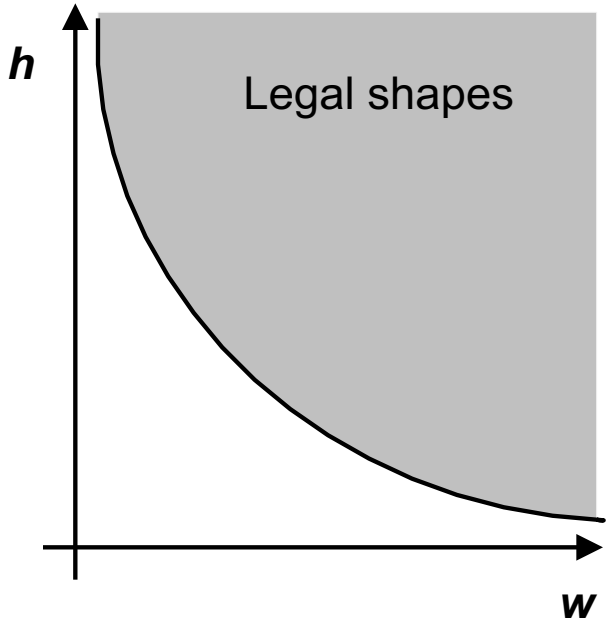
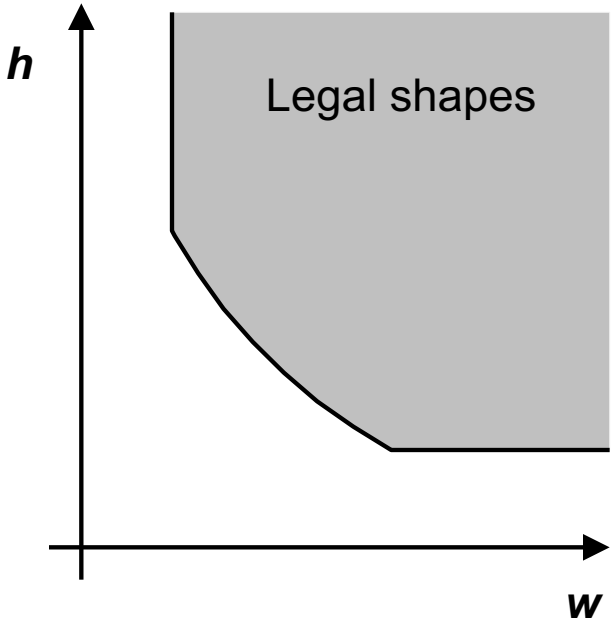
Floorplan Sizing

Shape functions



$h * w \geq A$

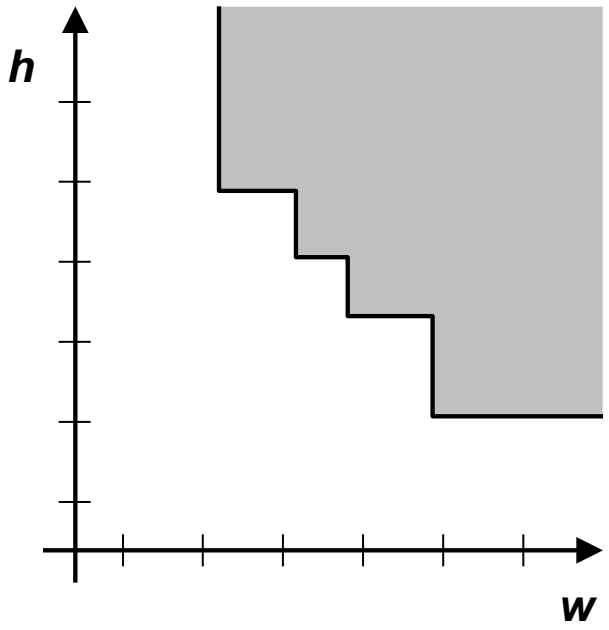


Block with minimum width and height restrictions

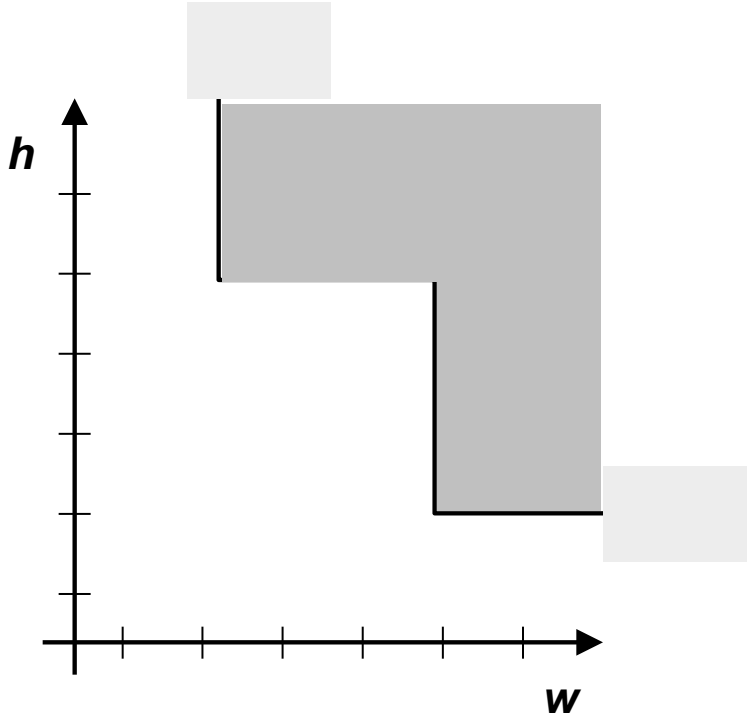
Otten, R.: Efficient Floorplan Optimization. Int. Conf. on Computer Design, 499-502, 1983

Floorplan Sizing

Shape functions



Discrete (*h,w*) values

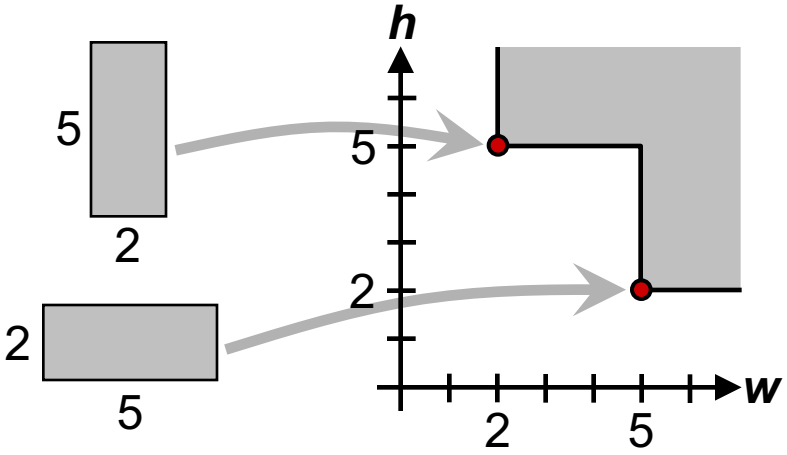


Hard library block

Otten, R.: Efficient Floorplan Optimization. Int. Conf. on Computer Design, 499-502, 1983

Floorplan Sizing

Corner points



Floorplan Sizing

- This algorithm finds the **minimum floorplan area** for a given slicing floorplan in polynomial time. For non-slicing floorplans, the problem is NP-hard.

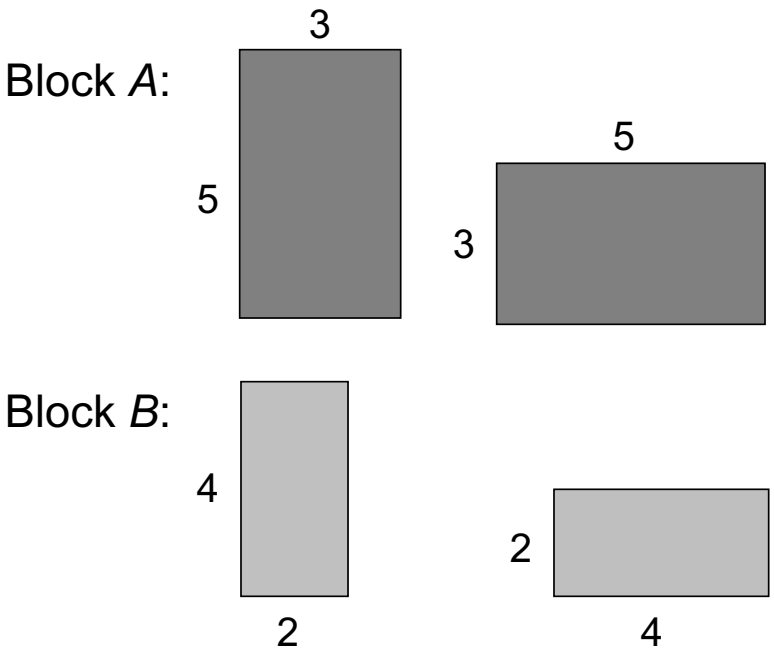
- Construct the shape functions of all individual blocks

- Bottom up: Determine the shape function of the top-level floorplan
  from the shape functions of the individual blocks

- Top down: From the corner point that corresponds to the minimum top-level floorplan area, trace back to each block's shape function to find that block's dimensions and location.

Floorplan Sizing – Example

Step 1: Construct the shape functions of the blocks



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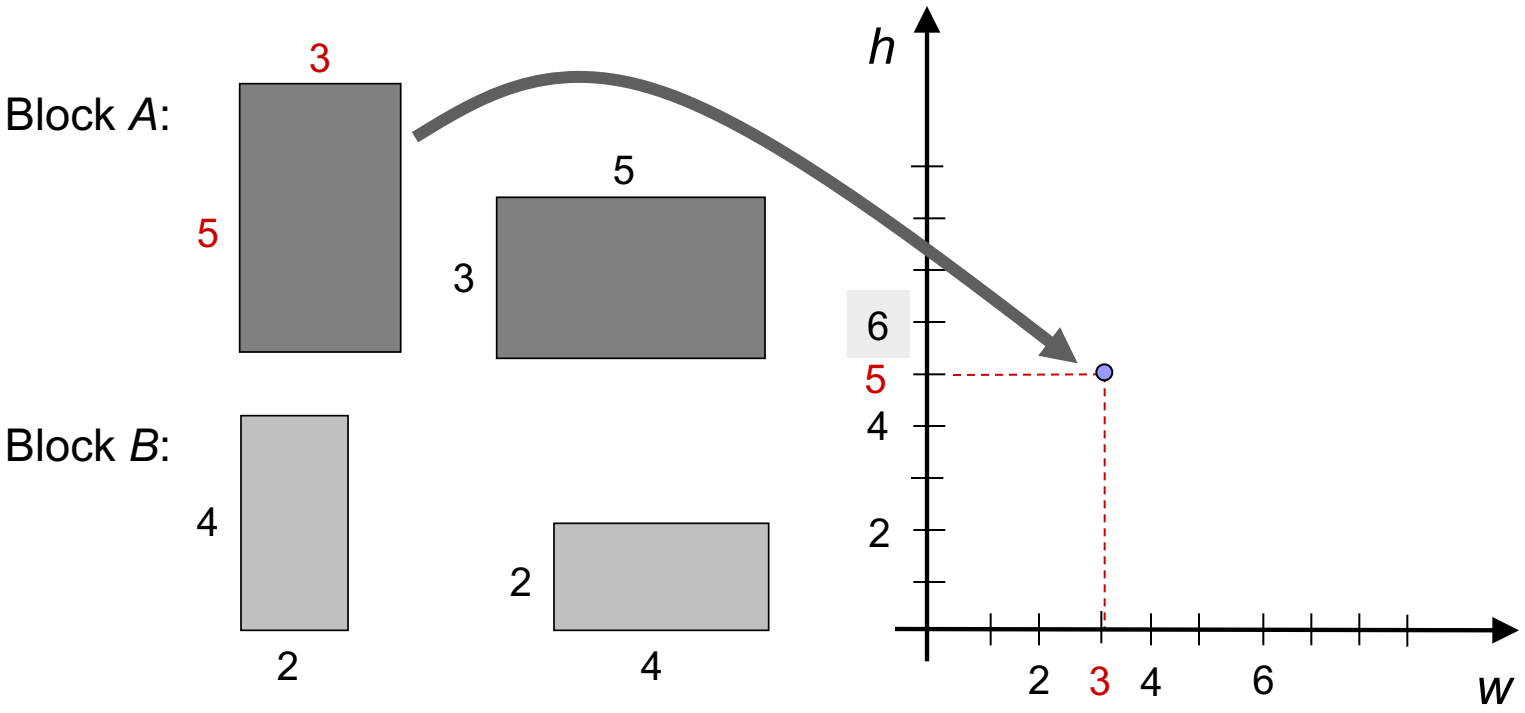

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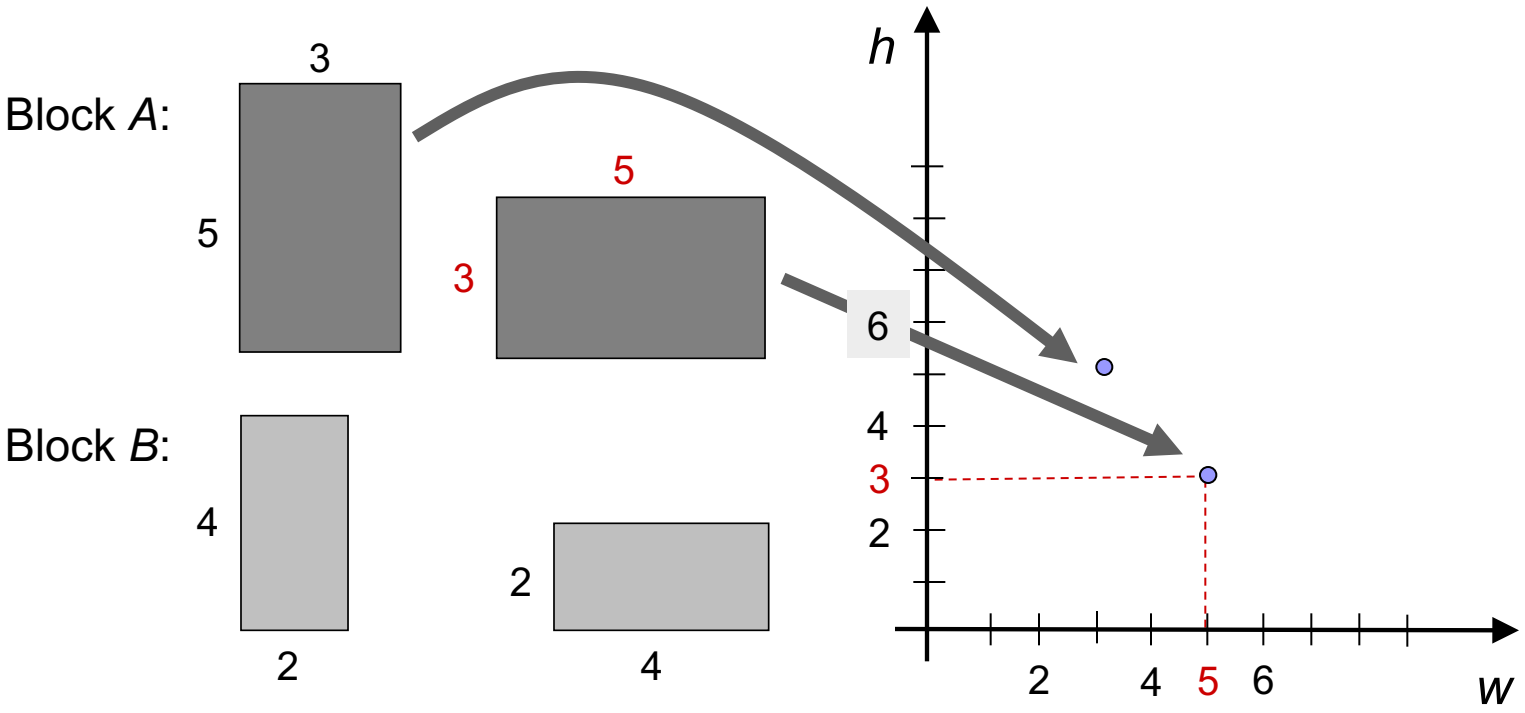

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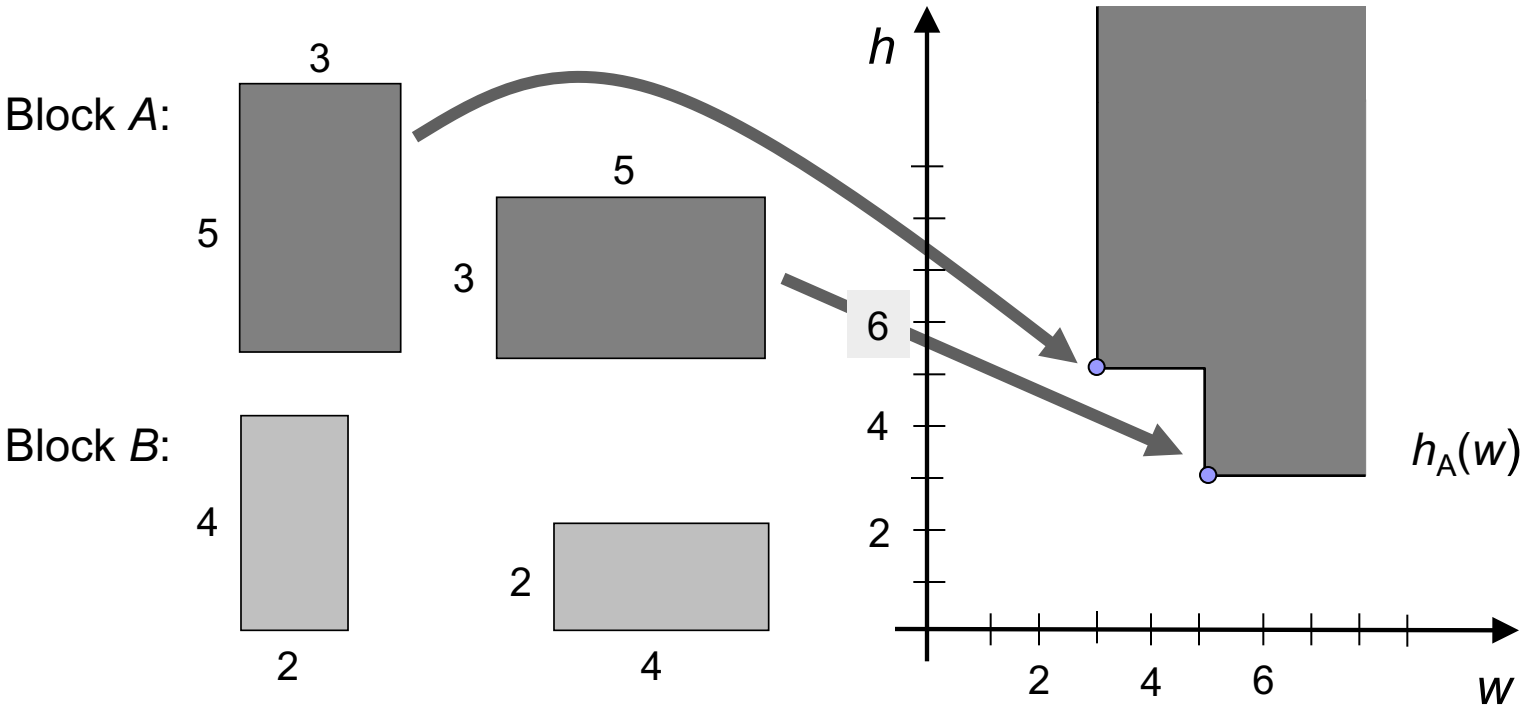

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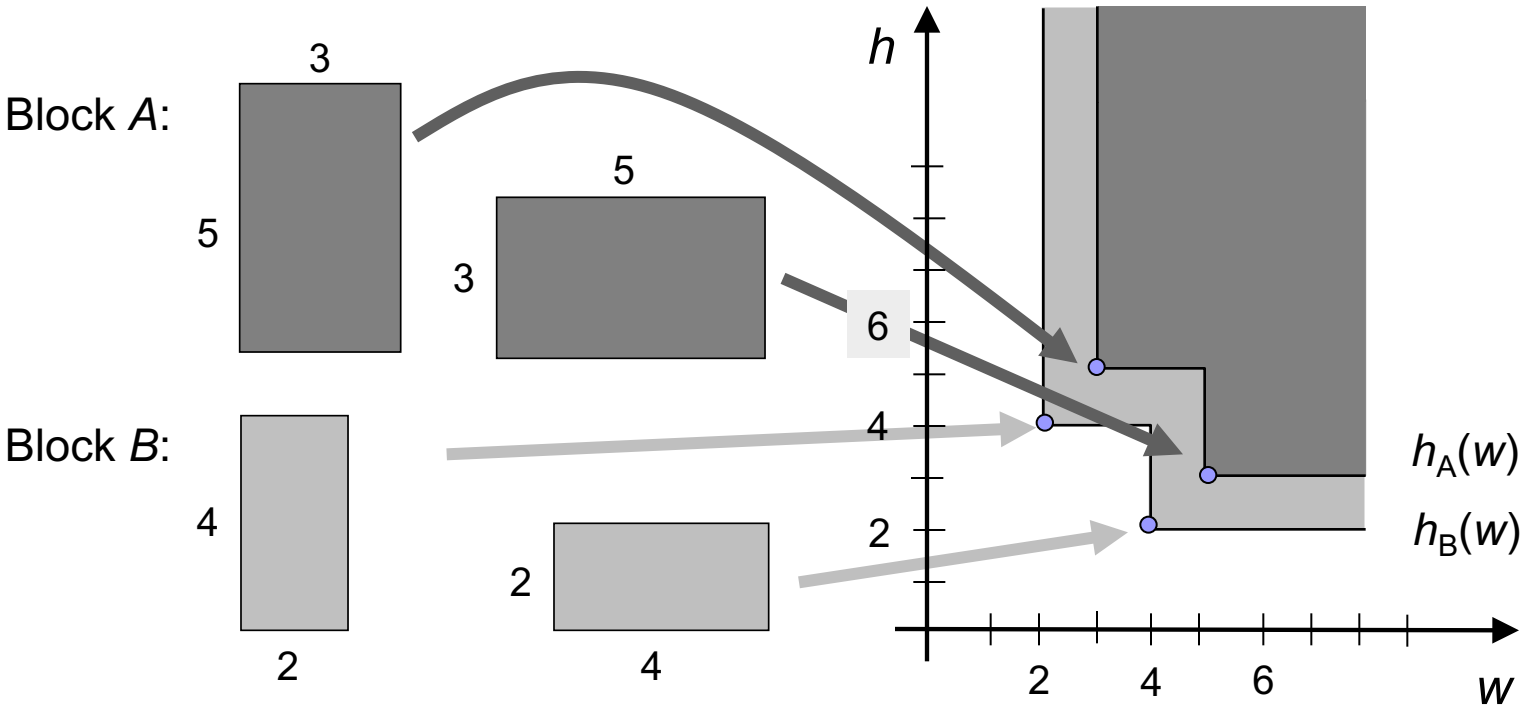
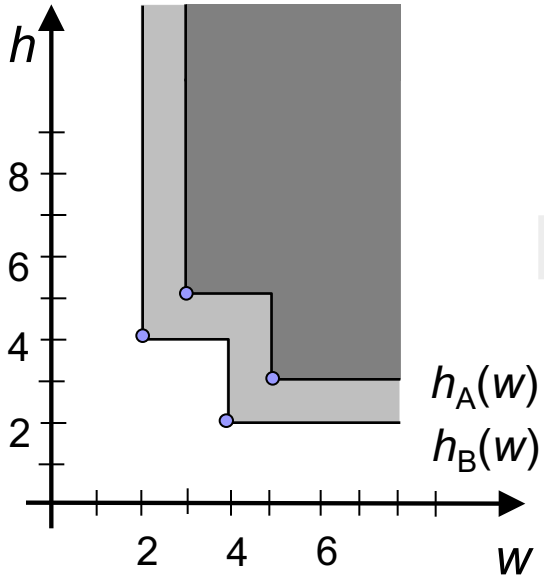


Floorplan Sizing – Example

Step 2: Determine the shape function of the top-level floorplan (vertical)



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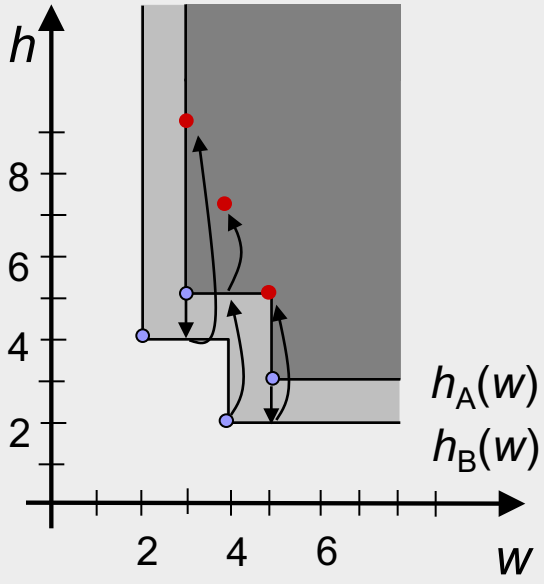

Floorplan Sizing – Example

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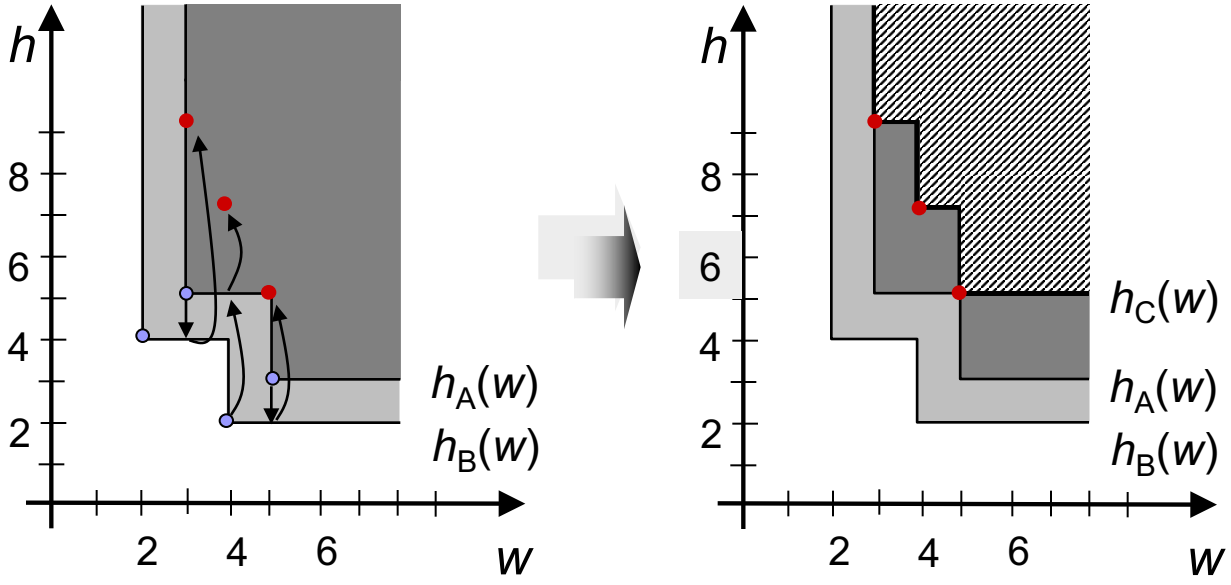

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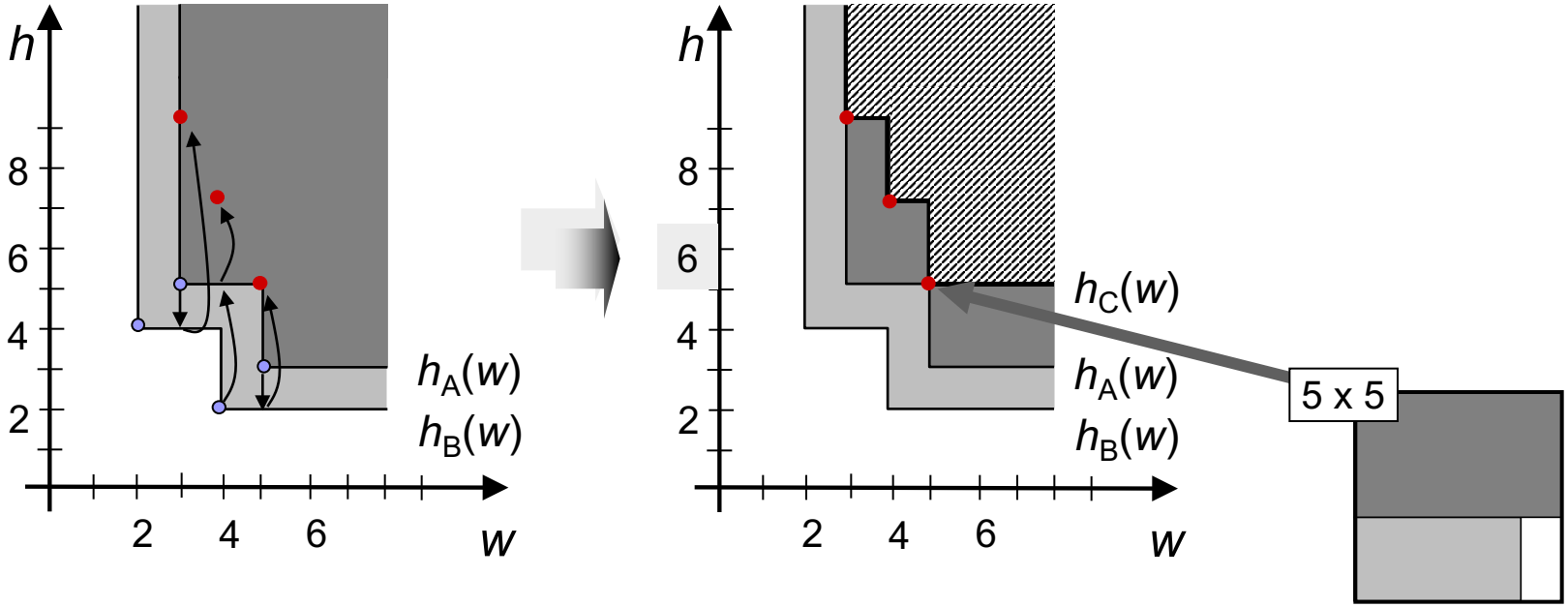

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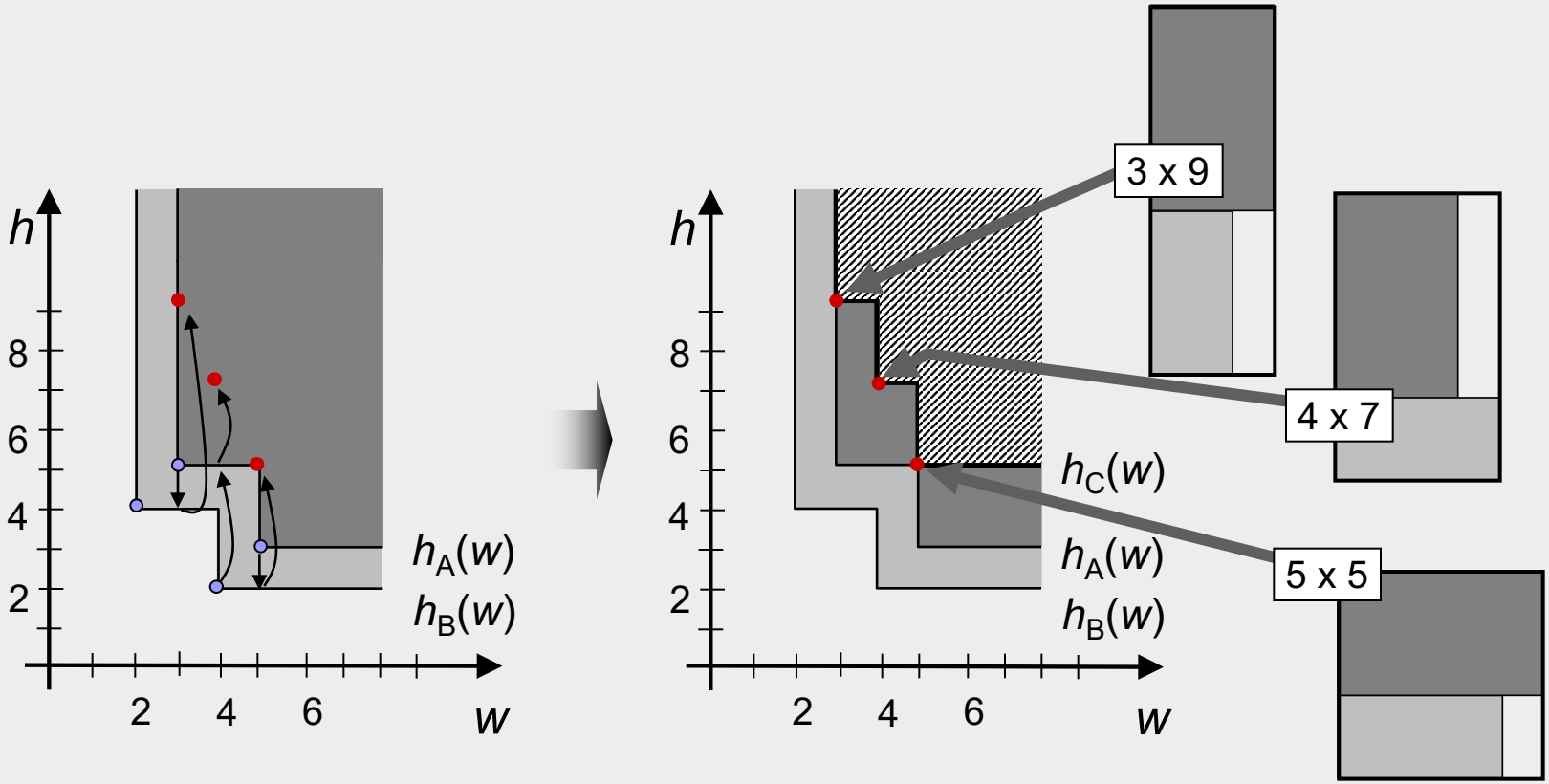

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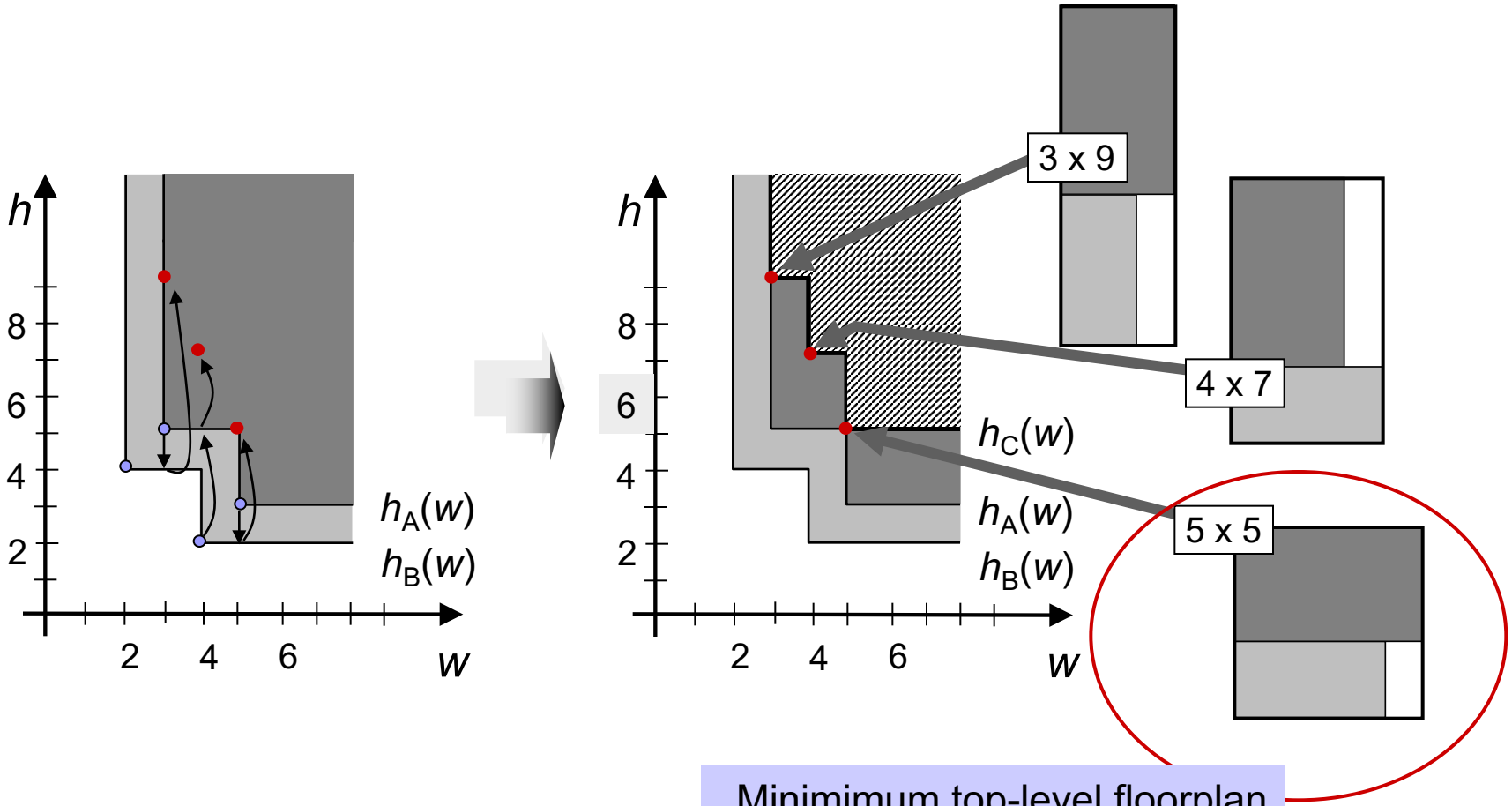
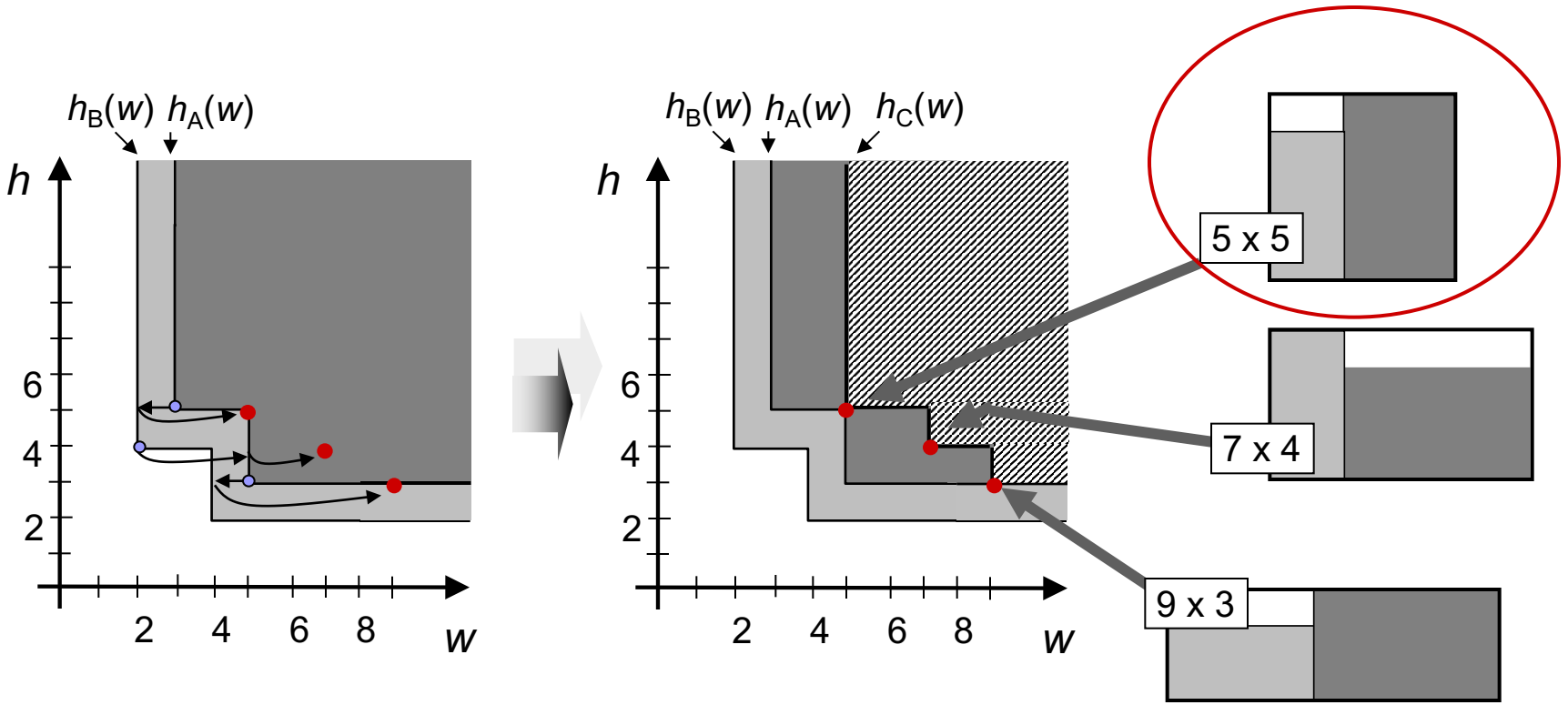


Minimum top-level floorplan with vertical composition

Floorplan Sizing – Example

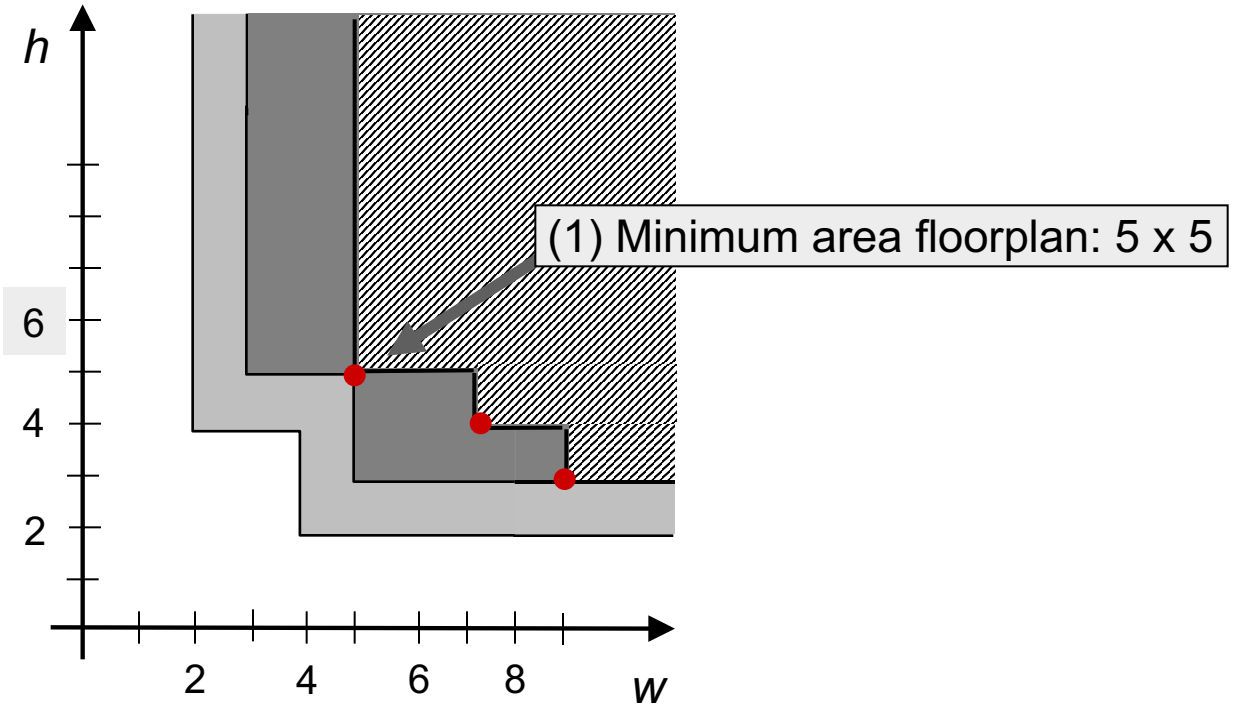
Step 2: Determine the shape function of the top-level floorplan (horizontal)



Minimum top-level floorplan with horizontal composition

Floorplan Sizing – Example

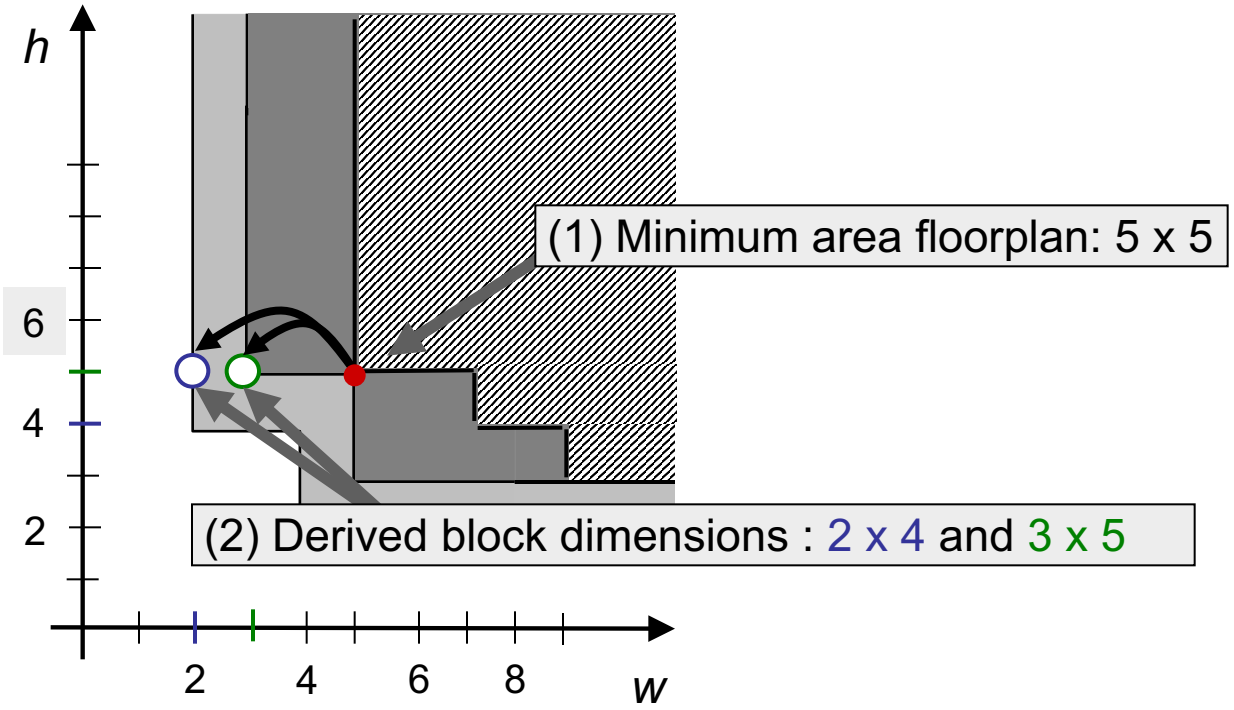
Step 3: Find the individual blocks' dimensions and locations



Horizontal composition

Floorplan Sizing – Example

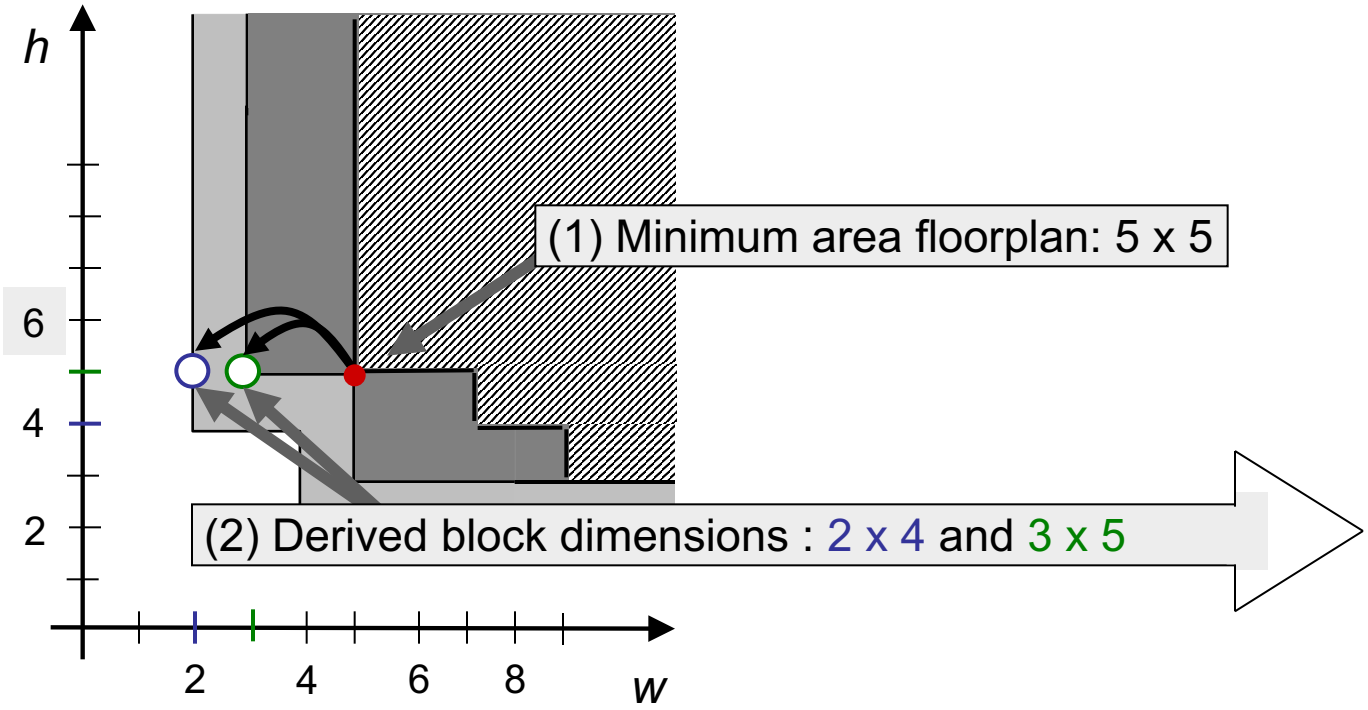
Step 3: Find the individual blocks' dimensions and locations

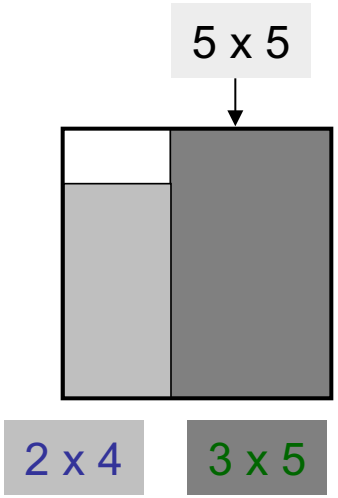


Horizontal composition

Floorplan Sizing – Example

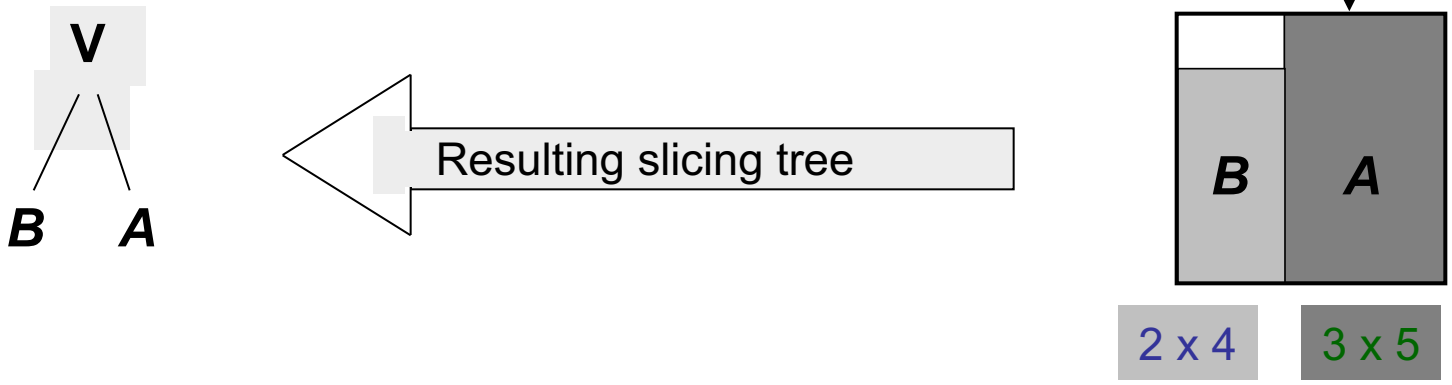
Step 3: Find the individual blocks' dimensions and locations





Horizontal composition

Floorplan Sizing – Example



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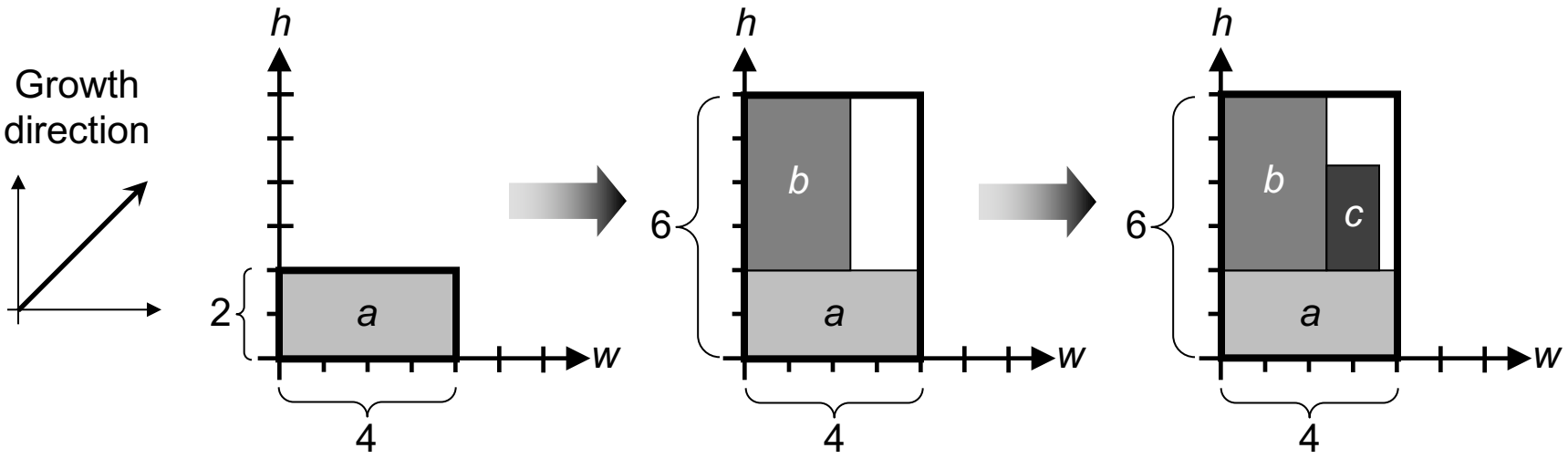
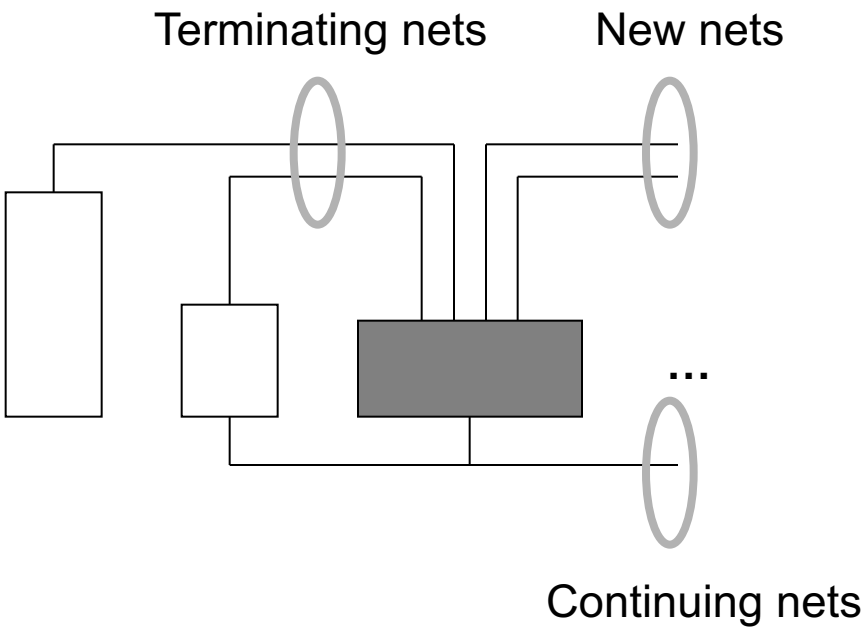
Cluster Growth

- Iteratively add blocks to the cluster until all blocks are assigned
- Only the different orientations of the blocks instead of the shape / aspect ratio are taken into account
- Linear ordering to minimize total wirelength of connections between blocks



Cluster Growth – Linear Ordering

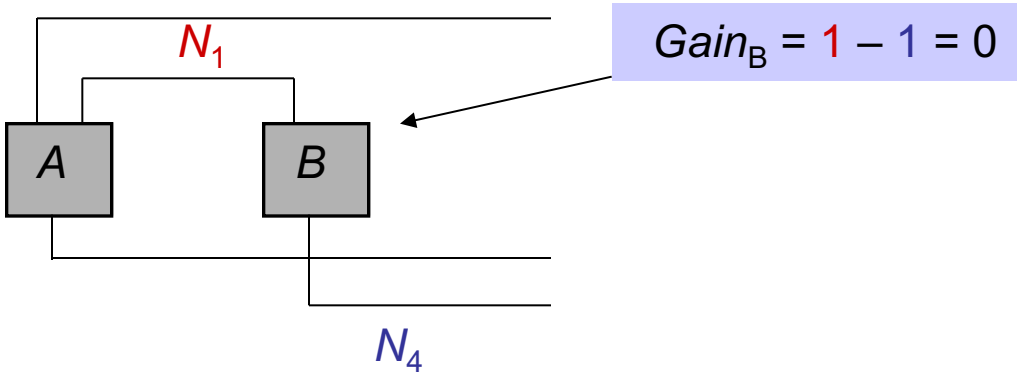
- New nets have no pins on any block from the partially-constructed ordering
- Terminating nets have no other incident blocks that are unplaced
- Continuing nets have at least one pin on a block from the partially-constructed ordering and at least one pin on an unordered block



Cluster Growth – Linear Ordering

- Gain of each block *m* is calculated:

  $Gain_m$ = (Number of terminating nets of *m*) – (New nets of *m*)

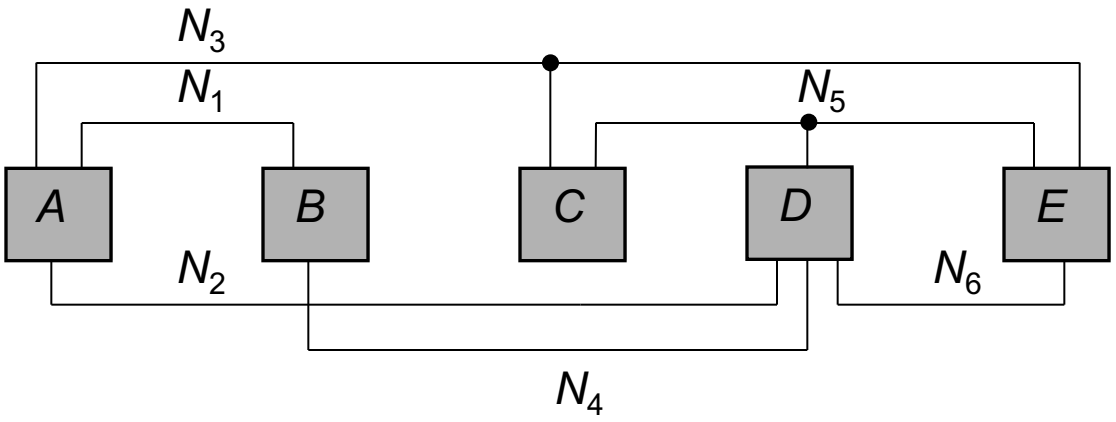


- The block with the maximum gain is selected to be placed next

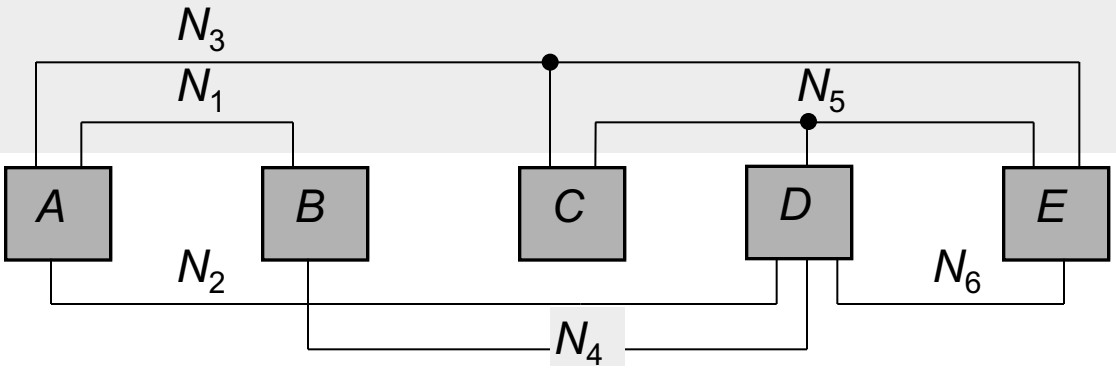
Cluster Growth – Linear Ordering (Example)

Given:

- Netlist with five blocks *A, B, C, D, E* and six nets
  $N_1 = \{A, B\}$
  $N_2 = \{A, D\}$
  $N_3 = \{A, C, E\}$
  $N_4 = \{B, D\}$
  $N_5 = \{C, D, E\}$
  $N_6 = \{D, E\}$
- Initial block: *A*



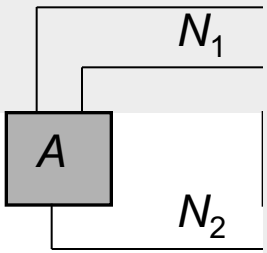
Task: Linear ordering with minimum netlength

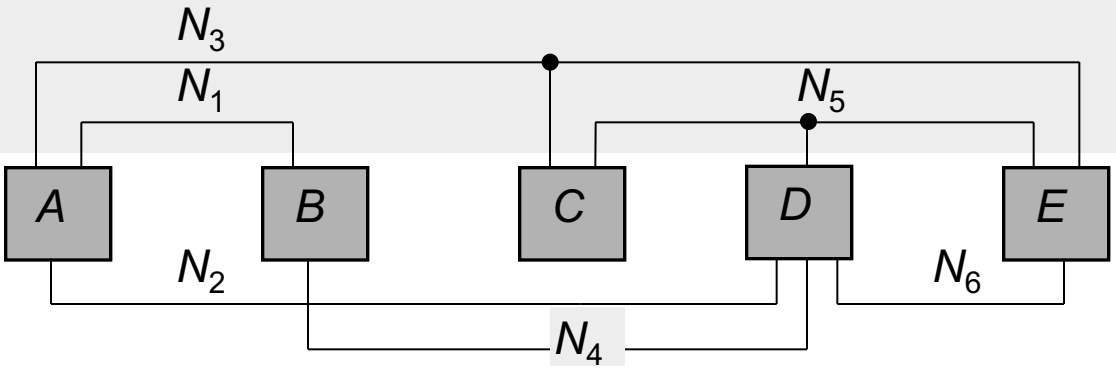


Iteration #	Block	New Nets	Terminating Nets	Gain	Continuing Nets
0	***A***	N_1,N_2,N_3	--	-3	--

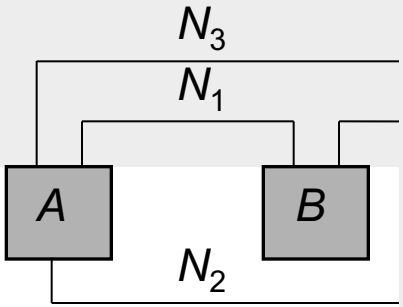
Initial block

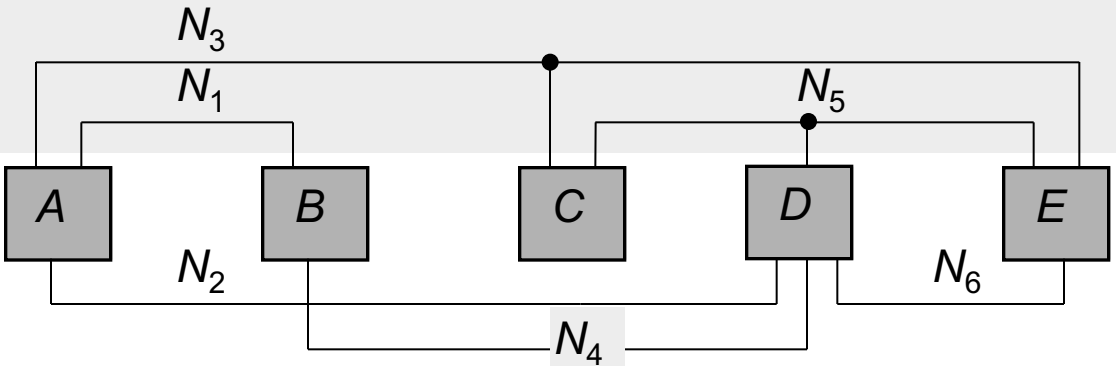
$Gain_A$ = (Number of terminating nets of *A*) – (New nets of *A*)



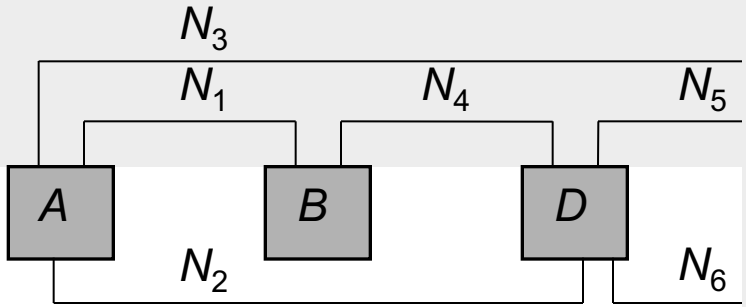


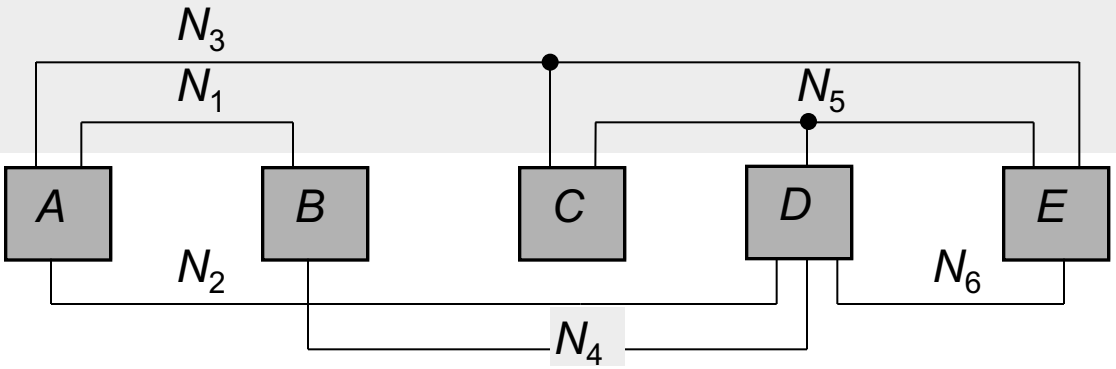
Iteration #	Block	New Nets	Terminating Nets	Gain	Continuing Nets
0	***A***	N_1,N_2,N_3	--	-3	--
1	***B***	N_4	N_1	0	--
	C	N_5	--	-1	N_3
	D	N_4,N_5,N_6	N_2	-2	--
	E	N_5,N_6	--	-2	N_3





Iteration #	Block	New Nets	Terminating Nets	Gain	Continuing Nets
0	***A***	N_1,N_2,N_3	--	-3	--
1	***B***	N_4	N_1	0	--
	C	N_5	--	-1	N_3
	D	N_4,N_5,N_6	N_2	-2	--
	E	N_5,N_6	--	-2	N_3
2	*C*	N_5	--	-1	N_3
	D	N_5,N_6	N_2,N_4	0	--
	E	N_5,N_6	--	-2	N_3





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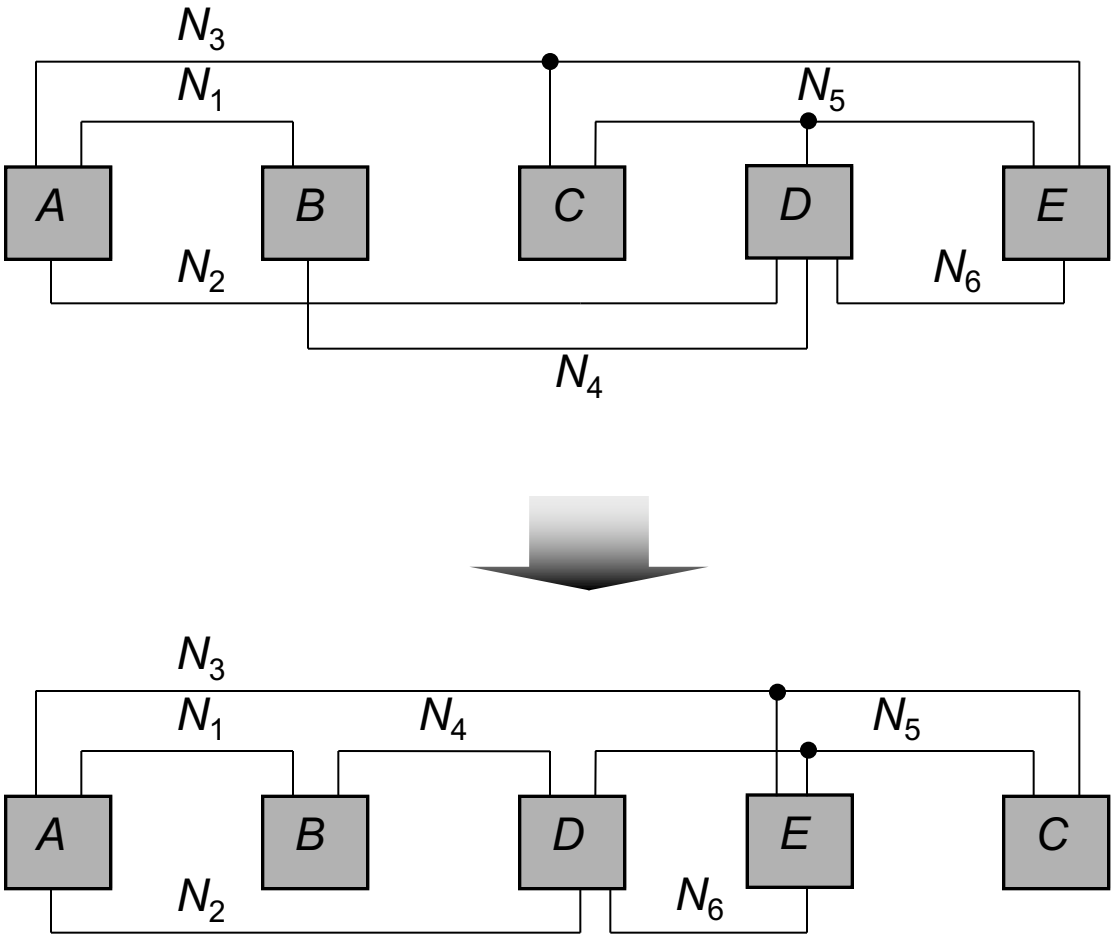
0	***A***	N_1,N_2,N_3	--	-3	--
1	***B***	N_4	N_1	0	--
	C	N_5	--	-1	N_3
	D	N_4,N_5,N_6	N_2	-2	--
	E	N_5,N_6	--	-2	N_3
2	*C*	N_5	--	-1	N_3
	D	N_5,N_6	N_2,N_4	0	--
	E	N_5,N_6	--	-2	N_3
3	*C*	--	--	0	N_3,N_5
	E	--	N_6	1	N_3,N_5

Cluster Growth – Linear Ordering (Example)



Cluster Growth – Algorithm

Input: set of all blocks *M*, cost function *C*
Output: optimized floorplan *F* based on *C*

```
F = Ø
order = LINEAR_ORDERING(M)                  // generate linear ordering
for (i = 1 to |order|)
    curr_block = order[i]
    ADD_TO_FLOORPLAN(F,curr_block,C)        // find location and orientation
                                            // of curr_block that causes
                                            // smallest increase based on
                                            // C while obeying constraints
```

Cluster Growth

Analysis

- The objective is to minimize the total wirelength of connections blocks
- Though this produces mediocre solutions, the algorithm is easy to implement and fast.
- Can be used to find the initial floorplan solutions for iterative algorithms such as *simulated annealing*.

Chip Planning

- Introduction

- Floorplanning Algorithms
  - Floorplan Sizing
  - Cluster Growth
  - Simulated Annealing

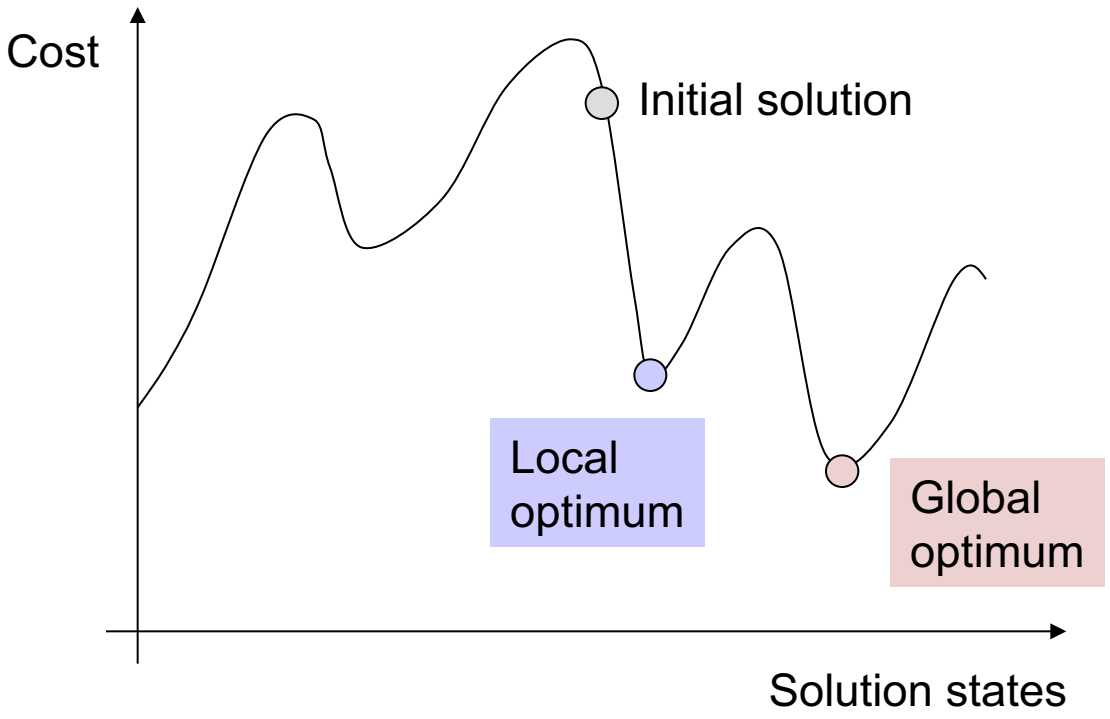
- Power and Ground Routing
  - Design of a Power-Ground Distribution Network
  - Planar Routing
    Mesh Routing

Simulated Annealing

Introduction

- Simulated Annealing (SA) algorithms are iterative in nature.
- Begins with an initial (arbitrary) solution and seeks to incrementally improve the objective function.
- During each iteration, a local neighborhood of the current solution is considered. A new candidate solution is formed by a small perturbation of the current solution.
- Unlike greedy algorithms, SA algorithms can accept candidate solutions with higher cost.

Simulated Annealing



Simulated Annealing

What is annealing?

- Definition (from material science): controlled cooling process of high-temperature materials to modify their properties.
- Cooling changes material structure from being highly randomized (chaotic) to being structured (stable).
- The way that atoms settle in low-temperature state is probabilistic in nature.

- Slower cooling has a higher probability of achieving a perfect lattice with minimum-energy
  - Cooling process occurs in steps
  - Atoms need enough time to try different structures
  - Sometimes, atoms may move across larger distances and create (intermediate) higher-energy states
  - Probability of the accepting higher-energy states decreases with temperature

Simulated Annealing

Simulated Annealing

- Generate an initial solution S_{init}, and evaluate its cost.
- Generate a new solution S_{new} by performing a random walk
- S_{new} is accepted or rejected based on the temperature T
  - Higher T means a higher probability to accept S_{new} if $COST(S_{new}) > COST(S_{init})$
  - T slowly decreases to form the final solution

- Boltzmann acceptance criterion, where r is a random number [0,1)

$$e^{\frac{COST(S_{init}) - COST(S_{new})}{T}} > r$$

Simulated Annealing

Simulated Annealing

- Generate an initial solution and evaluate its cost
- Generate a new solution by performing a random walk
- Solution is accepted or rejected based on a temperature parameter T
- Higher T indicates higher probability to accept a solution with higher cost
- T slowly decreases to form the finalized solution.

- Boltzmann acceptance criterion:

$$e^{-\frac{cost(curr_{sol})-cost(next_{sol})}{T}} > r$$

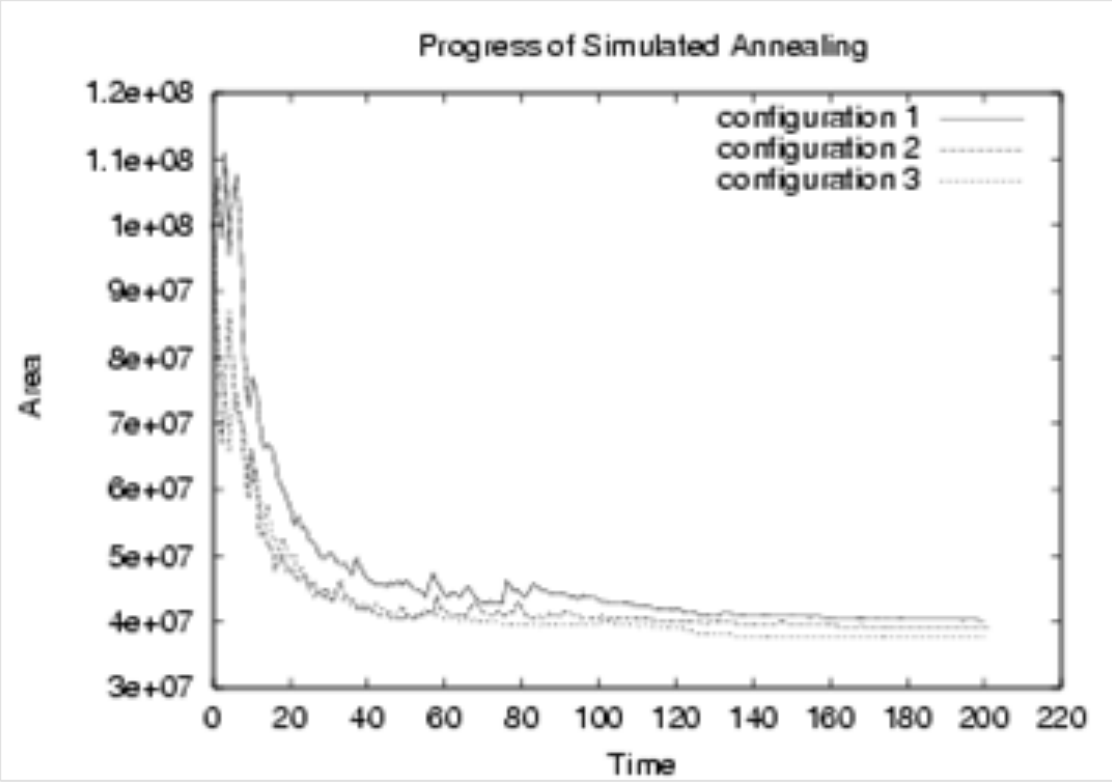
$curr_{sol}$: current solution

$next_{sol}$: new solution after perturbation

T: current temperature

r: random number between[0,1) from normal distr.

Simulated Annealing – Algorithm



Simulated Annealing – Algorithm

Input: initial solution *init_sol*
Output: optimized new solution *curr_sol*

```
T = T_0                                          // initialization
i = 0
curr_sol = init_sol
curr_cost = COST(curr_sol)
while (T > T_min)
    while (stopping criterion is not met)
    i = i + 1
    (a_i,b_i) = SELECT_PAIR(curr_sol)            // select two objects to perturb
    trial_sol = TRY_MOVE(a_i,b_i)                // try small local change
    trial_cost = COST(trial_sol)
    Δcost = trial_cost – curr_cost
    if (Δcost < 0)                               // if there is improvement,
                curr_cost = trial_cost           //  update the cost and
                curr_sol = MOVE(a_i,b_i)         //  execute the move
    else
                r = RANDOM(0,1)                  // random number [0,1]
                if (r < e^(−Δcost/T))            // if it meets threshold,
                     curr_cost = trial_cost      //   update the cost and
                     curr_sol = MOVE(a_i,b_i)    //   execute the move
    T = α · T                                    // 0 < α < 1, T reduction
```

Chip Planning

- Introduction
- Floorplanning Algorithms
  - Floorplan Sizing
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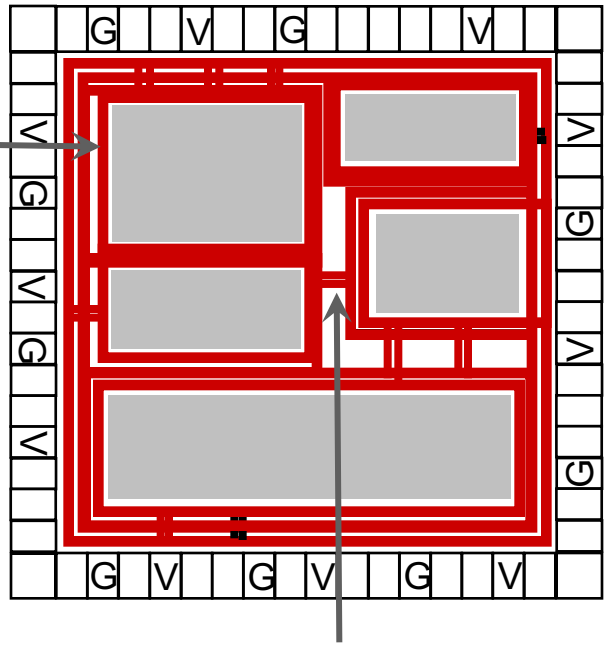
  - Simulated Annealing
- **Power and Ground Routing**
  - Design of a Power-Ground Distribution Network
  - Planar Routing
    - Mesh Routing

Power and Ground Routing

Power-ground distribution for a chip floorplan

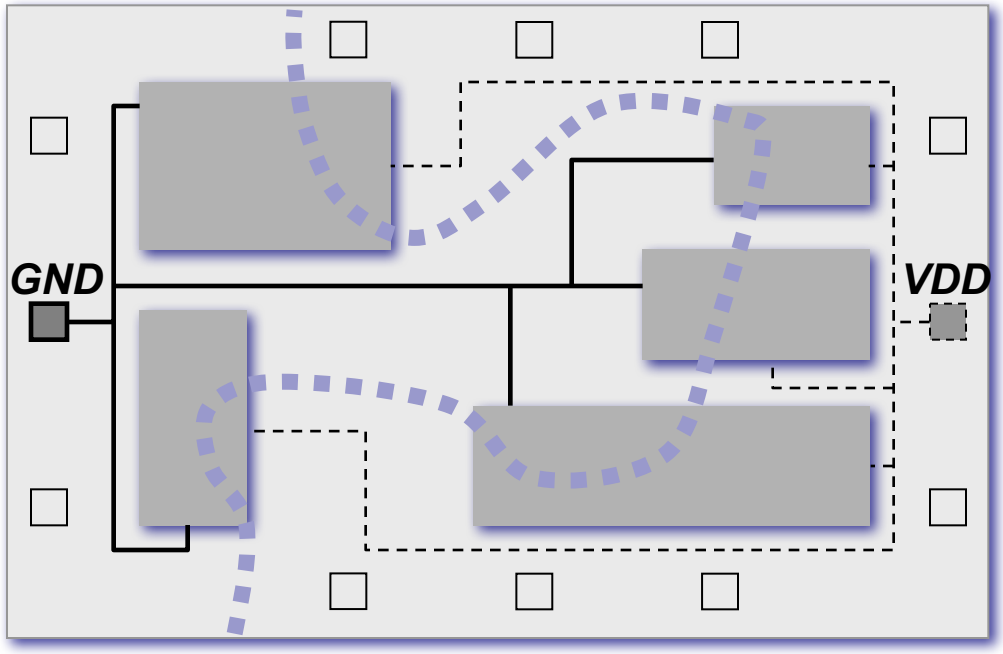
Power and ground rings per block or abutted blocks



Trunks connect rings to each other or to top-level power ring

Power and Ground Routing

Planar routing



Hamiltonian path

Power and Ground Routing

Planar routing

Step 1: Planarize the topology of the nets

- As both power and ground nets must be routed on one layer, the design should be split using the Hamiltonian path

Step 2: Layer assignment

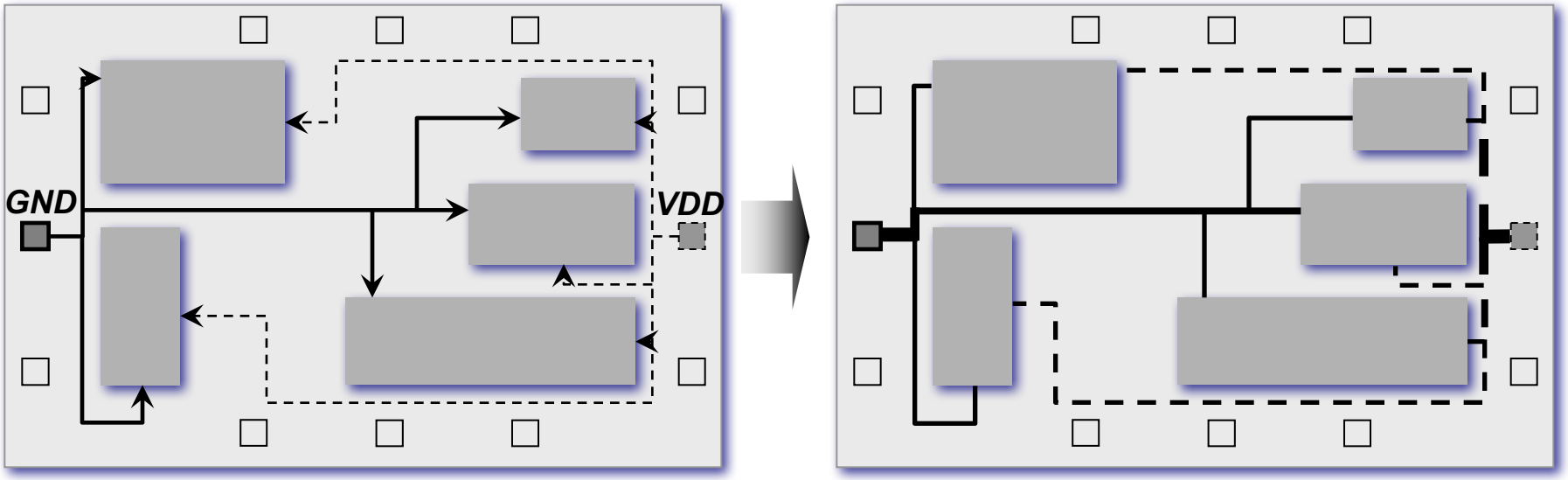
- Net segments are assigned to appropriate routing layers

Step 3: Determining the widths of the net segments

- A segment's width is determined from the sum of the currents from all the cells to which it connects

Power and Ground Routing

Planar routing



Generating topology
of the two supply nets

Adjusting widths of the segments
with regard to their current loads

Power and Ground Routing

Mesh routing

Step 1: Creating a ring

- A ring is constructed to surround the entire core area of the chip, and possibly individual blocks.

Step 2: Connecting I/O pads to the ring

Step 3: Creating a mesh

- A power mesh consists of a set of stripes at defined pitches on two or more layers

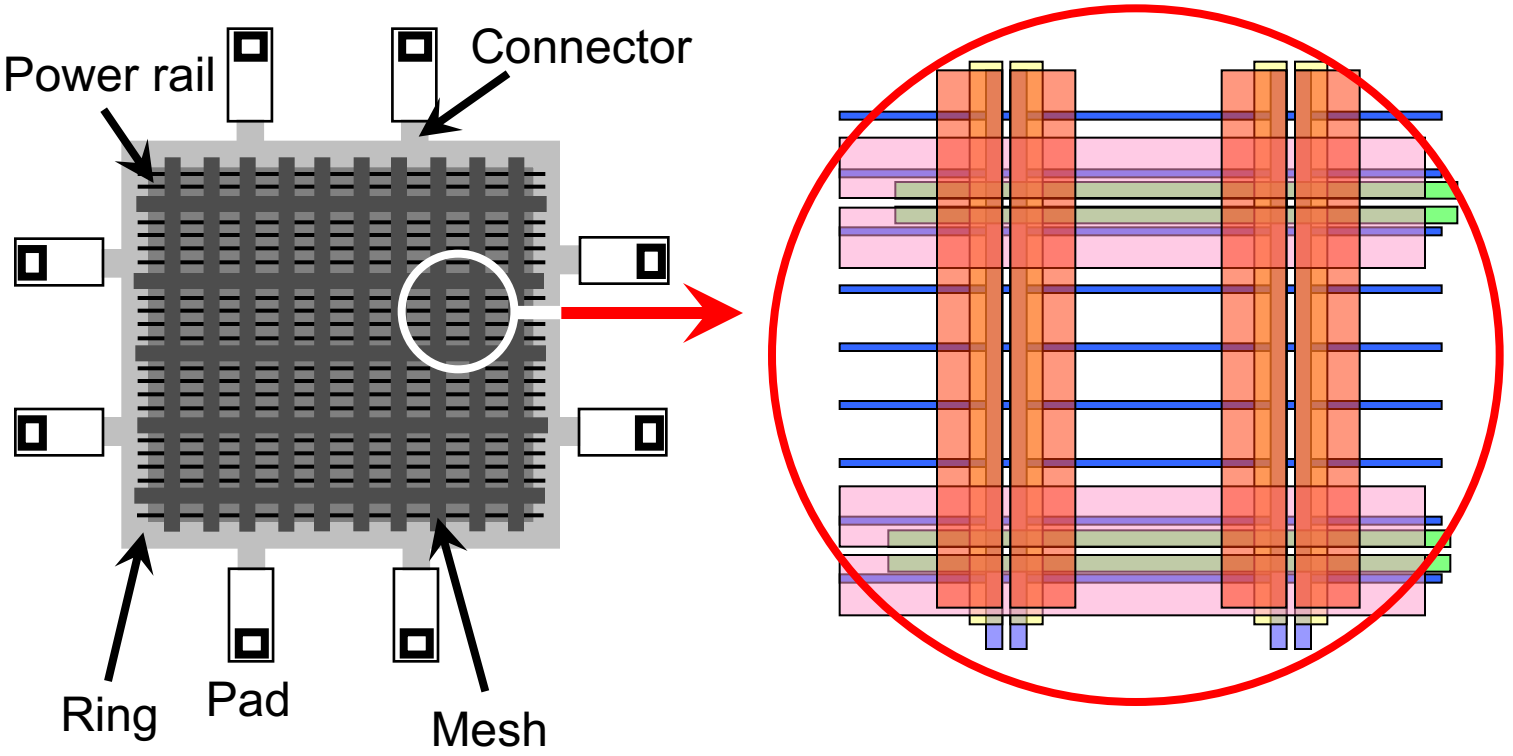
Step 4: Creating Metal1 rails

- Power mesh consists of a set of stripes at defined pitches on two or more layers

Step 5: Connecting the Metal1 rails to the mesh

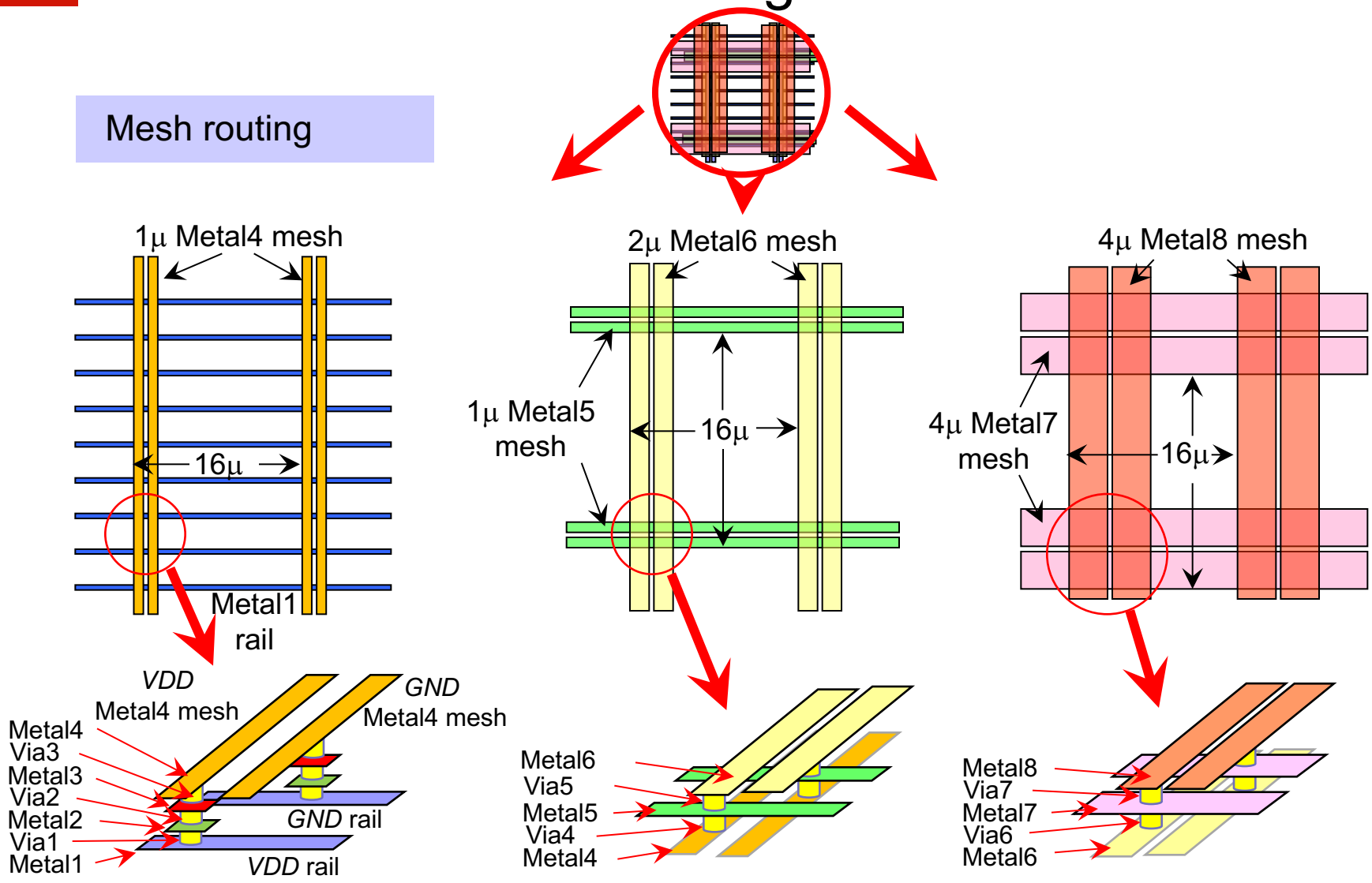
Power and Ground Routing

Mesh routing



Power and Ground Routing

Mesh routing



M1-to-M4 connection **M4-to-M6 connection** **M6-to-M8 connection**

Summary

- Traditional floorplanning
  - Assumes area estimates for top-level circuit modules
  - Determines shapes and locations of circuit modules
  - Minimizes chip area and length of global interconnect
- Additional aspects
  - Assigning/placing I/O pads
  - Defining channels between blocks for routing and buffering
  - Design of power and ground networks
  - Estimation and optimization of chip timing and routing congestion
- Fixed-outline floorplanning
  - Chip size is fixed, focus on interconnect optimization
  - Can be applied to individual chip partitions (hierarchically)
- Structure and types of floorplans
  - Slicing versus non-slicing, the wheels
  - Hierarchical
  - Packed
  - Zero-deadspace

Summary - Data Structures for Floorplanning

- Slicing trees and Polish expressions
  - Evaluating a floorplan represented by a Polish expression
- Horizontal and vertical constraint graphs
  - A data structure to capture (non-slicing) floorplans
  - Longest paths determine floorplan dimensions
- Floorplan sizing
  - Shape-function arithmetic

Summary - Algorithms for Floorplanning

- Floorplan Slicing - An algorithm for slicing floorplans
- Cluster growth
  - Simple, fast and intuitive
  - Not competitive in practice
- Simulated annealing
  - Stochastic optimization with hill-climbing
  - Many details required for high-quality implementation (e.g., temperature schedule)
  - Difficult to debug, fairly slow
  - Competitive in practice
- Power and ground routing
  - Planar routing in channels between blocks
  - Can form rings around blocks to increase current supplied and to improve reliability
  - Mesh routing