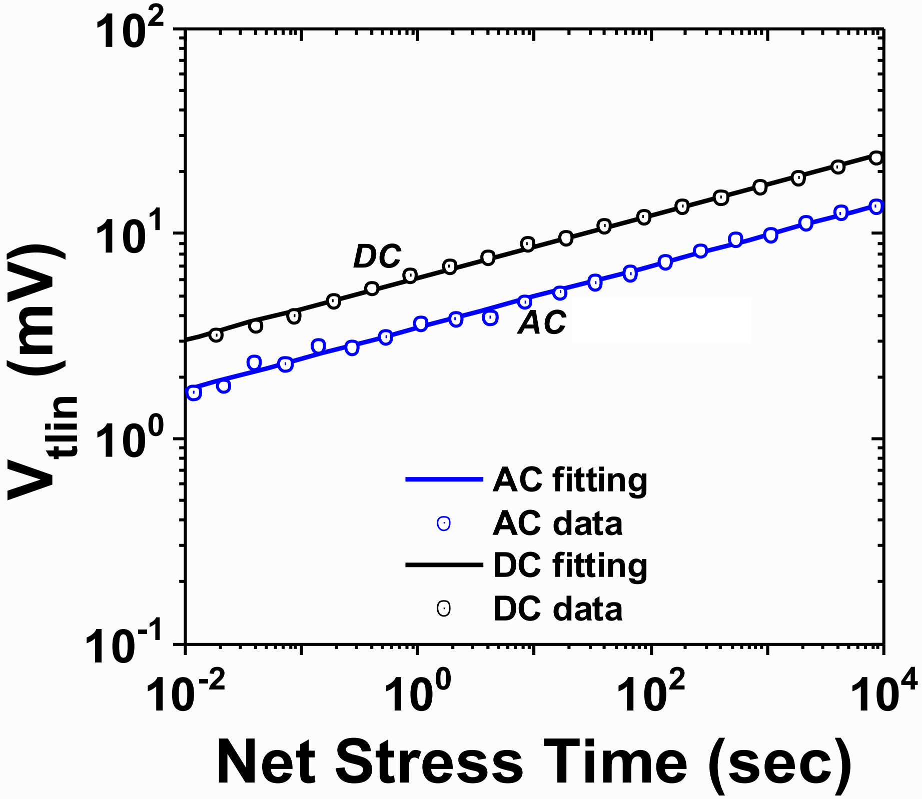
FET characteristics and BTI

- Threshold voltage (V_T)
- Current degradation approximately corresponds to V_T degradation
- Known sensitivities
  - PBTI is *more* sens. to Voltage
  - NBTI is *more* sens. to temperature
- Semi-empirical model (for both NBTI and PBTI)

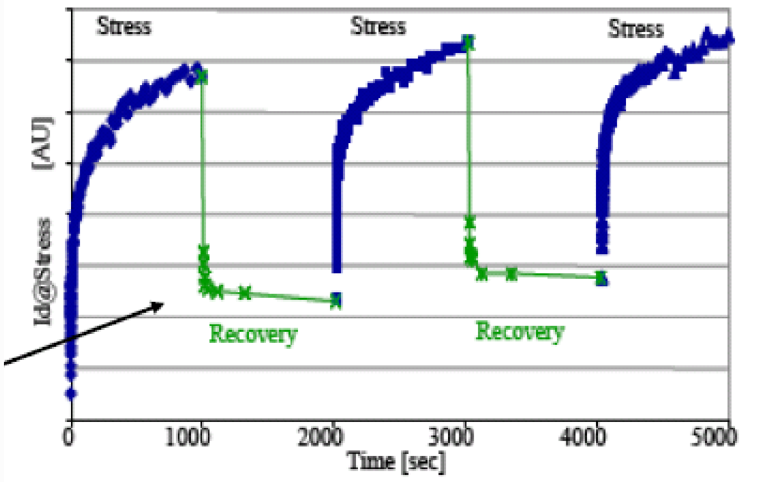


$$V_T\,|_{DC\_stress} = A V_{DD}^{a} T^{b} t^{n}$$ *(without including recovery)*

Recovery after stress

Static stress and recovery or "0.001 Hz waveform"

*Ramey et. al., Intel, IRPS 2009



- **Recovery happens when FET is OFF**

$$V_T\,|_{after\_relax} = FR\text{x}\quad V_T\,|_{DC\_stress}$$

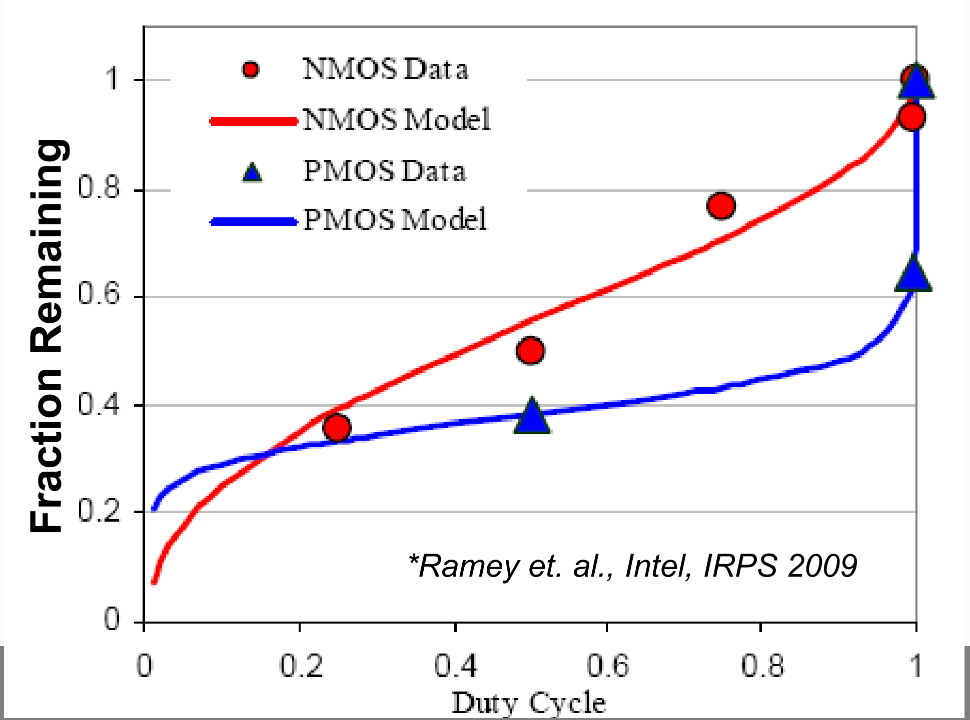
Fraction Remaining

$$FR = 1 + \frac{t_{relax}}{t_{stress}}{}^{n}{}^{1}$$

- In other words, if probability of '1' at the gate of an NFET is say P_1, then,

$$\text{duty\_cycle} = \frac{t_{\text{stress}}}{t_{\text{stress}} + t_{\text{relax}}} = P_1$$

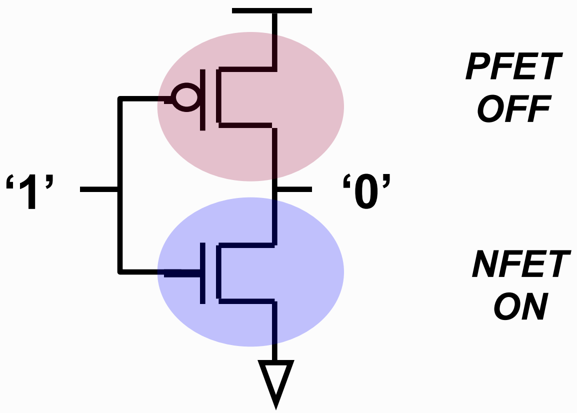
- **Biggest benefits of recovery when duty_cycle < 95%**

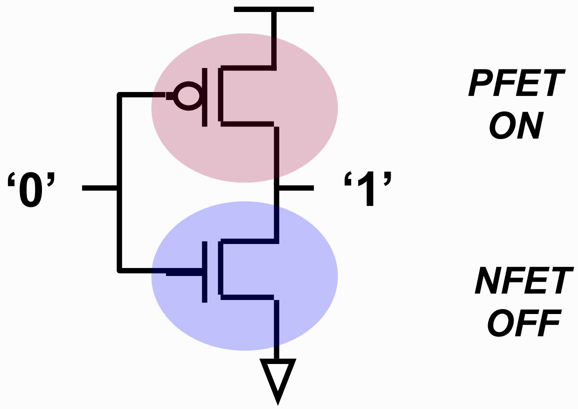


*Ramey et. al., Intel, IRPS 2009

FET stress-recovery

Let’s take an example of simple CMOS inverter





PFET is relaxing: Gate-source HIGH and drain LOW

NFET is stressed: Gate is HIGH and source-drain LOW

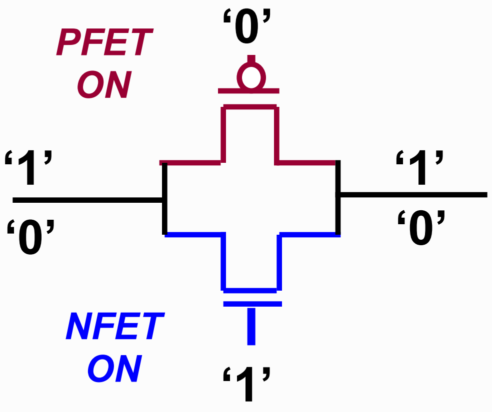
PFET is stressed: Gate is LOW and source-drain HIGH

NFET is relaxing: Gate-source LOW and drain HIGH

- If a FET is ON, it’s stressed (for both NFET and PFET)
- If a FET is OFF, it’s relaxed (for both NFET and PFET)

FET stress-recovery

For other circuit types say transmission gate



PFET ON

‘0’

‘1’

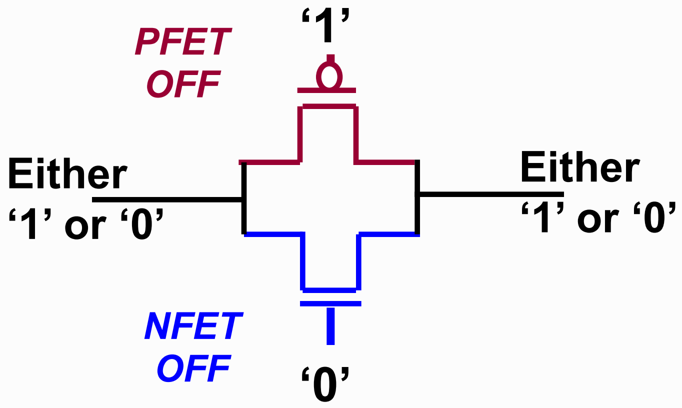
‘0’

‘1’

‘0’

NFET ON

‘1’



PFET OFF

‘1’

Either
‘1’ or ‘0’

Either
‘1’ or ‘0’

NFET OFF

‘0’

- Both the FETs are either ON or OFF together

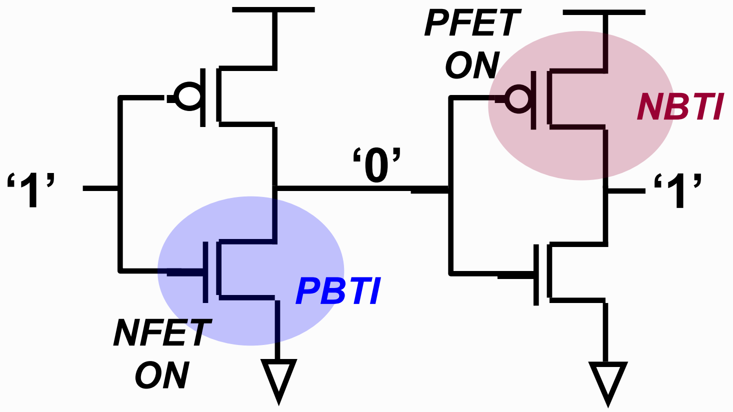
- Source-drain voltages during relaxation depends on other circuit blocks on left and right

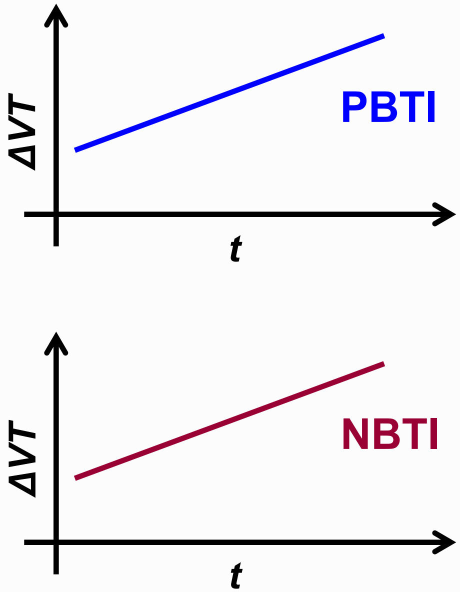
  - e.g., negative gate-drain or gate-source voltage in NFET may speed up recovery (also true for inverter on previous slide)

Nature of Stresses/recovery

Static or DC stress

- FETs are in the same voltage bias condition during the USAGE





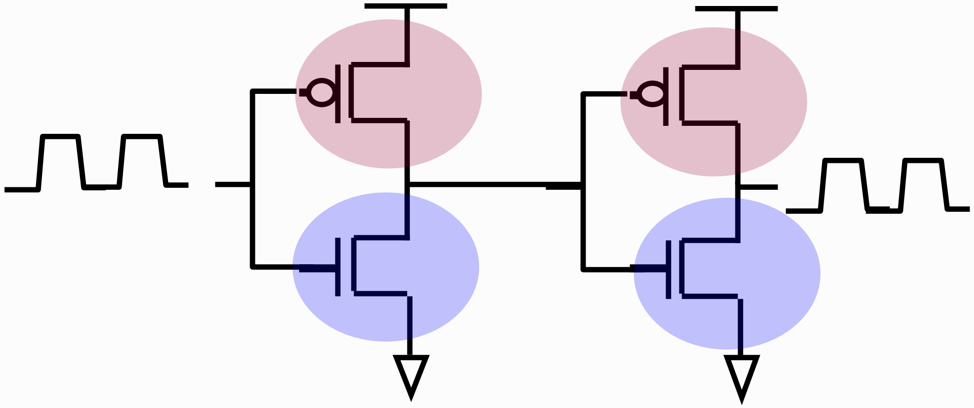
Examples:

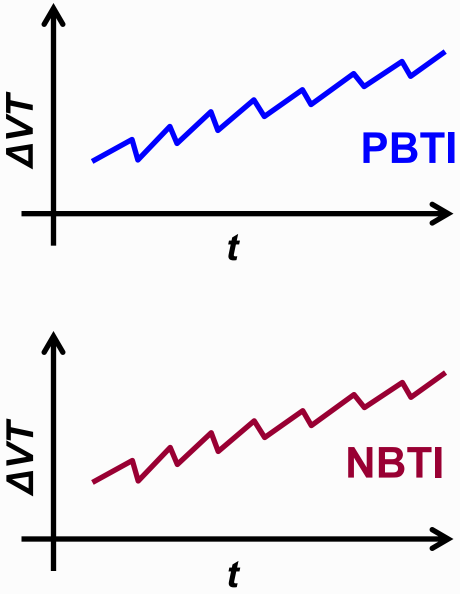
- **SRAM cells storing the same data for long time**
- **Circuit paths not used for long time but powered on**
  - **Word line drivers, local and global eval circuits**

Nature of Stresses/recovery

Alternating or AC stress

- FETs turn ON (stress) and OFF (recover) during the USAGE
- It's composed of several DC stress and recovery conditions
- Durations of stress and recovery depend on nature of program running and typically can not be estimated





Examples:

–SRAM cells frequently changing the stored data

–Logic circuit paths doing computations

Question

❑ The bias temperature instability device degradation in a circuit can be reduced by

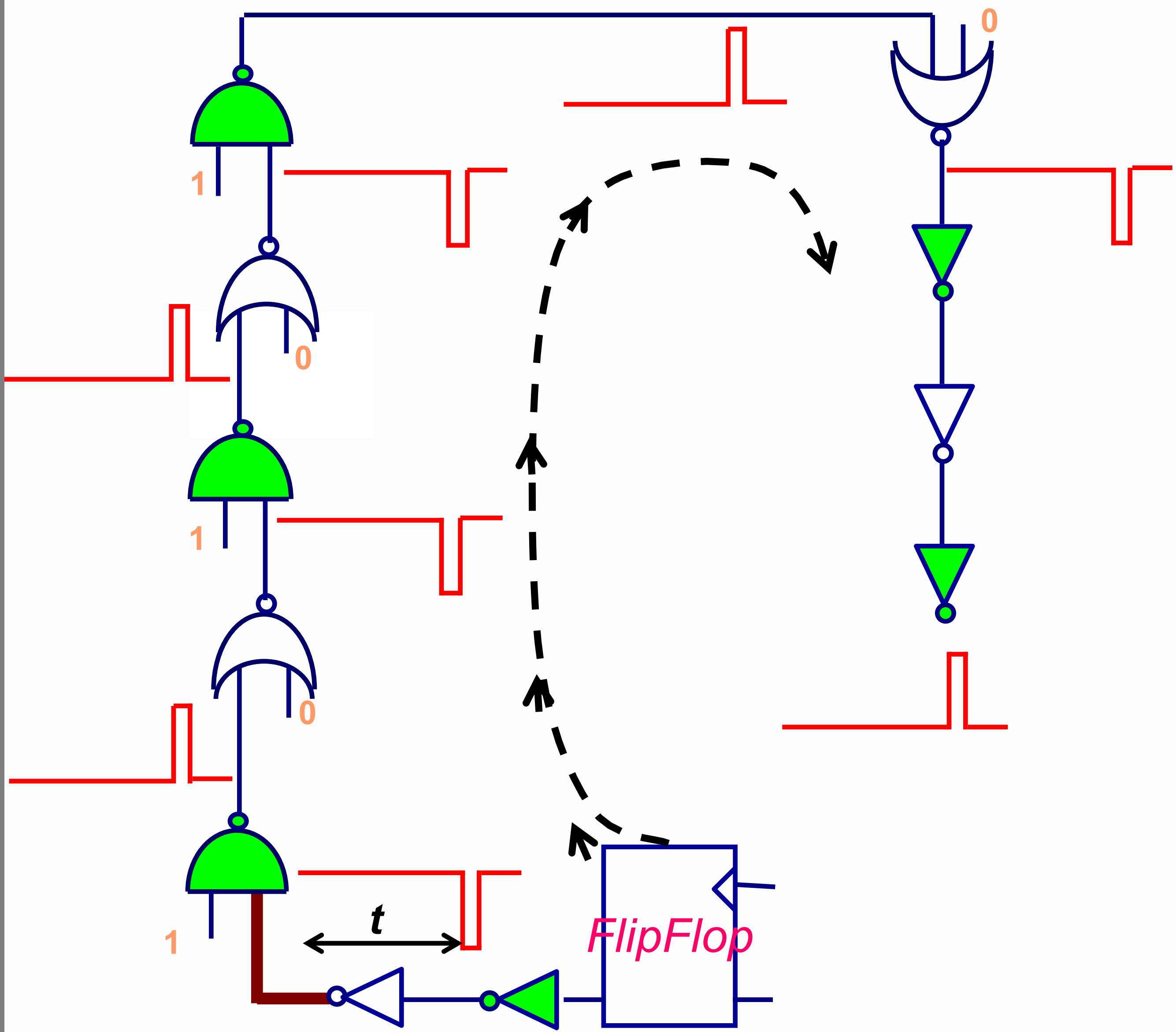
a) Using assymmetric transistors since they will degrade at different rates

b) Avoiding pass gates in the design and always using transmission gates

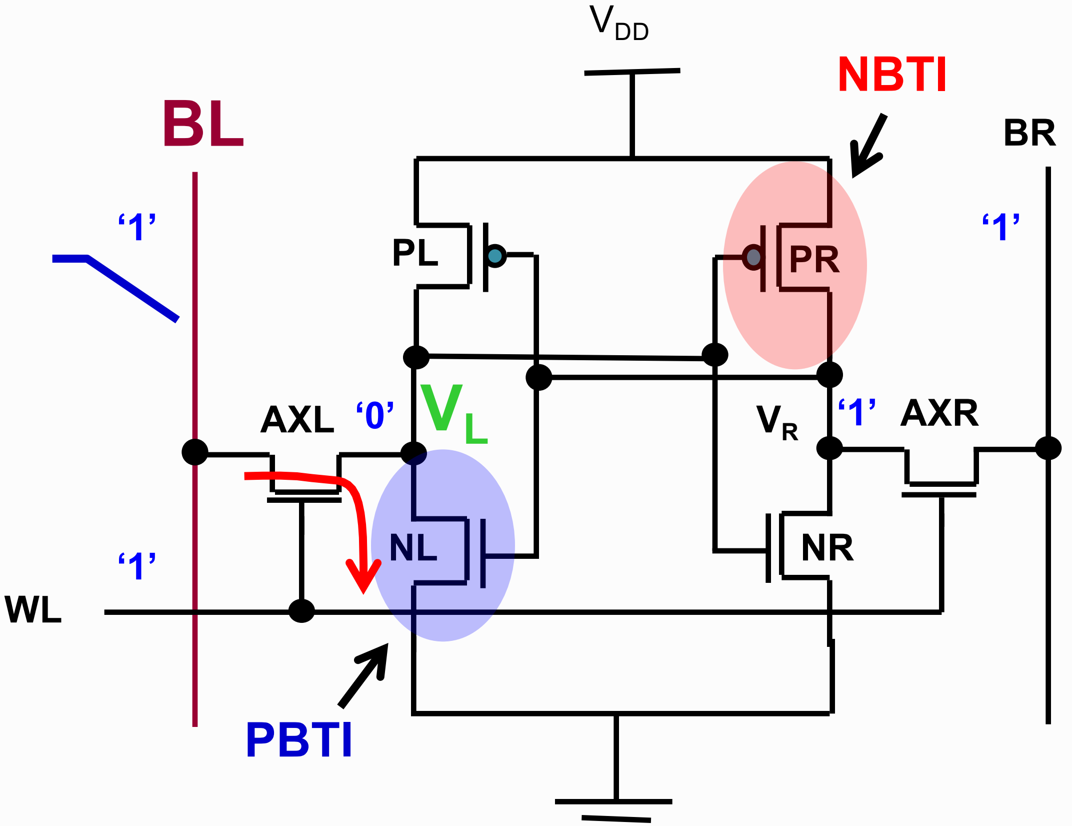
c) Increasing the supply voltage of the circuit

d) Ensuring that all nodes in a circuit switch every N cycles

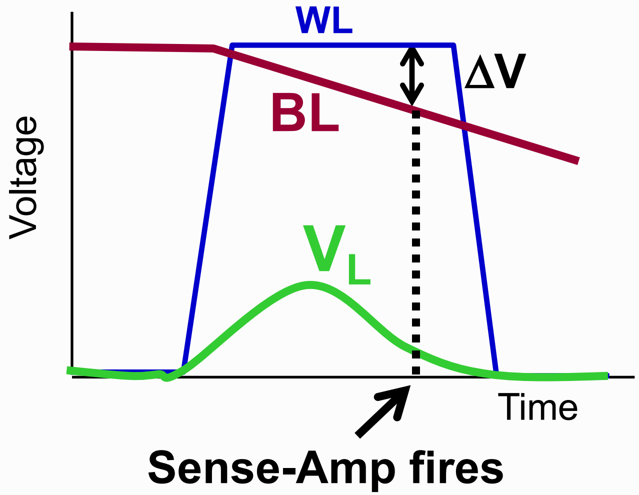
Timing Failure due to BTI



SRAM Operating Mode: READ



BL and BR are pre-charged to VDD and then left hanging

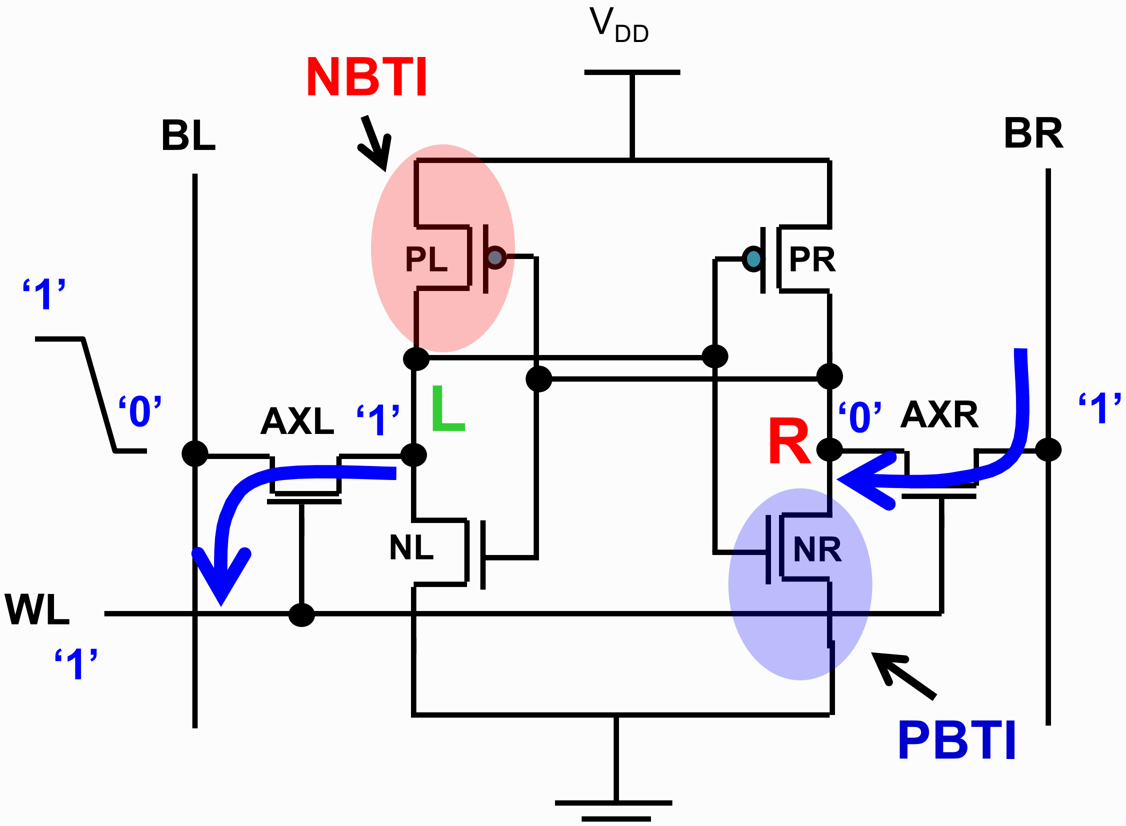


Access FETs (AXL & AXR) are ON for short duration while cell is accessed => assumed negligible degradation

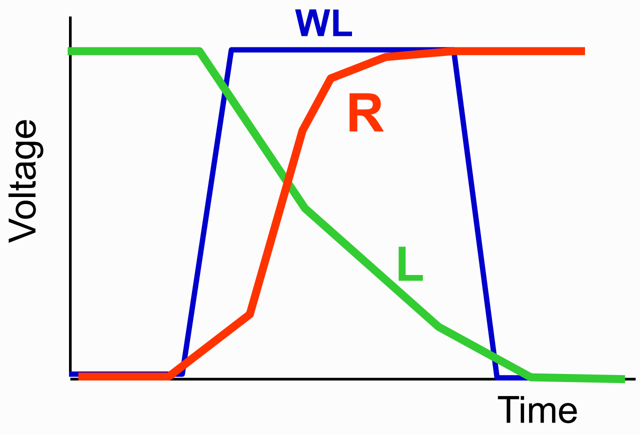
- **The data stored should *not* flip during READ**
  => NL (NR) should be stronger than AXL (AXR): *PBTI can make NL weak (bad!)*
- **Sufficient ΔV to fire SA should be developed while WL = '1'**
  => AXL-NL should fast discharge BL: *Weak NL will slow discharge (bad!)*

(A. Bansal, MicroReliability 2009)

SRAM Operating Mode: WRITE



BL and BR are FIXED to data



Weak cross-coupled inverters (NL-PL and NR-PR) are good for writing

- **The data stored *must* flip during WRITE**

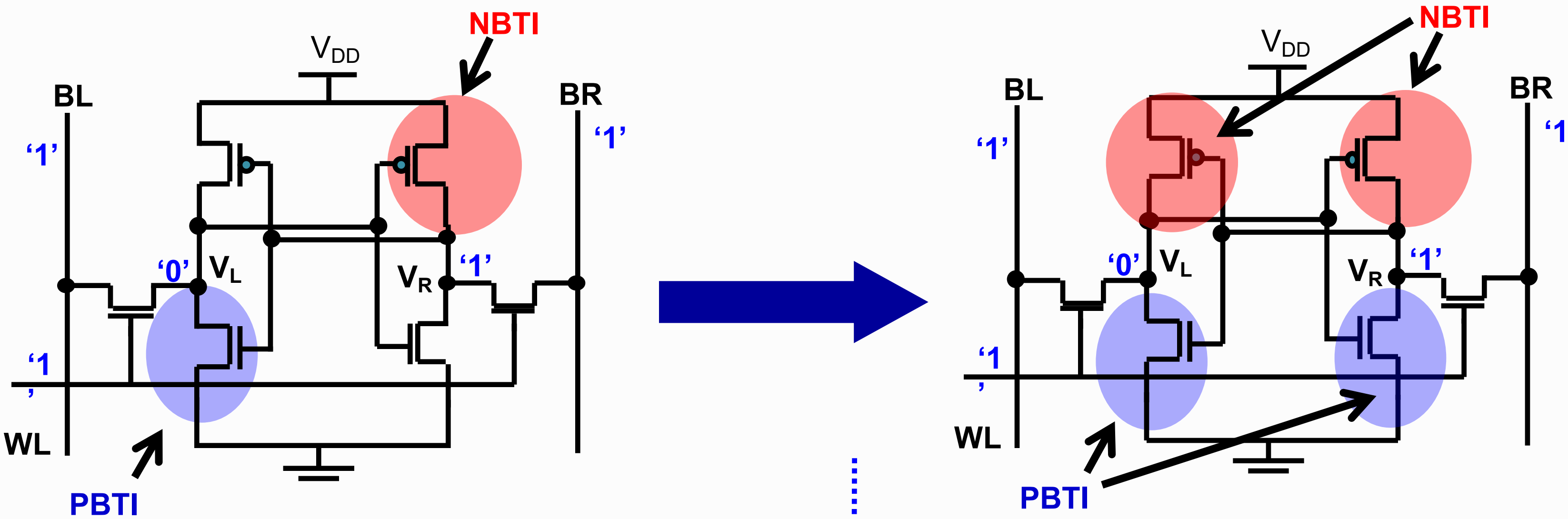
=> AXL (AXR) should be stronger than PL (NR) *NBTI (PBTI) can make PL (NR) weak (good!)*

- **Data should flip while WL = '1'**

=> *WL pulse width increased (good)*

(A. Bansal, MicroReliability 2009)

Static and Alternating Stress



Static Stress

- Cell is storing same data for long time => asymmetric
- May be *READ* multiple times but not flipped
- ΔVt for static stress larger than alternating stress (no recovery)
- READ gradually becomes unstable
- Increases READ access time

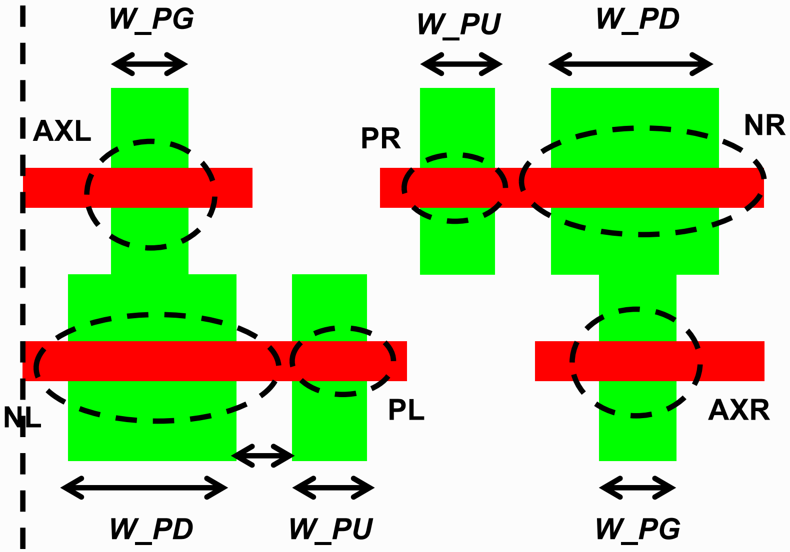
Alternating Stress

- Cell is regularly flipped => symmetric
- Equal time/relaxation for storing '1' and '0' to maintain symmetry
- ΔVt for same usage is less (low power-on time)
- β-ratio between pull-down and pass-gate FETs varies => PD weakens and READ fail increases
- Increases READ access time

➢Typically all cells in between Static to Alternating stress

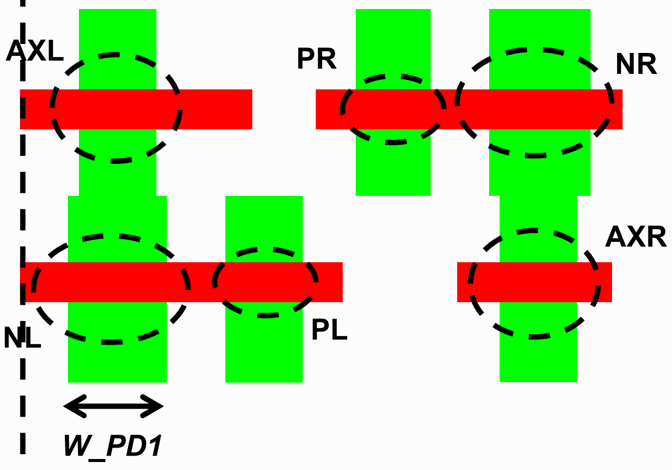
(A. Bansal, MicroReliability 2009)

High Performance vs Dense Cells



High-Performance and READ stable

- $W_{PD} >> W_{PG}$ for READ stability
- Low READ access time
- Large cell footprint
- Less RDF induced V_T fluctuation in PD
- Microprocessors etc.

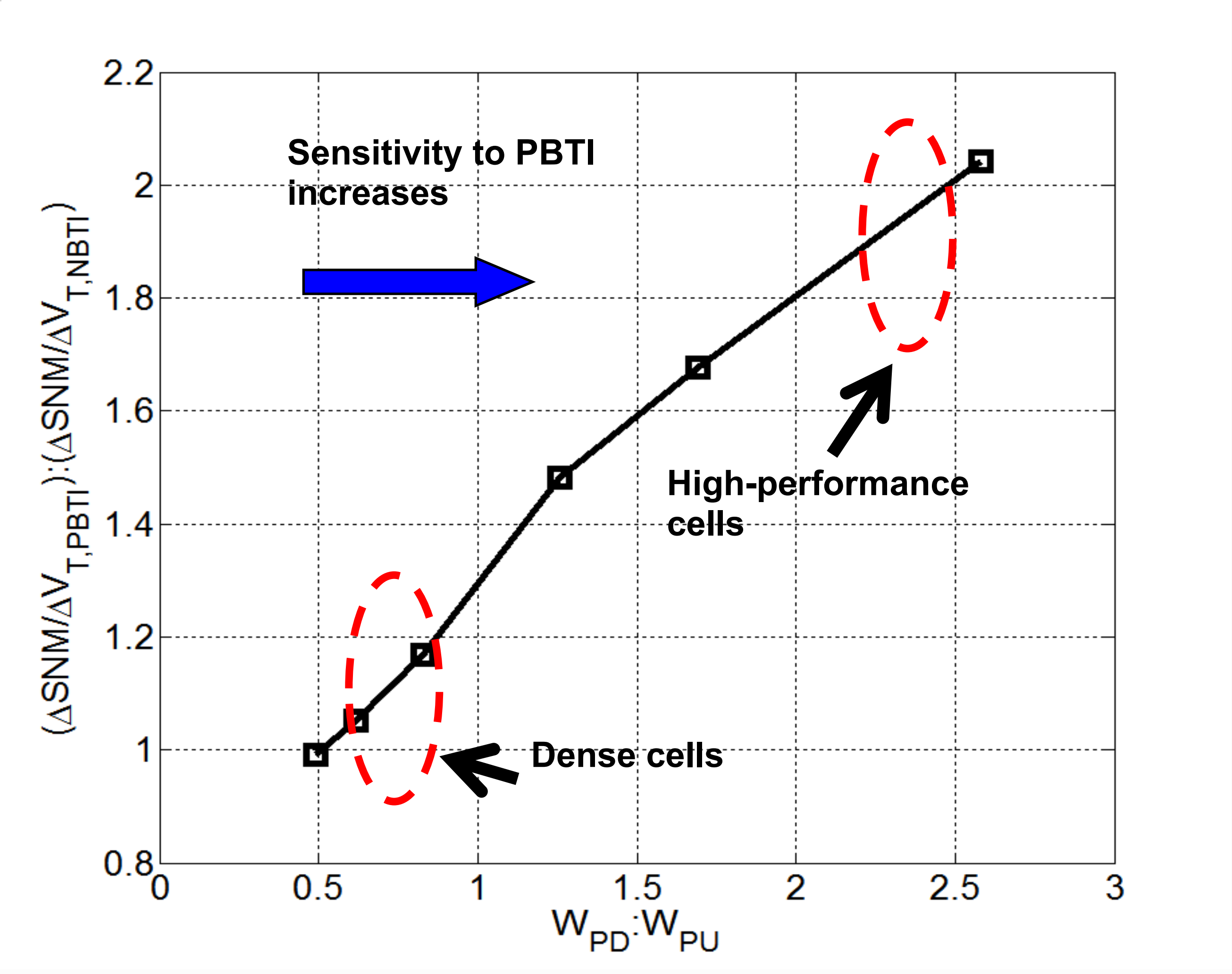


Dense and WRITE stable

- $W_{PD} \sim W_{PG}$ for WRITE stability
- Large READ access time
- Small cell footprint
- Large RDF induced V_T fluctuation in PD
- Dense applications – PDA etc.

(A. Bansal, IRPS 2009)

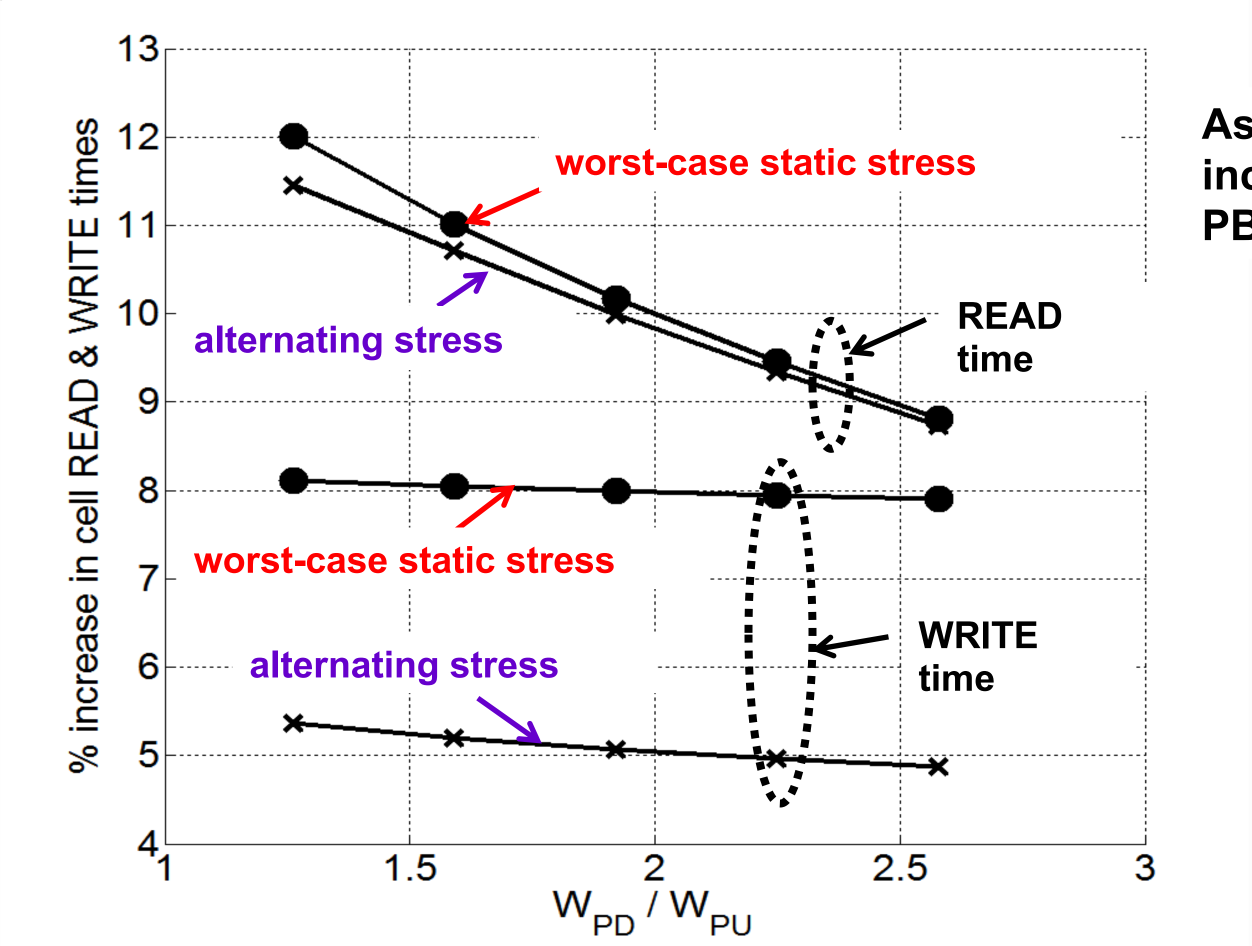
What happens when W_{PD} is scaled?



As W_{PD} / W_{PU} increases, a cell becomes *more* sensitive to PBTI than NBTI

(A. Bansal, IRPS 2009)

Impact on Cell READ and WRITE time

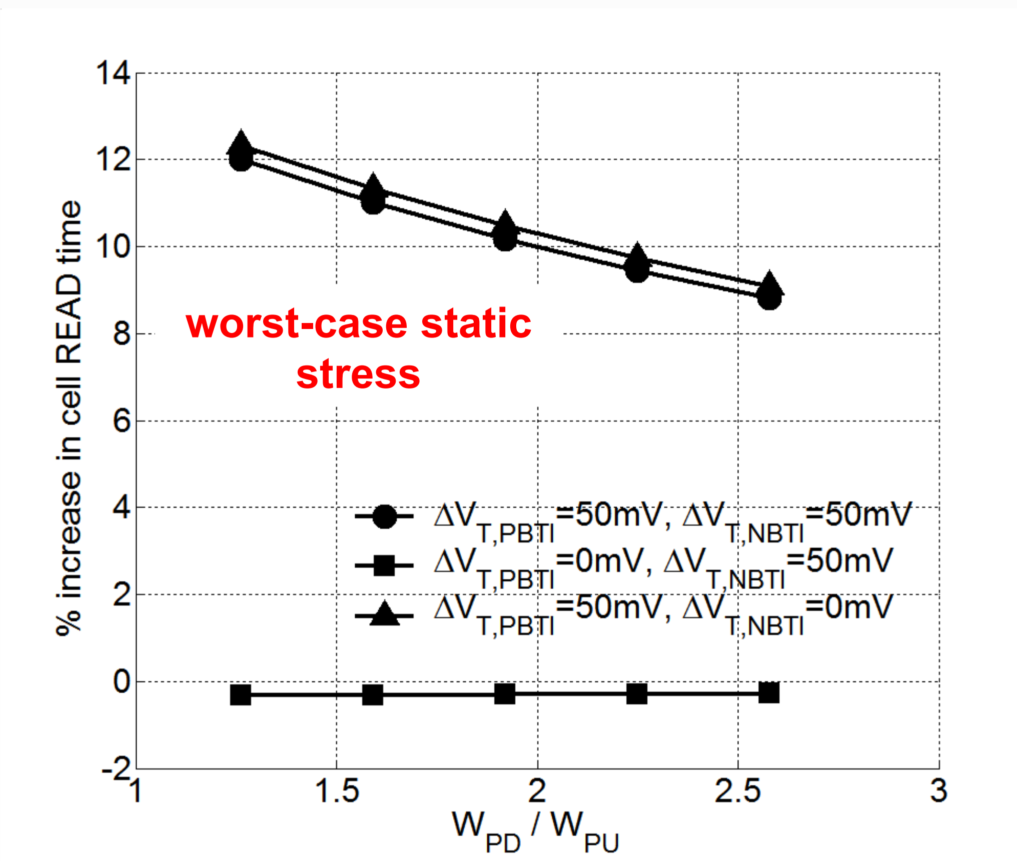


Assuming $\Delta V_T = 50mV$ increase due to NBTI and PBTI at end-of-life

- **READ time reduces as we go from dense to high-performance cell**
- **READ time is *less* dependent on stress condition**

(A. Bansal, IRPS 2009)

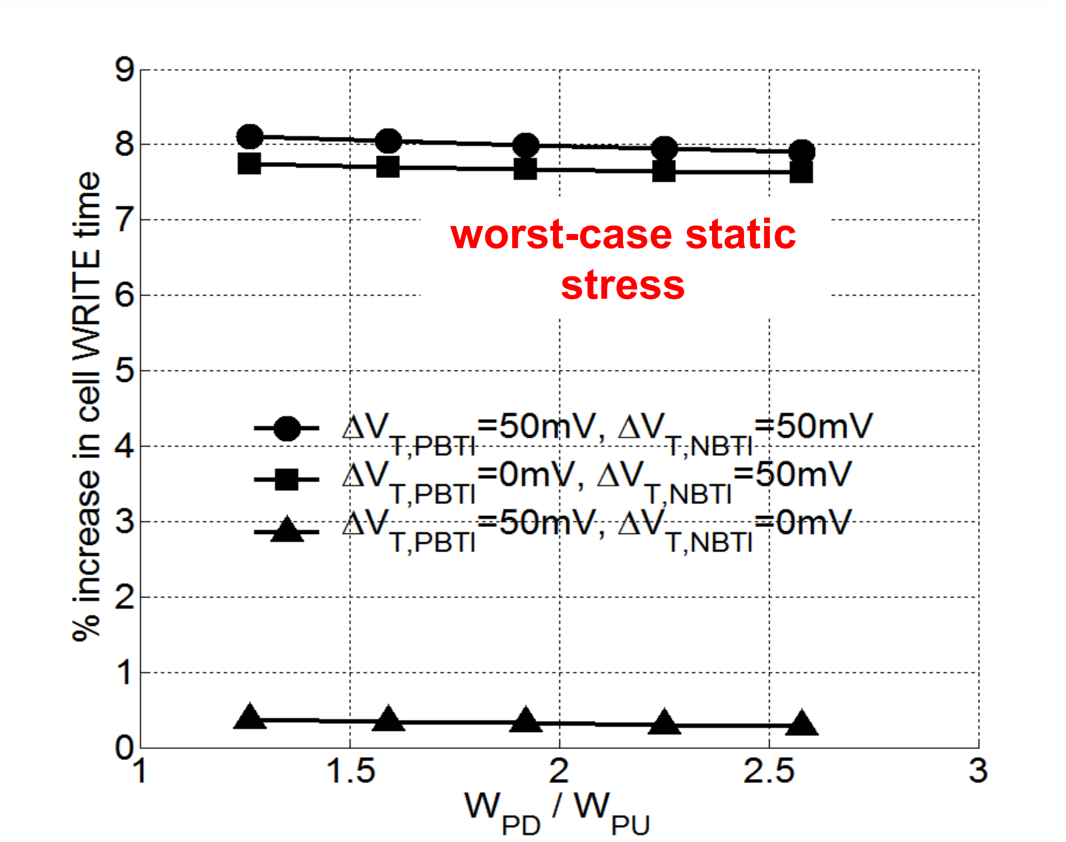
READ access time



- **READ time is *practically immune* to NBTI**
- **READ time degrades ~ 9-12% for 50mV V_T shift due to PBTI**
- ***Stringent PBTI requirements in high-performance cells***

(A. Bansal, IRPS 2009)

WRITE time



worst-case static stress

- **WRITE time is *practically immune* to PBTI**
- **WRITE time degrades ~ 8% for 50mV V_T shift due to NBTI**
- ***Similar NBTI requirements in high-performance and dense cells***

(A. Bansal, IRPS 2009)

Question

❑ A 8-T SRAM cell that was operation at time t = 0, will not see the following at time t = 5 years due to BTI

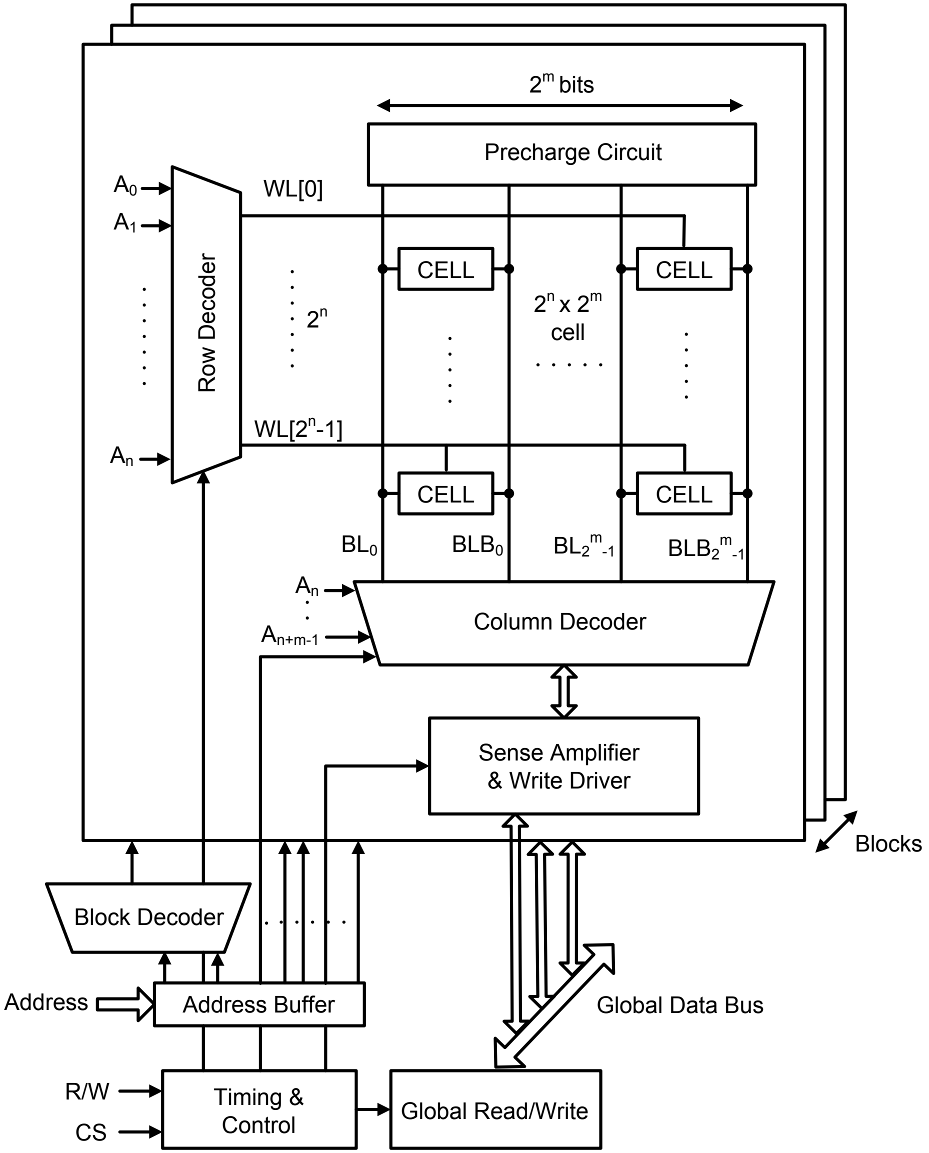
a) Access failures increasing due to NBTI

b) Write failures increasing due to the combination of NBTI and PBTI

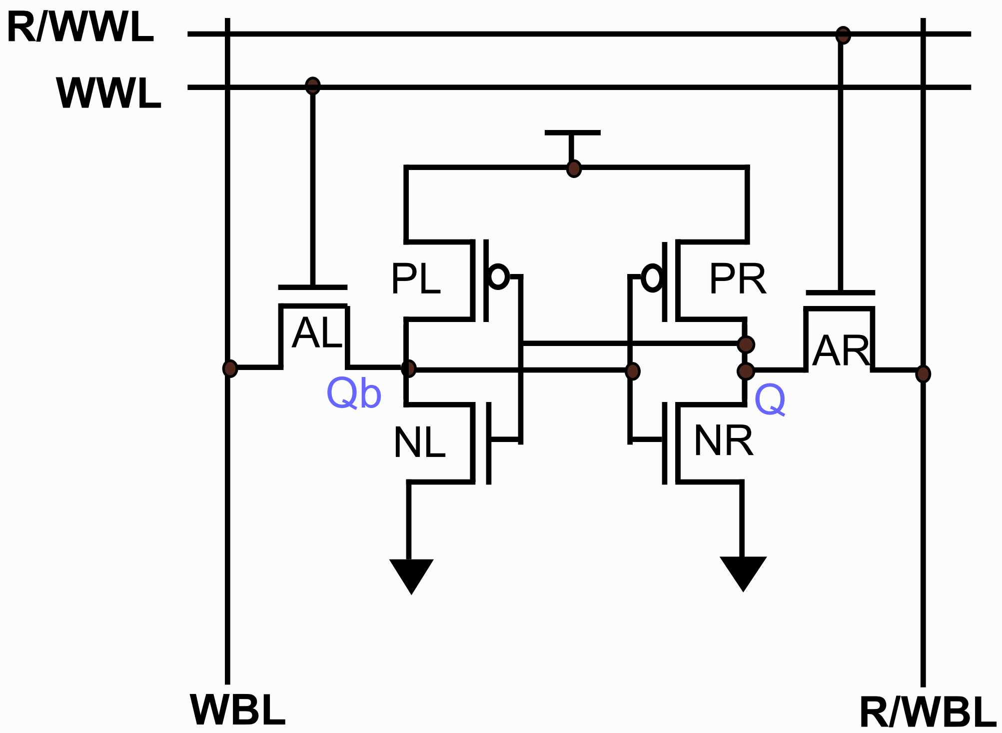
c) Read failures increasing due to PBTI

d) Hold failures increasing due to the combination of NBTI and PBTI

Block Diagram



Read and Write Patterns



Question

❑ Which of the following loops is a worst case access pattern (from a power point of view)

- Write AAAA to address 5
- Write 5555 to address A
- Read address A
- Read address 5

- Write 1234 to address 0
- Write 5678 to address 7
- Read address 0
- Read address 7

- Read address A
- Write AAAA to address A
- Read address 5
- Write 5555 to address 5

- Write AAAA to address F

  Write 7777 to address A
- Read address F
- Read address 5

Test

❑ Defect vs Fault

- Defect => A deviation from intended behavior
- Fault => A model for the defect

❑ Structural vs Functional Test

- Structural Test => Testing all nodes of the circuits
- Functional Test => Behaves as desired

❑ Verification vs Test

- Verification => Design is correct
- Test => Hardware is correct

Test

❑ Stuck At Faults => Cell is stuck at a particular value

❑ Transition Faults => Cell fails to undergo a particular transition

❑ Coupling Faults => Cell (v) fails due to Cell (a)

❑ Pattern Faults => Cell (v) fails due to a multiple set of Cells (a1 – an)

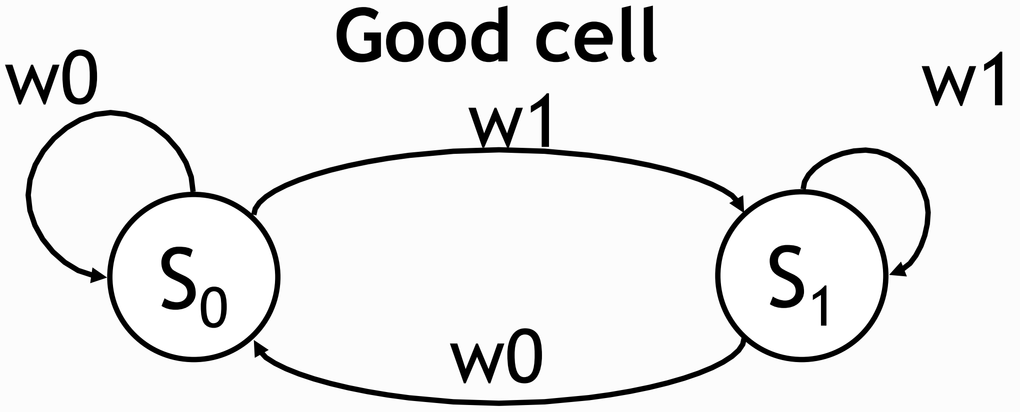
Fault Notation

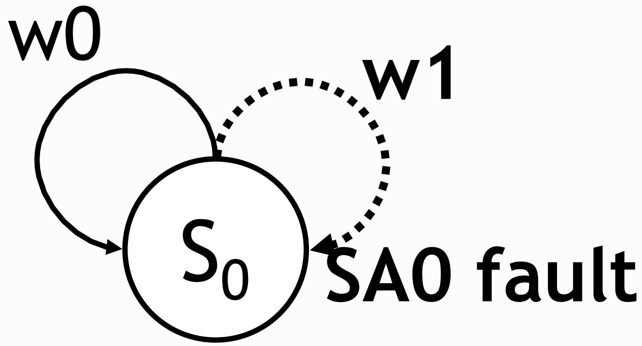
- <…> describes a fault
- <*S/F*> describes a *single-cell fault*
  - *S* describes the state/operation *sensitizing* the fault
    - A fault is sensitized when the fault effect is made present
  - *F* describes the *fault effect* in the *victim cell* (v-cell)
- <*S;F*> describes a *two-cell fault* (a Coupling Fault)
  - *S* describes the state/operation of the *aggressor cell* (a-cell) sensitizing the fault
  - *F* describes the fault effect in the v-cell

- Examples
  - <∀/0>: a SA0 fault	<∀/1>: a SA1 fault
  - <↑/0>: an ↑ TF	<↓/1>: a ↓ TF
  - <↑;0>: a CF	<↑;1>: a CF
  - <↓;0>: a CF	<↓;1>: a CF

Stuck Faults

- ☐ Stuck At Faults => Cell is stuck at a particular value

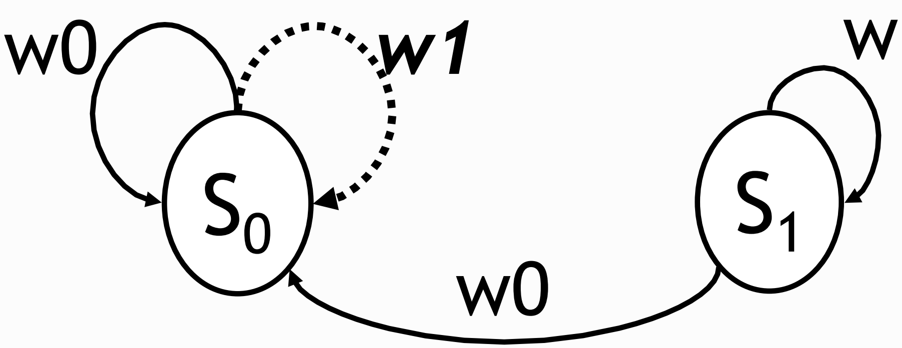




- ☐ Stuck at Open Fault
  - ☐ e.g Word line is broken => When read is performed both BL and BLB remain high

Transition Fault

- Transition Faults => Cell fails to undergo a particular transition



Cell with

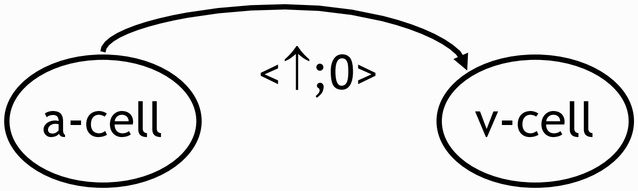
<↑/0> TF

Test: All cells should have a ↑ and ↓ transition and read

- Retention Faults => Cell loses value after a while

Coupling Faults

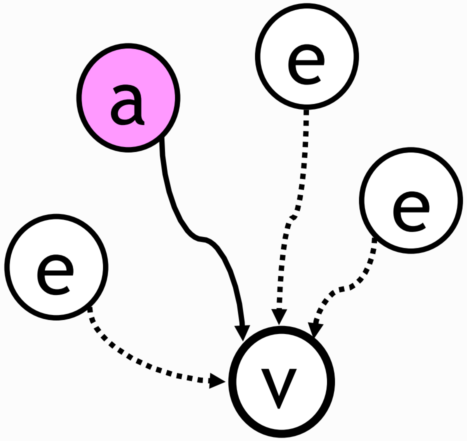
- Coupling Faults => State (or Transition) of Cell A causes a failure in Cell V



- Coupling Transition Faults: <↑;0>, <↑;1>, <↓;0> and <↓;1>
- Coupling state faults: <1;0>, <1;1>, <0;0> and <0;1>
- Coupling inversion fault: <↑;↕> and <↓;↕>
- Linked Coupling faults: The victim can be identical (difficult to detect)

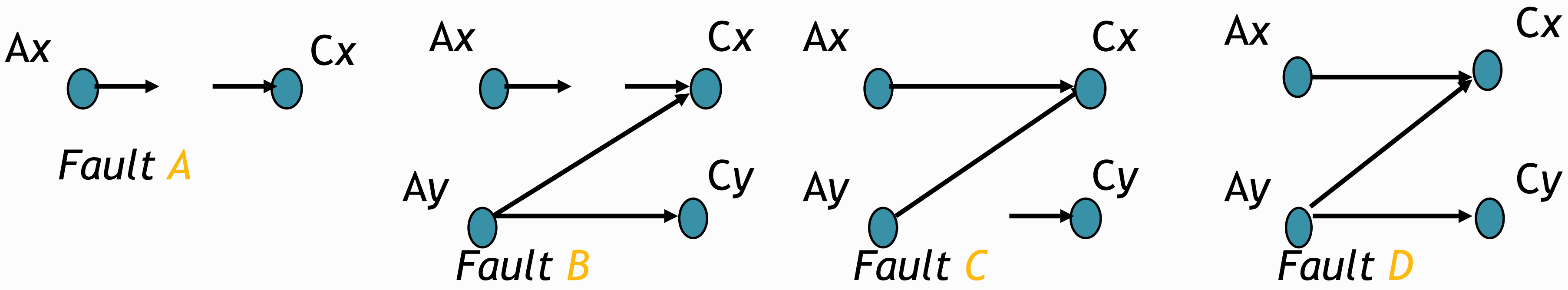
Pattern Sensitive Faults

- ❑ The state (transition) or K cells causes a failure in an ith cell
  - ❑NPSF => The k cells are adjacent



Address Faults

- ❑ Address (A1) cause no cell to be accessed
- ❑ Address (A1) accesses multiple cells
- ❑ Cell (C1) is accessed with multiple addresses
- ❑ Cell (C1) is accessed by its own and another address



March Tests

- A sequence of operations applied in a particular order aimed at targeting the various fault models

{⇕(w0);⇑(r0,w1);⇑(r1,w0);⇕(r0);⇓(r0,w1);⇓(r1,w0);⇕(r0)}

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