High-Performance SRAM Design

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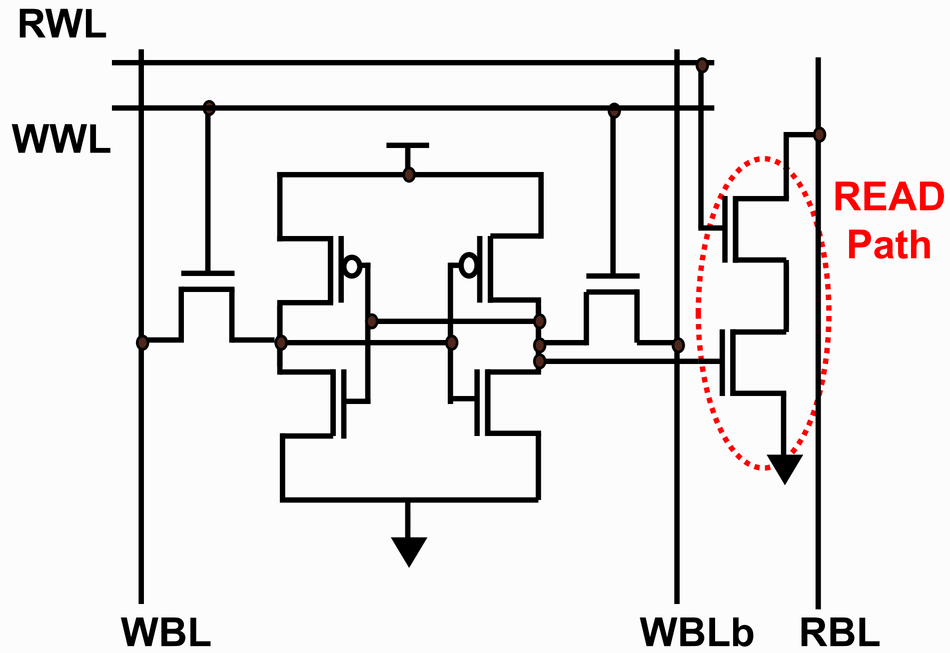
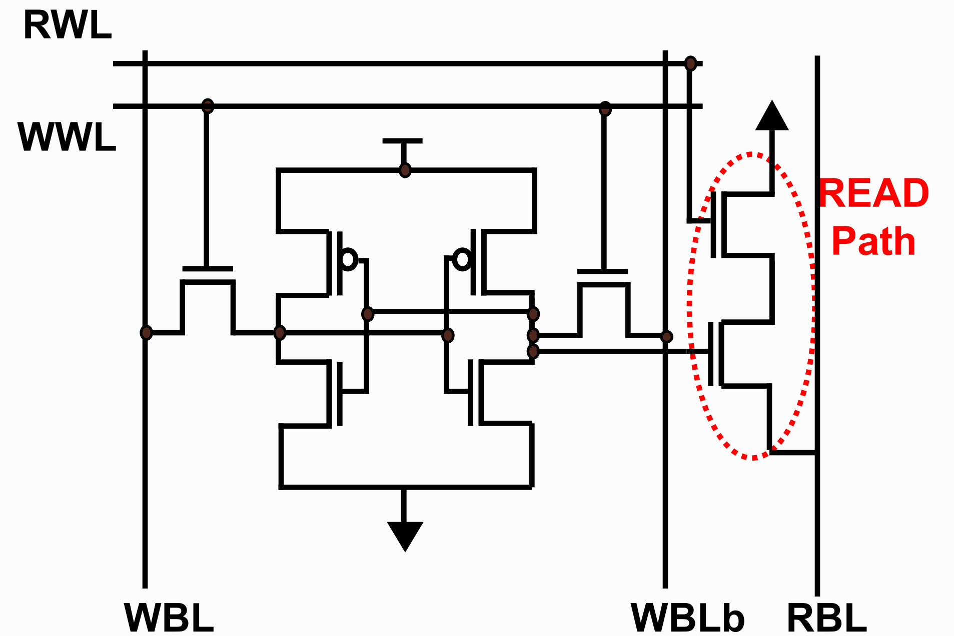
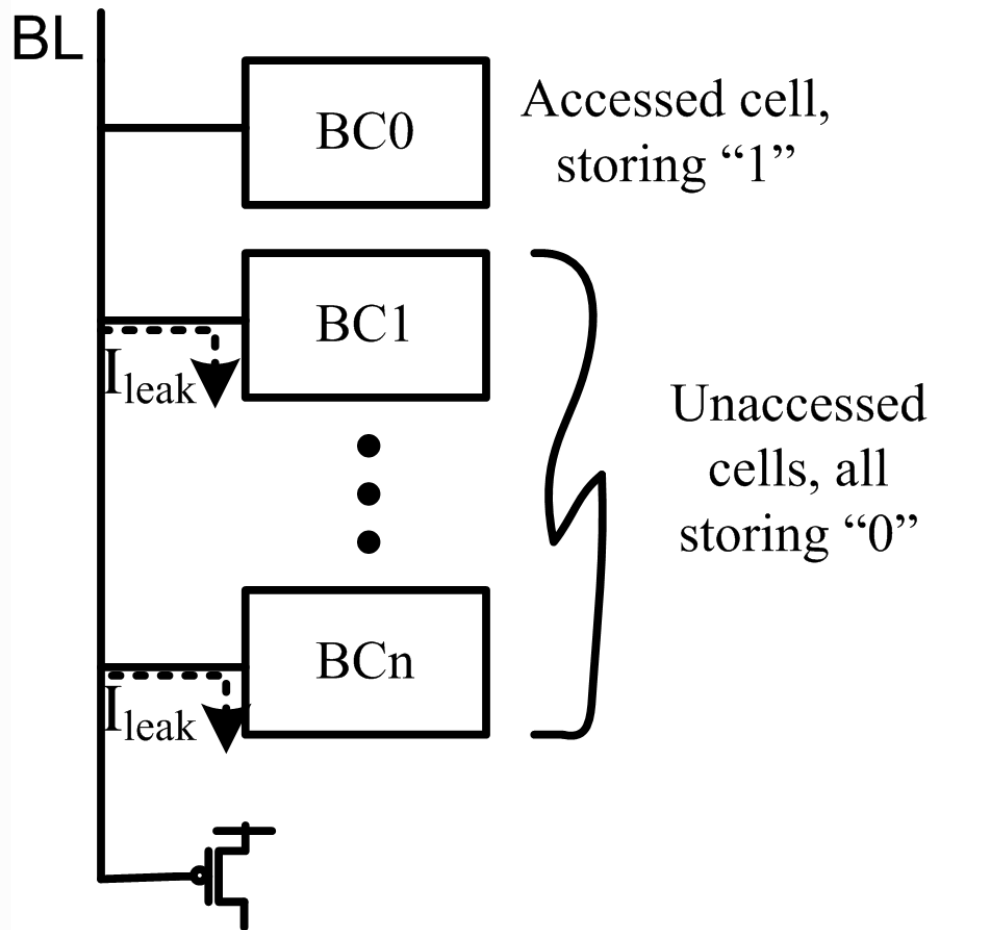
Exercise





Worst case read condition



: Worst case Bitline Leakage when reading a "1"

Data Independent Leakage Cell

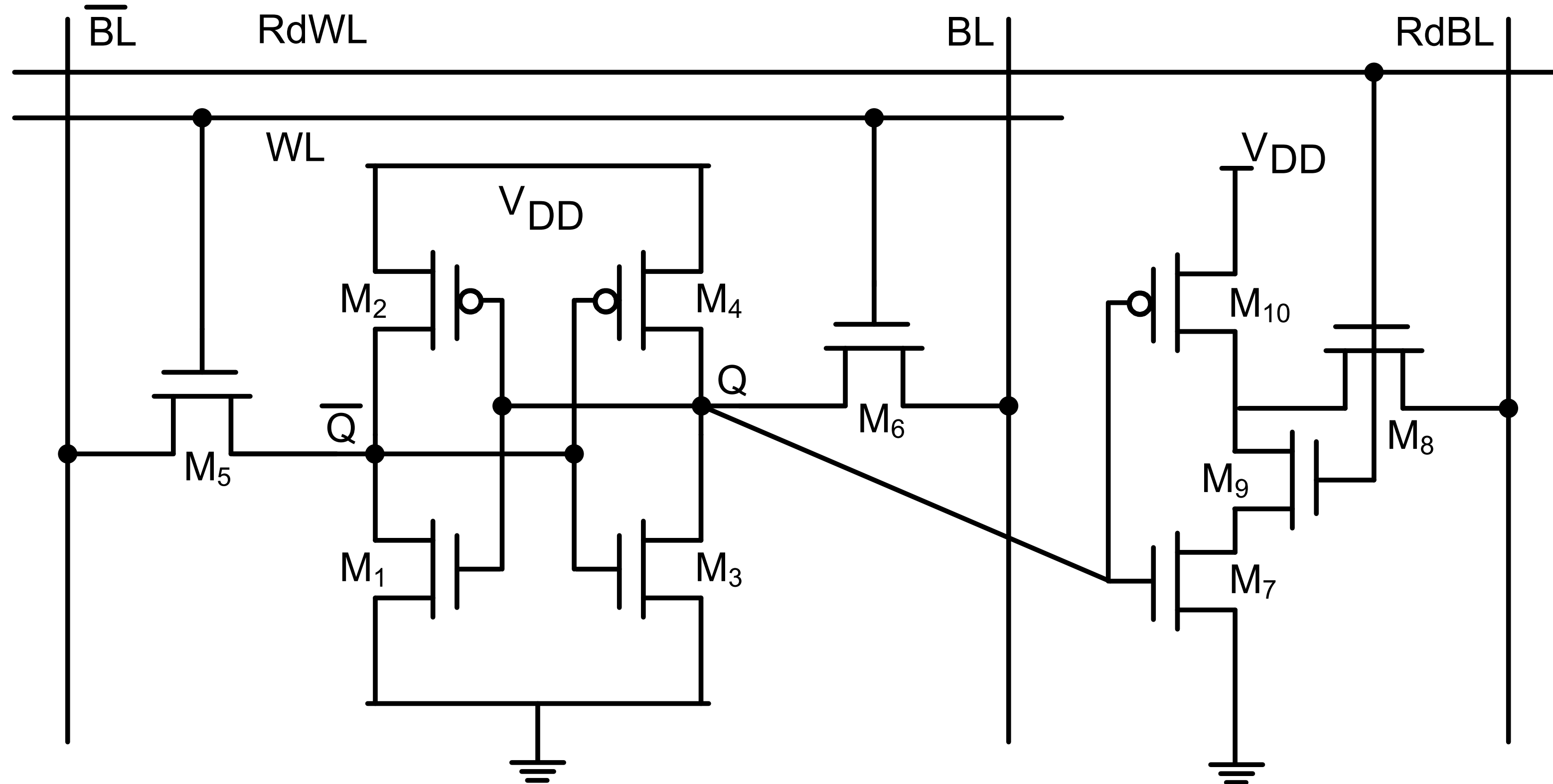
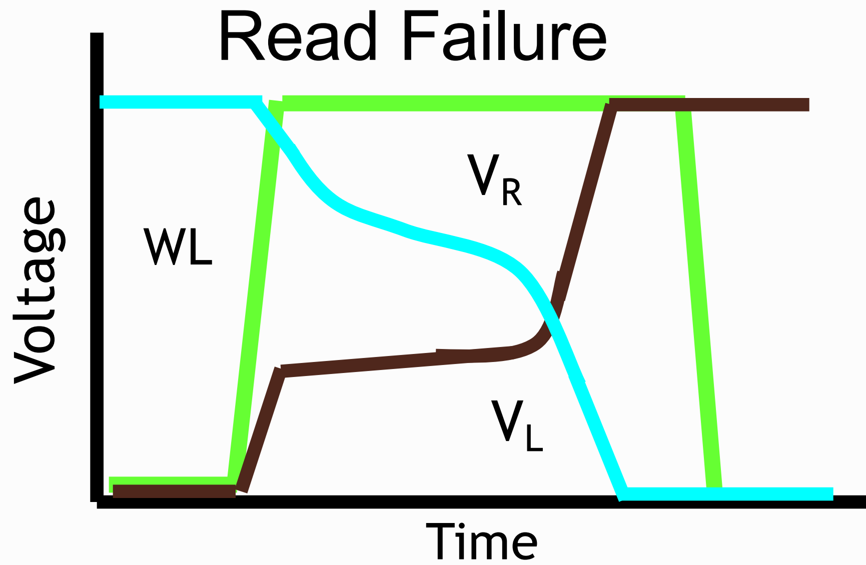
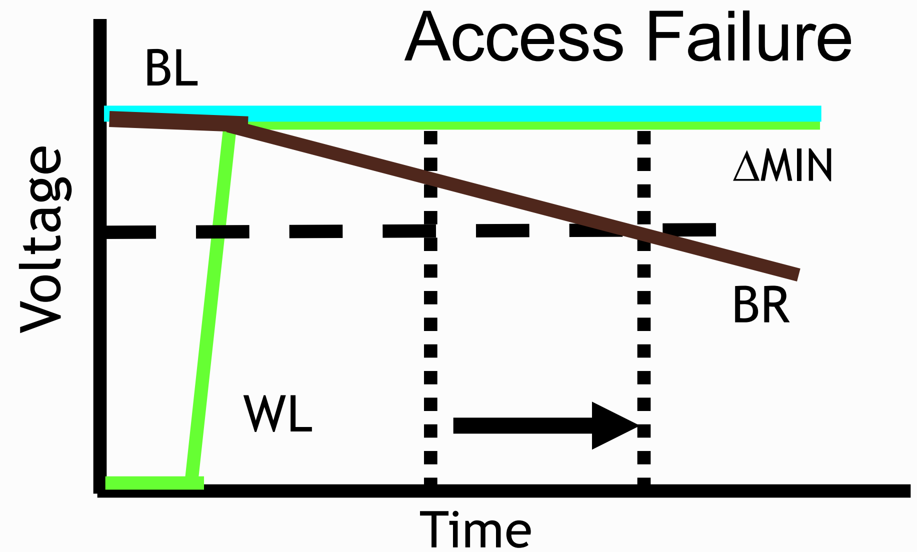


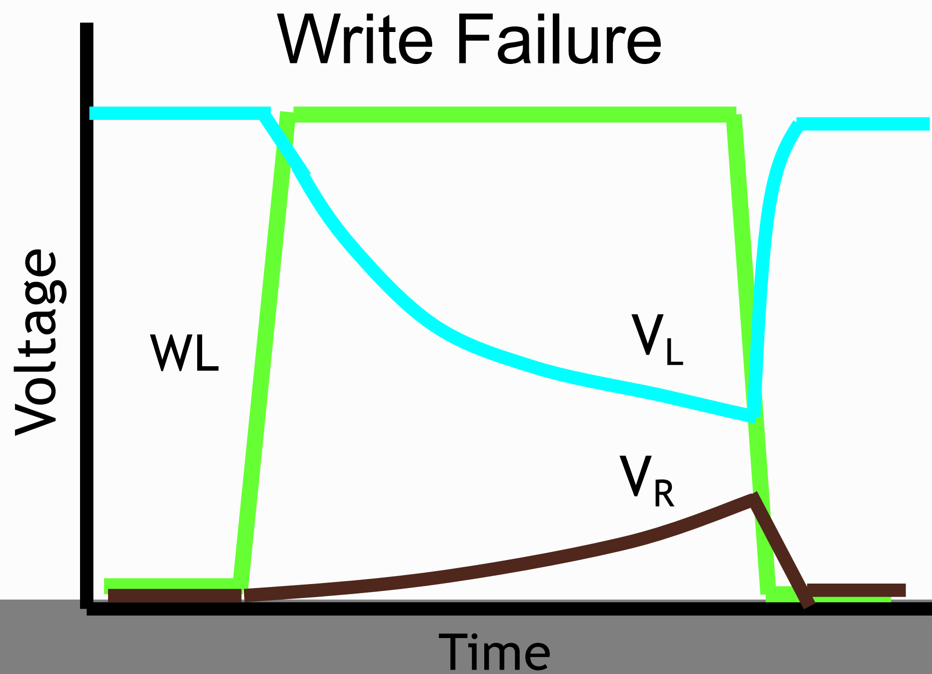
Figure 9 (c): Schematic of Ten transistors with M9 and M10 added to schematic of eight transistor to lower leakage power

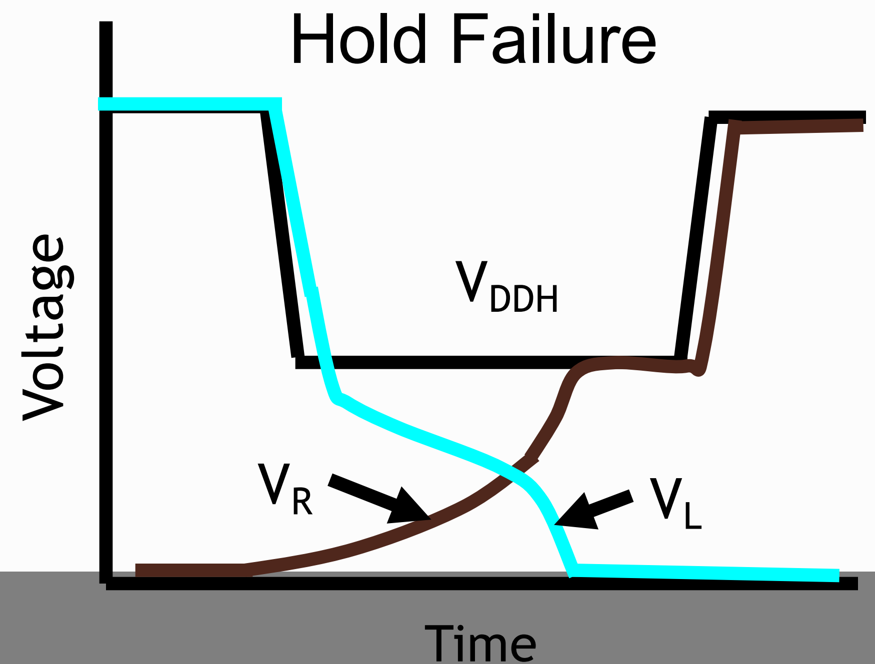
(Calhoun, 2010)

Mechanisms of Parametric Failures









Question

- ❑ Which of the following are true for the 6-T SRAM cell

a) A cell with poor READ margin is unlikely to have access failure

b) Differential read means there is no worst case data condition for read

c) The worst case write condition is having cells with alternate 0s and 1 along the column

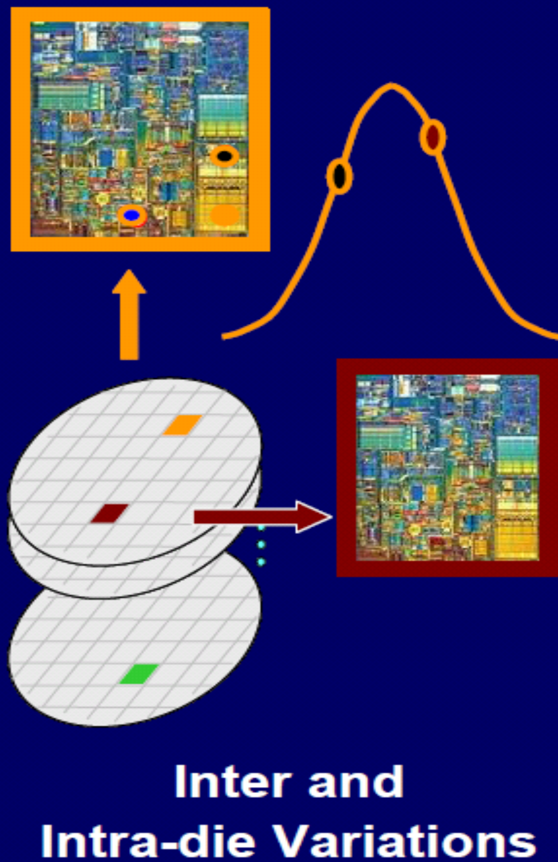
d) Access fails can be minimized by running the array at a slower frequency

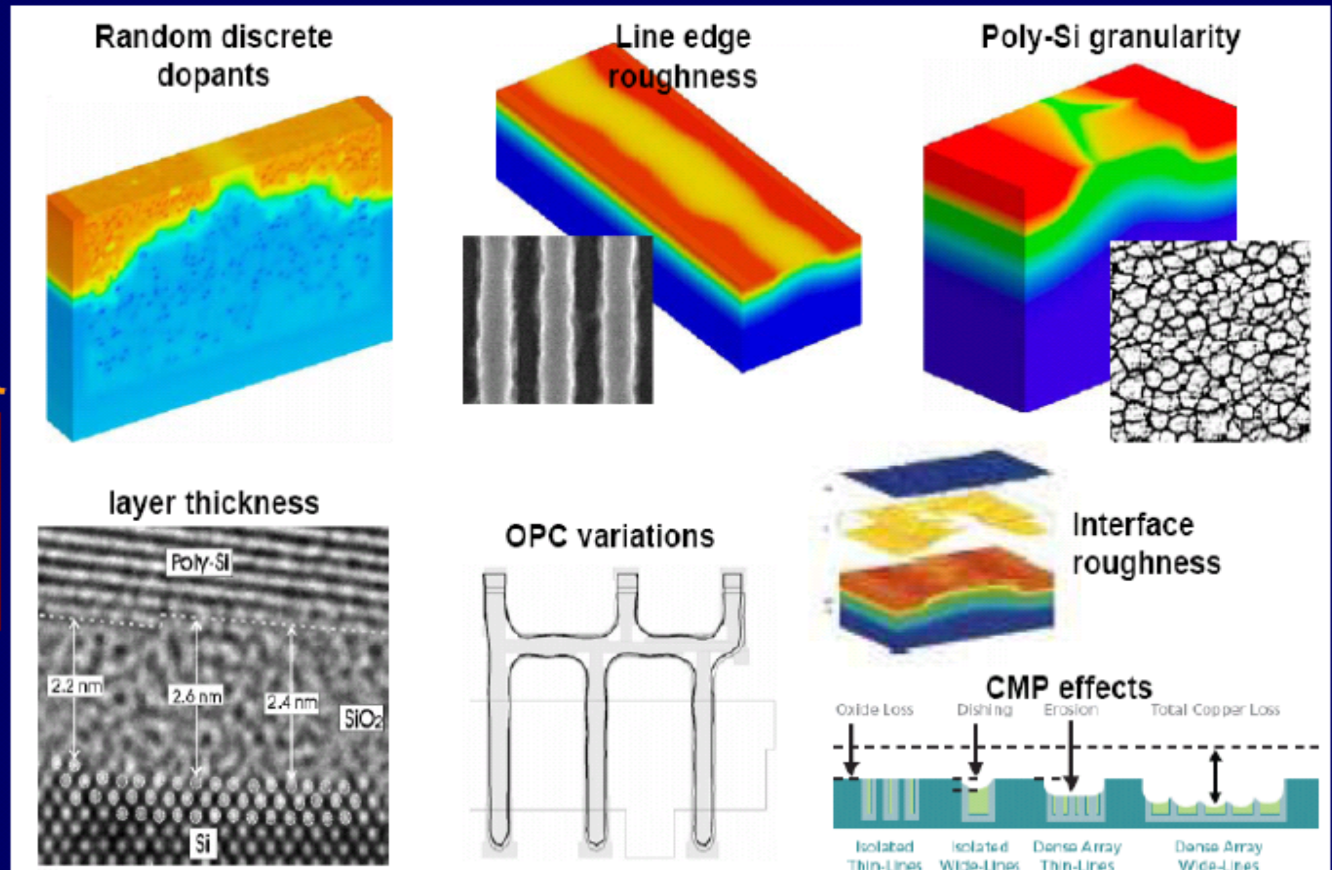
Topics

- ❑ Introduction to memory
- ❑ SRAM basics and bitcell array (refresher)
- ❑ Current Challenges
- ❑ Alternative Cell Types (6 to 10T), Asymmetric Cells, Sub-threshold Cells, Low – leakage cells
- ❑ Impact of Variation, Assist Circuits
- ❑ BTI and impact on SRAMs
- ❑ Power

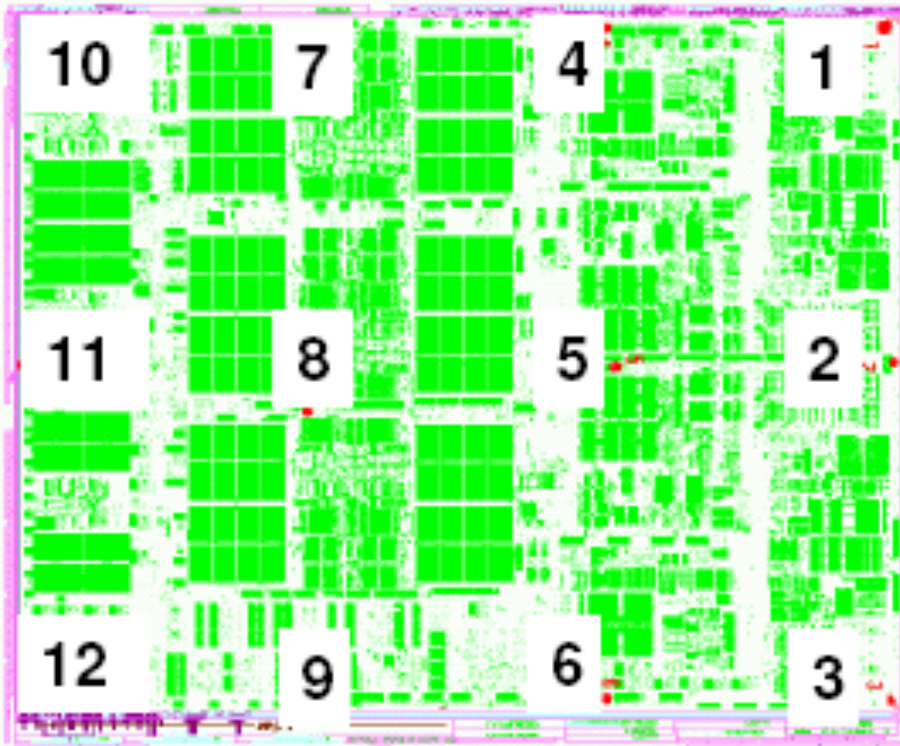
Sources of Manufacturing Variations

Variation in Process Parameters

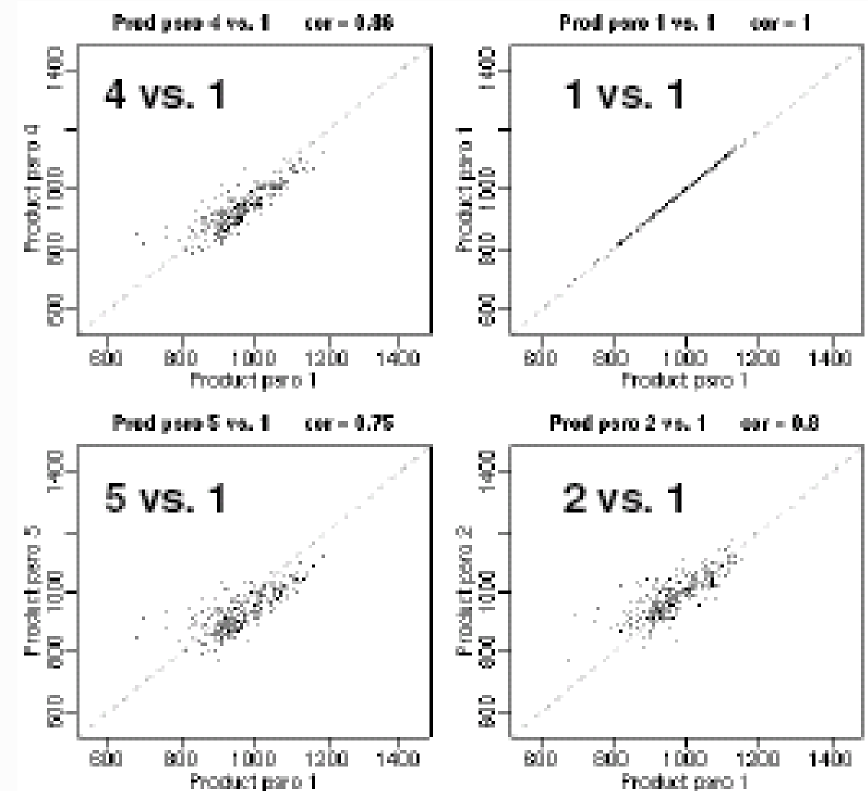




Impact of Manufacturing Variations



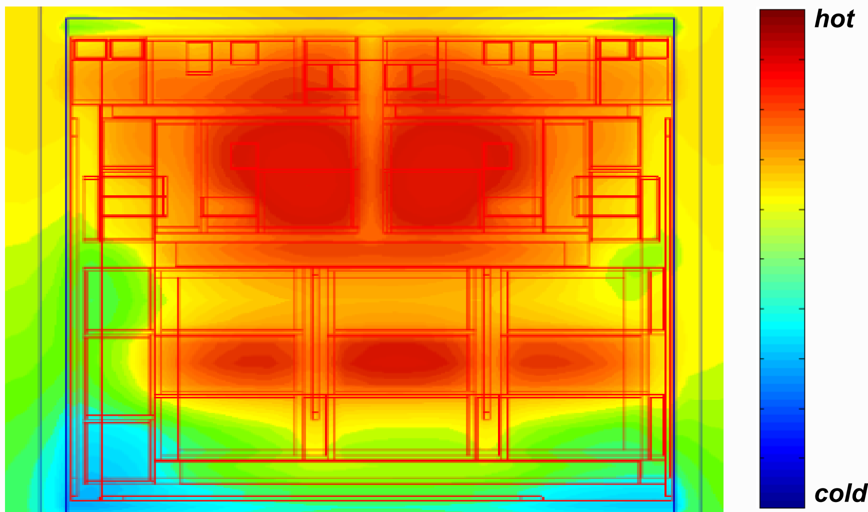
Location of Identical Ring Oscillators on a Die

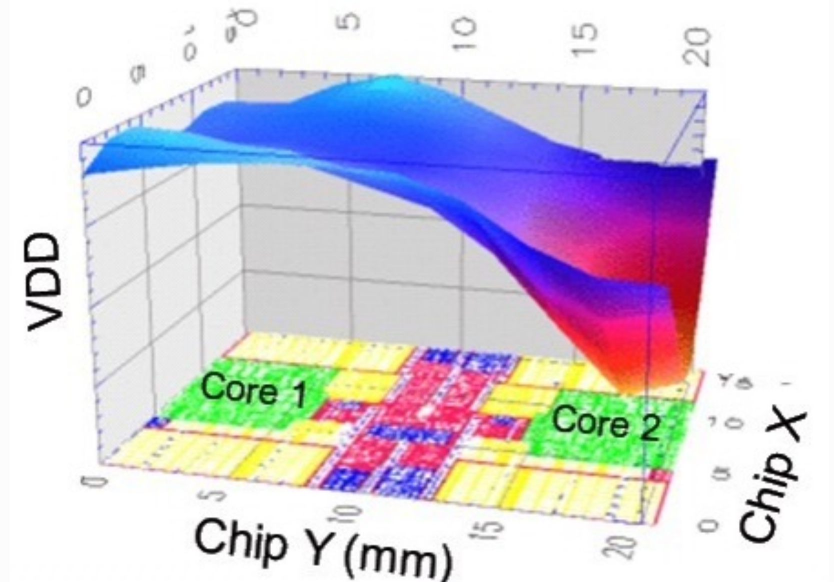


Frequency Correlation

(averaged over 300 die)

Environmental Variations





Temperature Variation

- Switching Characteristics of Blocks
- Material Properties: Thermal Coefficient
- Cooling and Packaging Solutions
- Workload and Thermal Management Policies

Delay and leakage increase with temperature

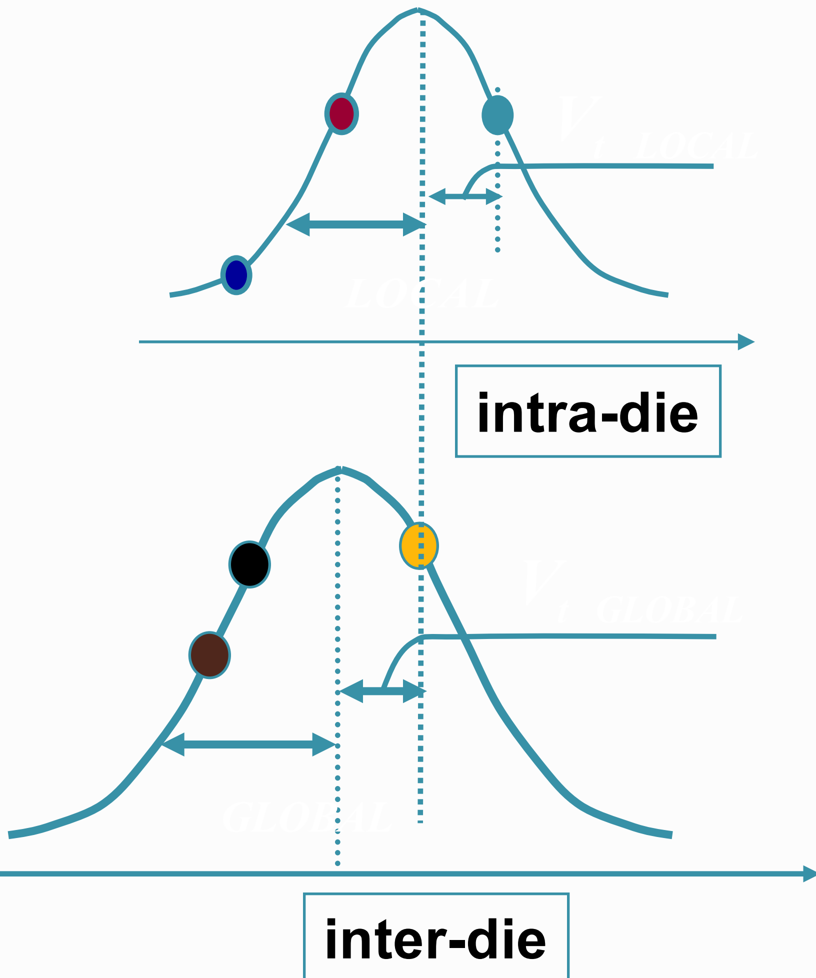
Power Supply Variation

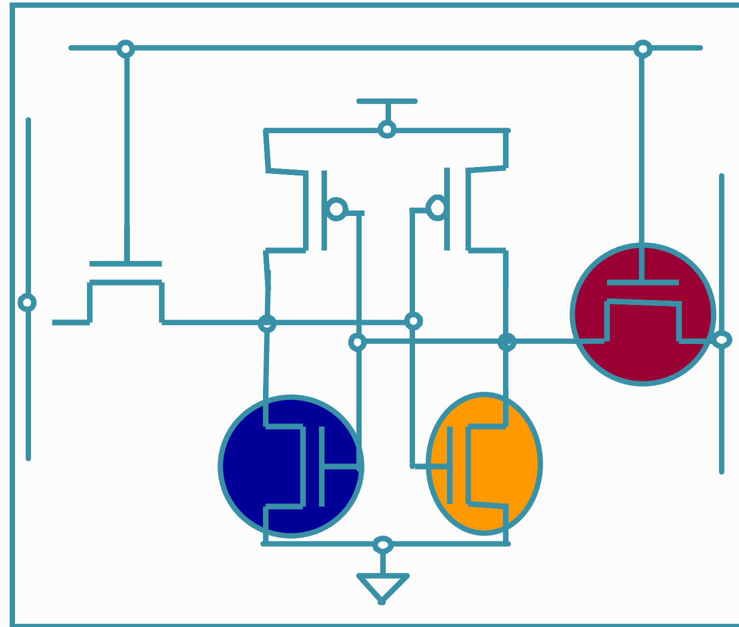
- IR drop: Leakage, Power grid robustness
- Ldi/dt: Transient activity, decoupling capacitors
- Power Efficient Design Strategies: Clock Gating, Power Gating

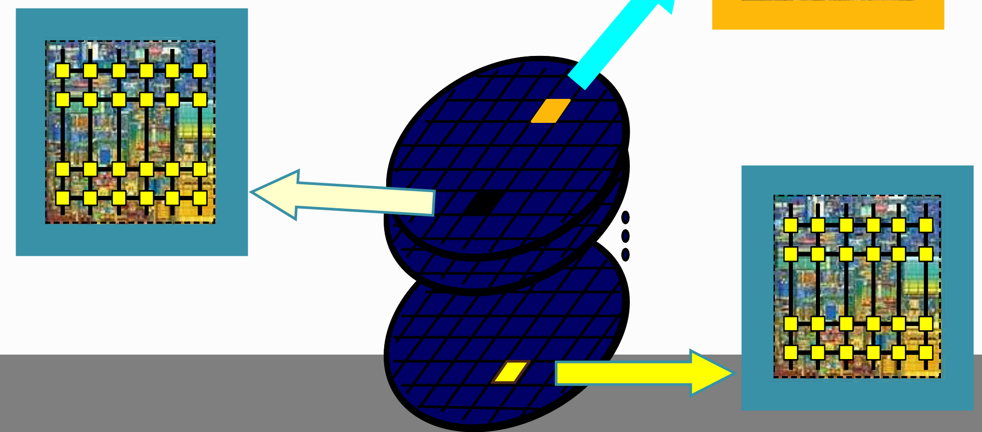
Delay increases with power supply droop

P. Restle, ICCAD 2006

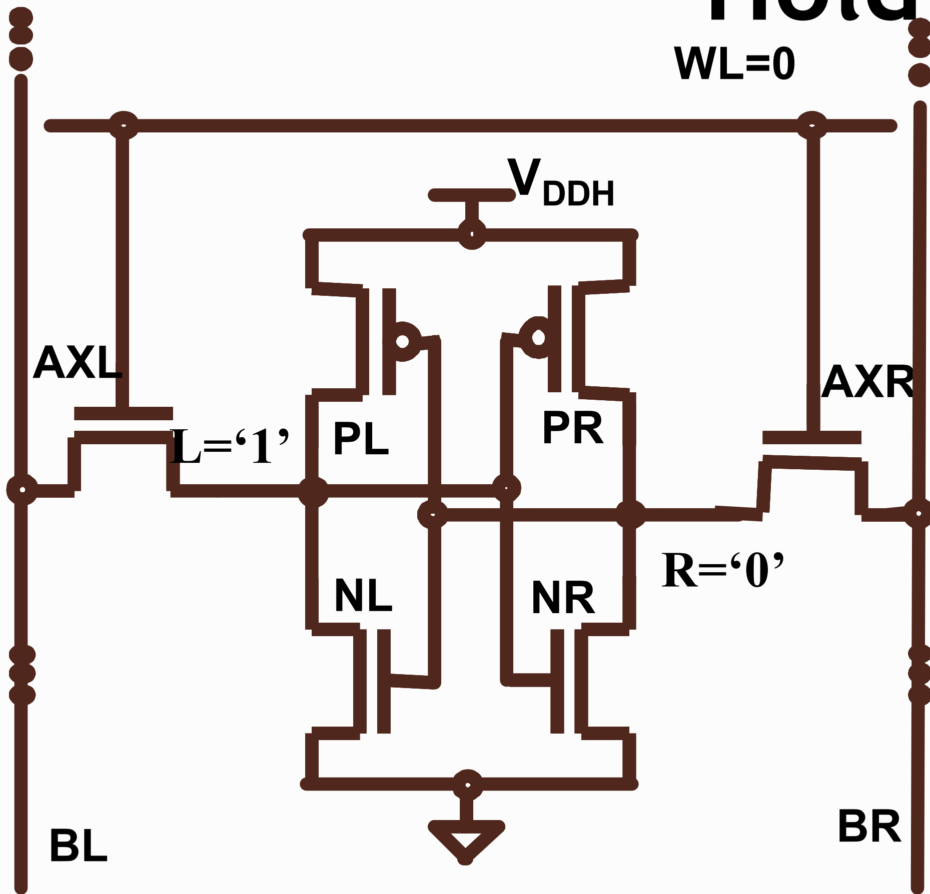
Global and Local Variations

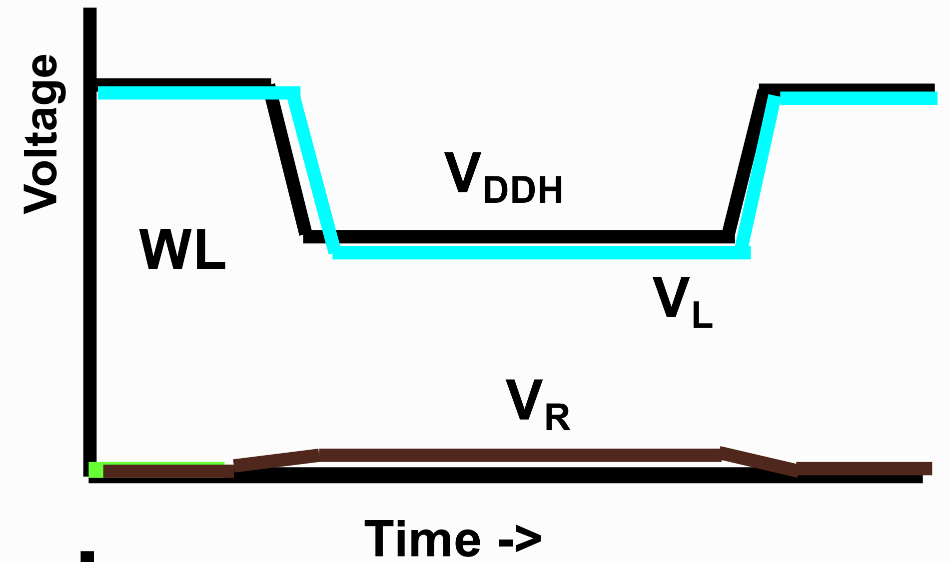


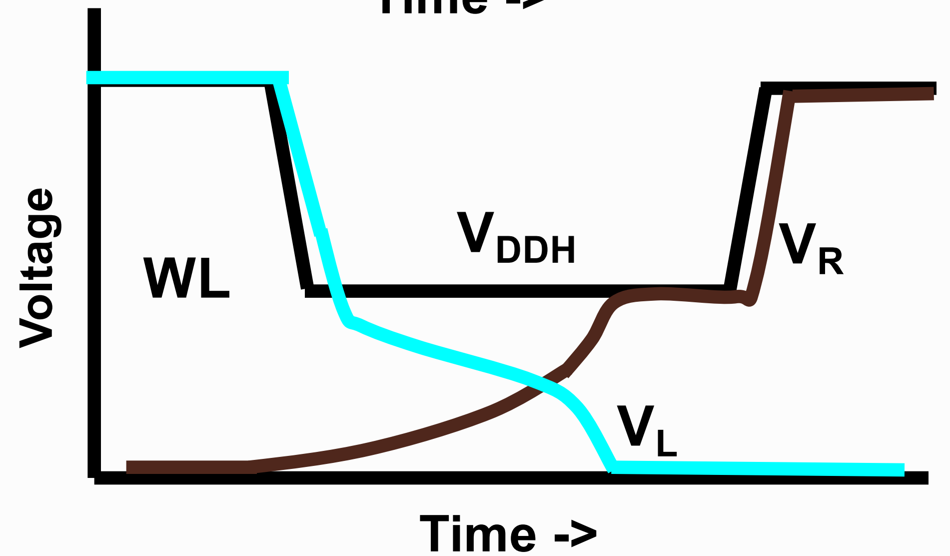




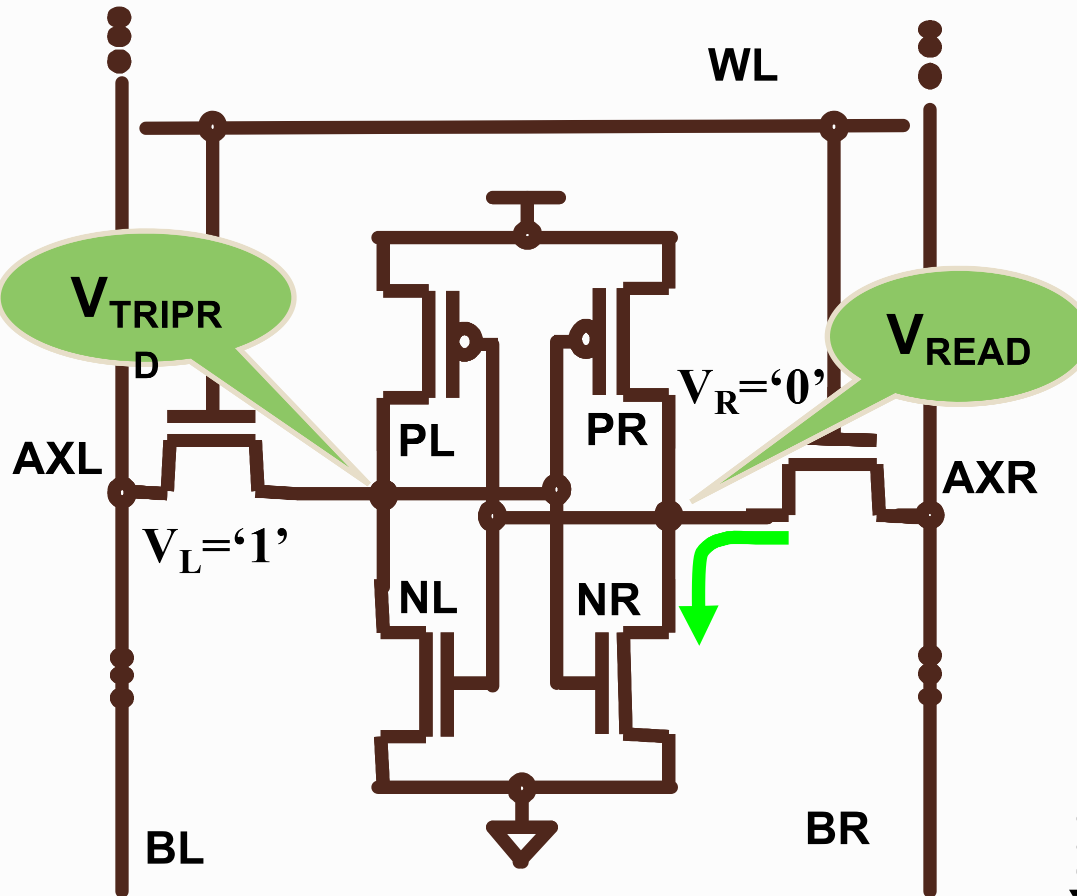
Hold Failure

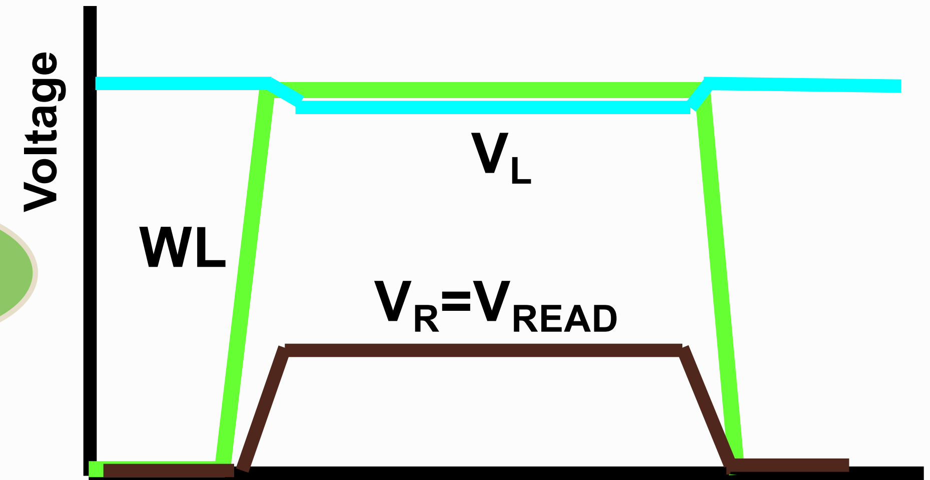


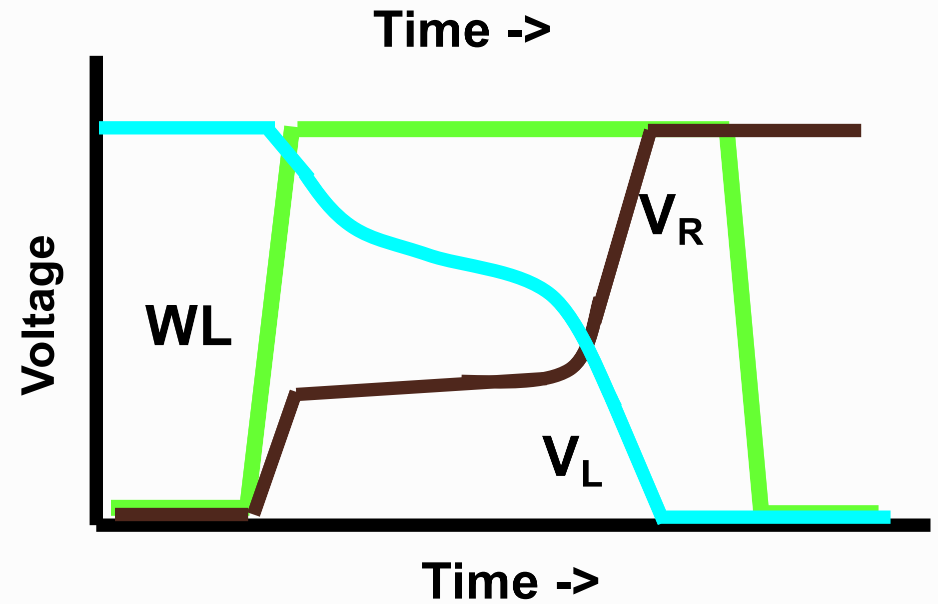




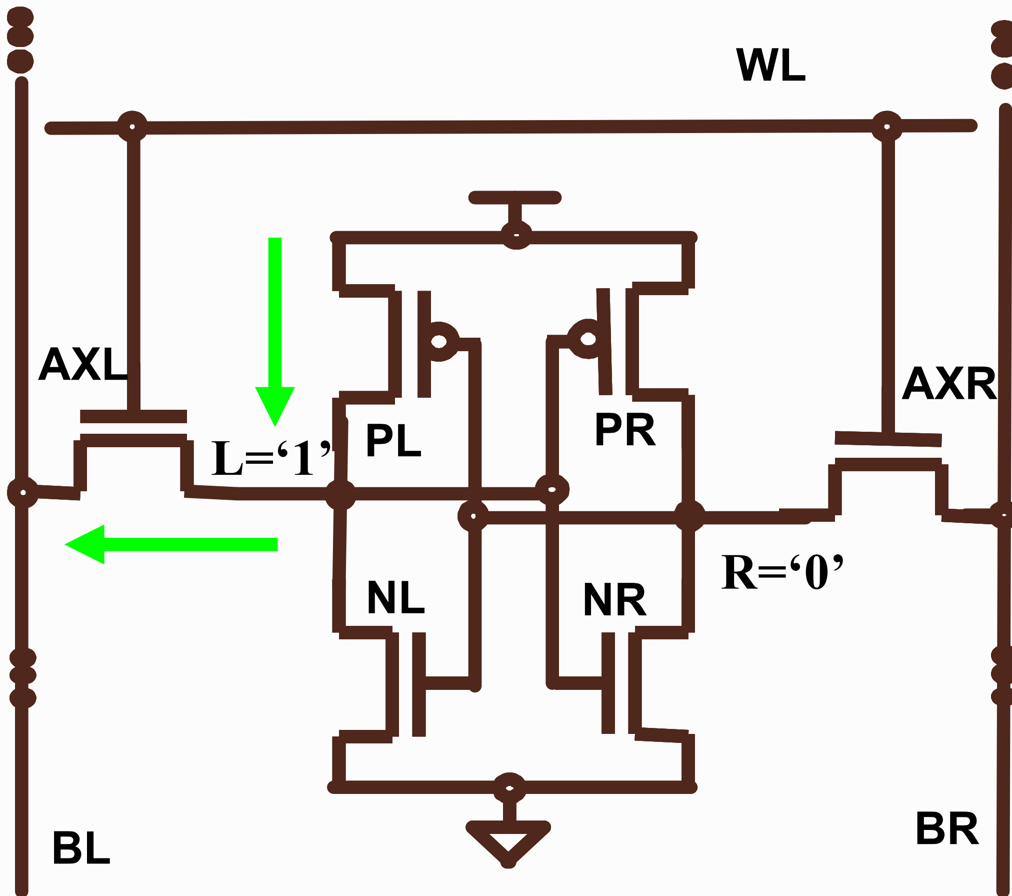
Read Failure

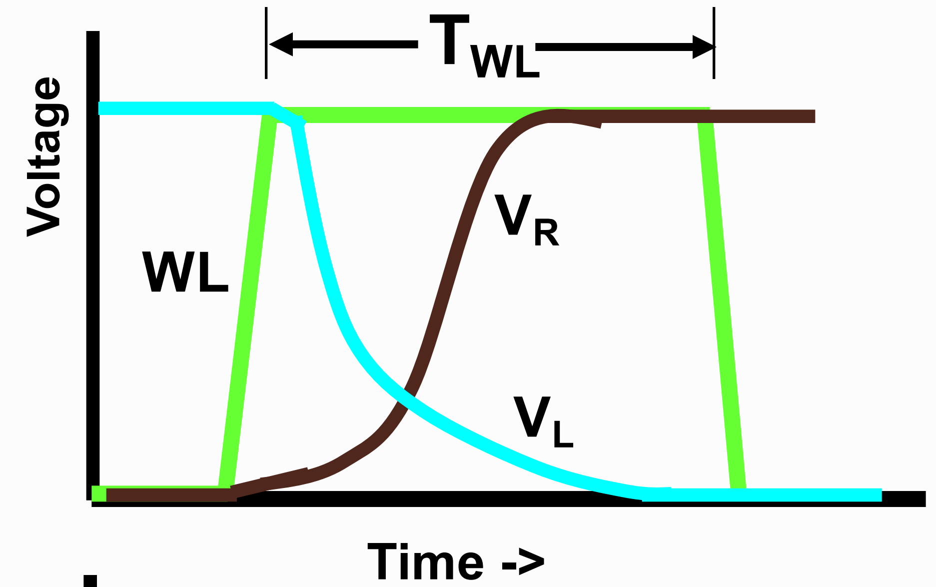


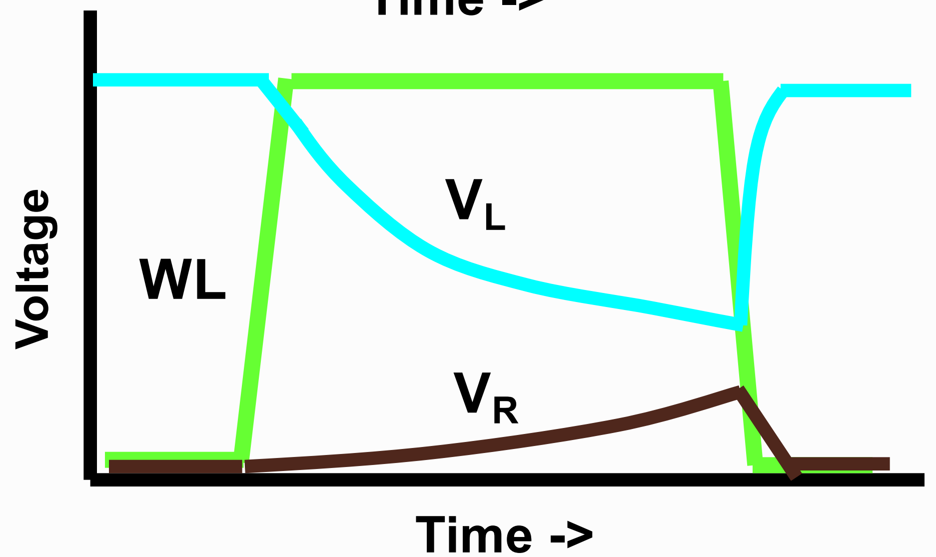




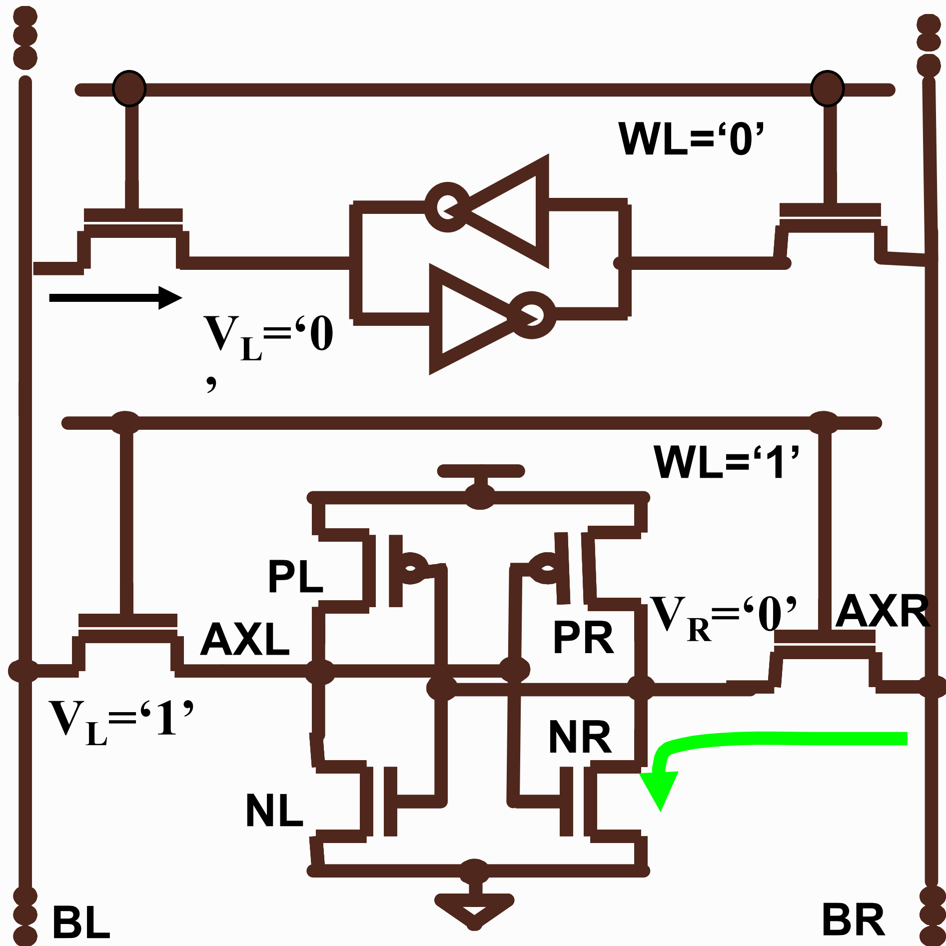
Write Failure

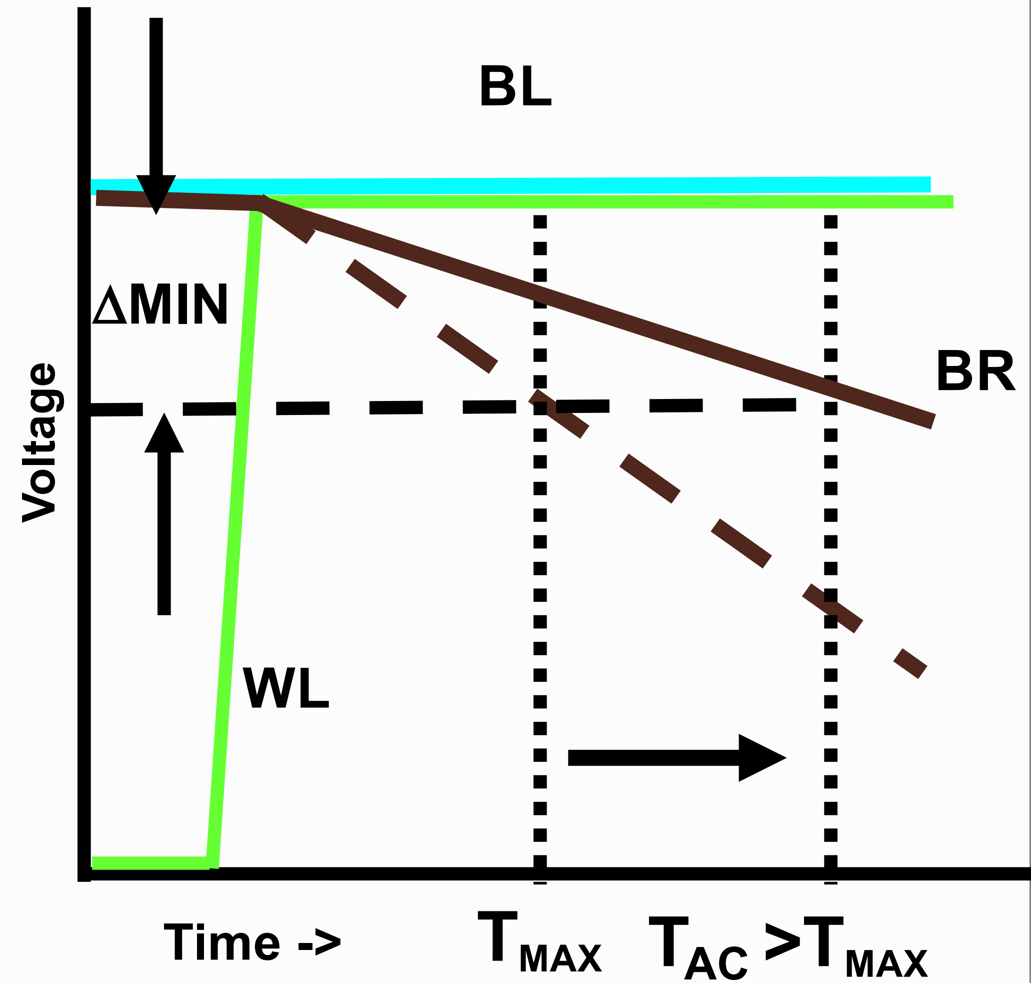






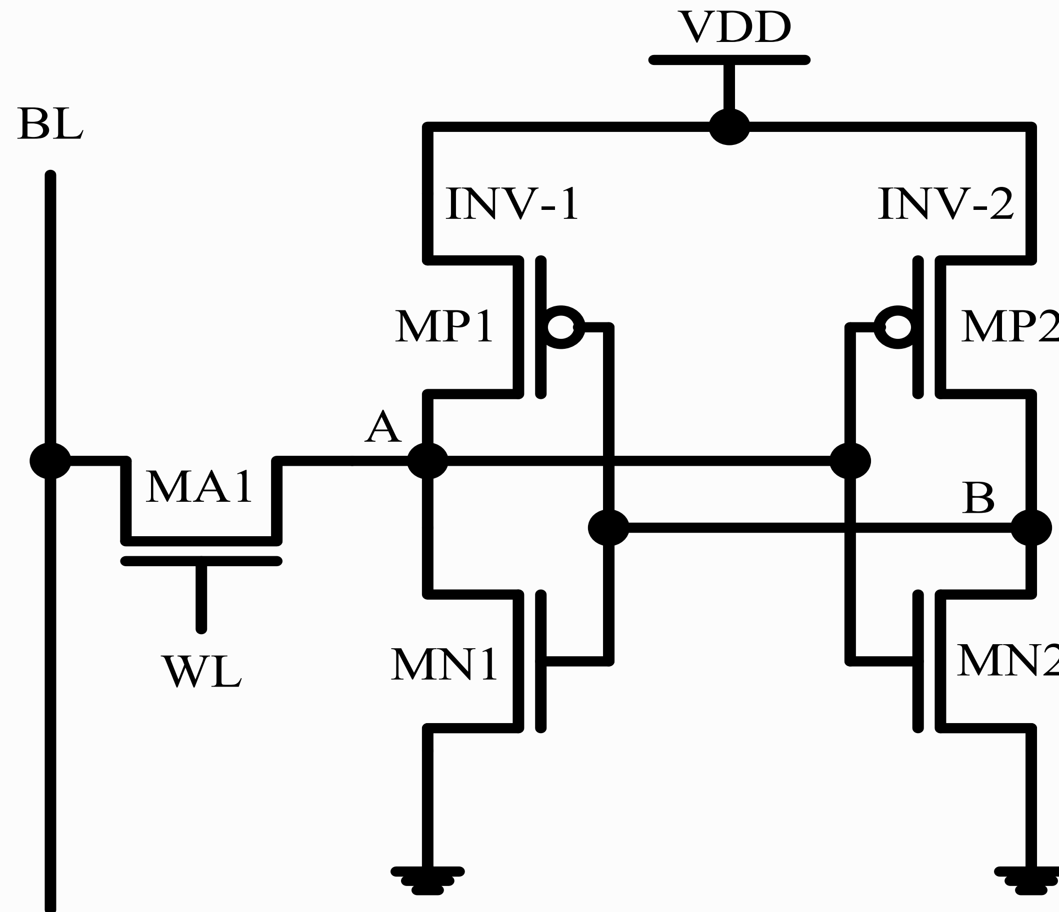
Access Failure



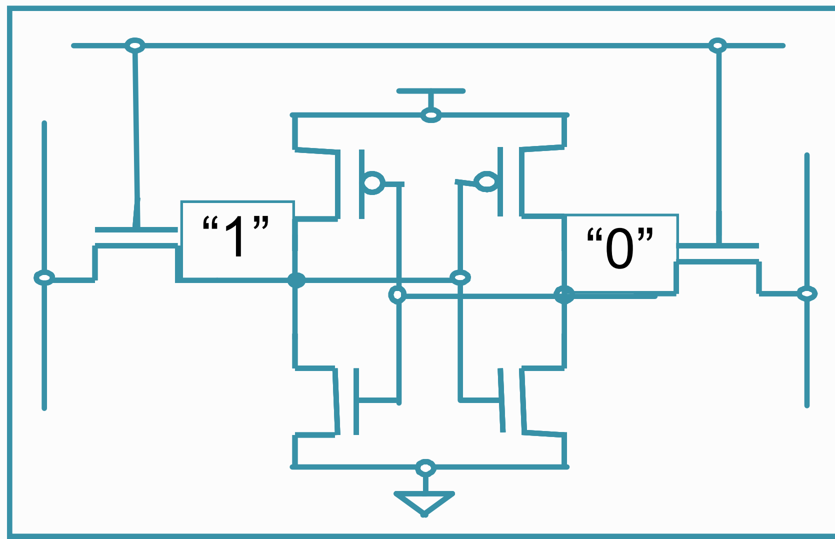


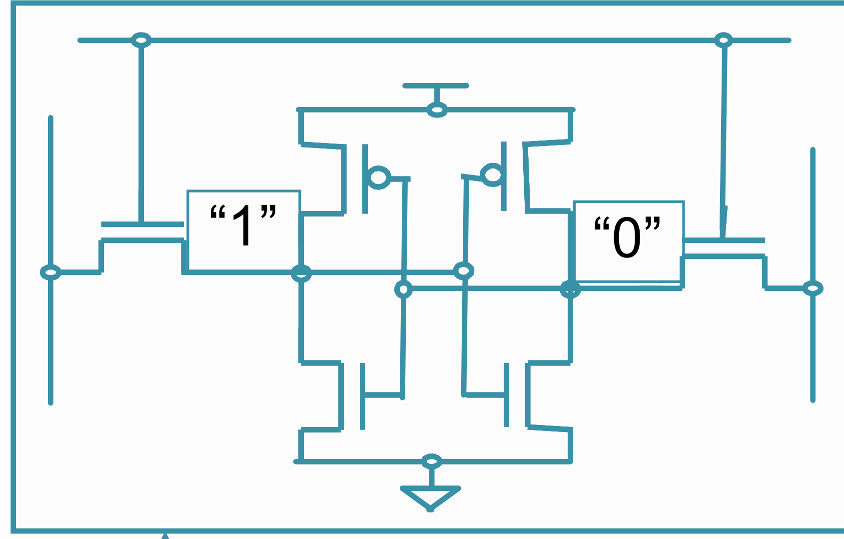
Question

- Mark worst case VT variation condition for each device for write failure

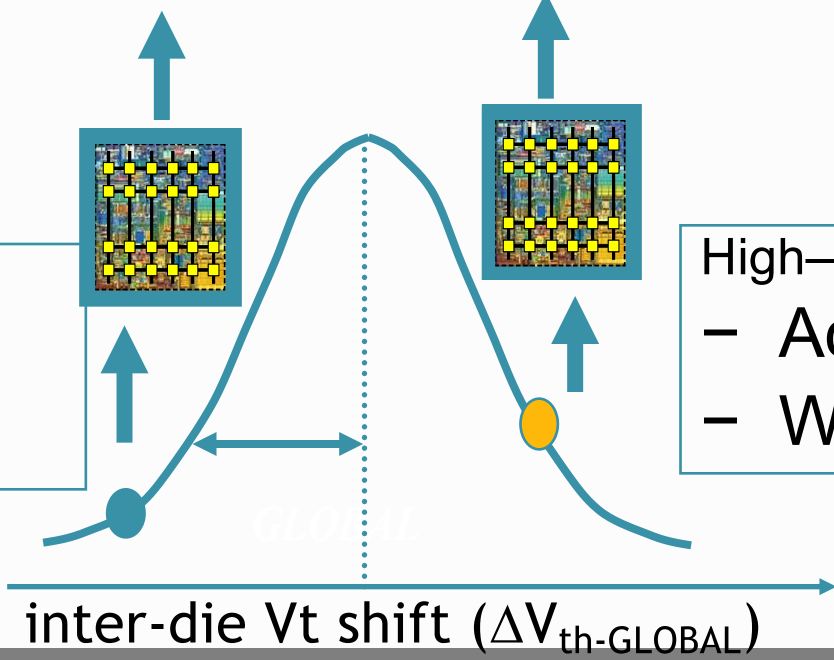


Inter-die Variation & Cell Failures





Low–Vt Corners
- Read failure ↑
- Hold failure ↑



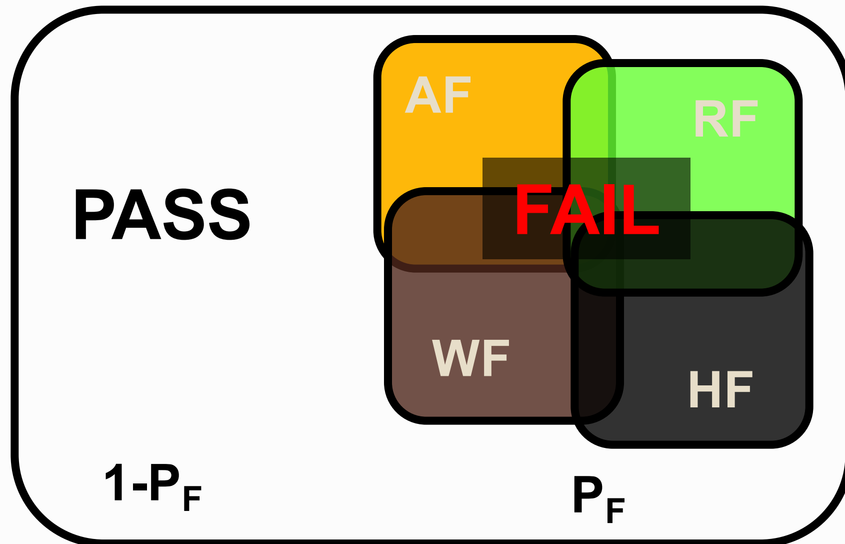
High–Vt Corners
- Access failure ↑
- Write failure ↑

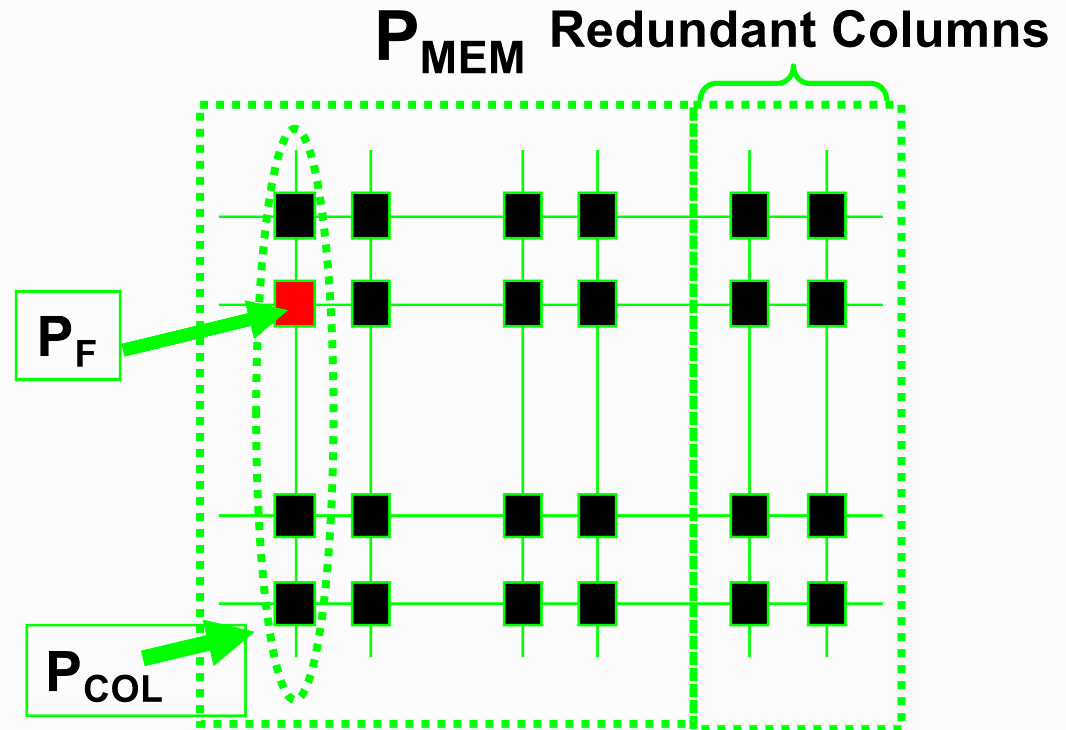
S. Mukhopadhyay et. al, ITC2005, VLSI2006, JSSC2007, TCAD2008

Failures in SRAM Array

Overall Cell Failure:

$$P_F = P\left[Fail\right] = P\left(A_F \cup R_F \cup W_F \cup H_F\right)$$

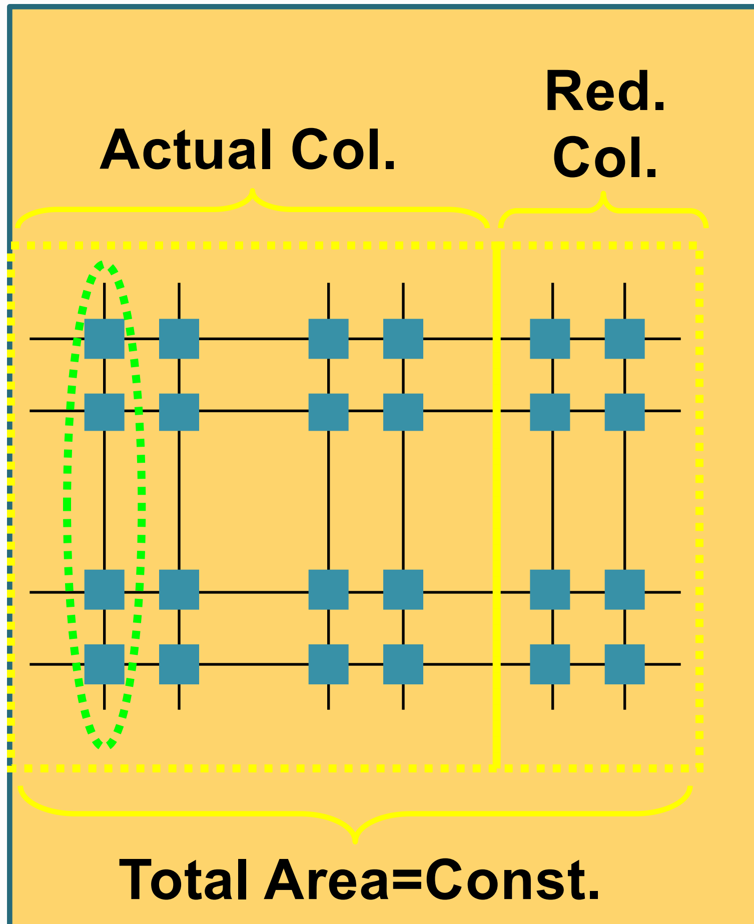




- P_{COL}: Probability that any of the cells in a column fail

$$P_{COL} = 1 - (1 - P_F)^{N_{ROW}}$$

Impact of Redundancy on Memory Failure



Failure Probability

Redundant Col / Total Col. [%]

σVt

P_{MEM}

σVt

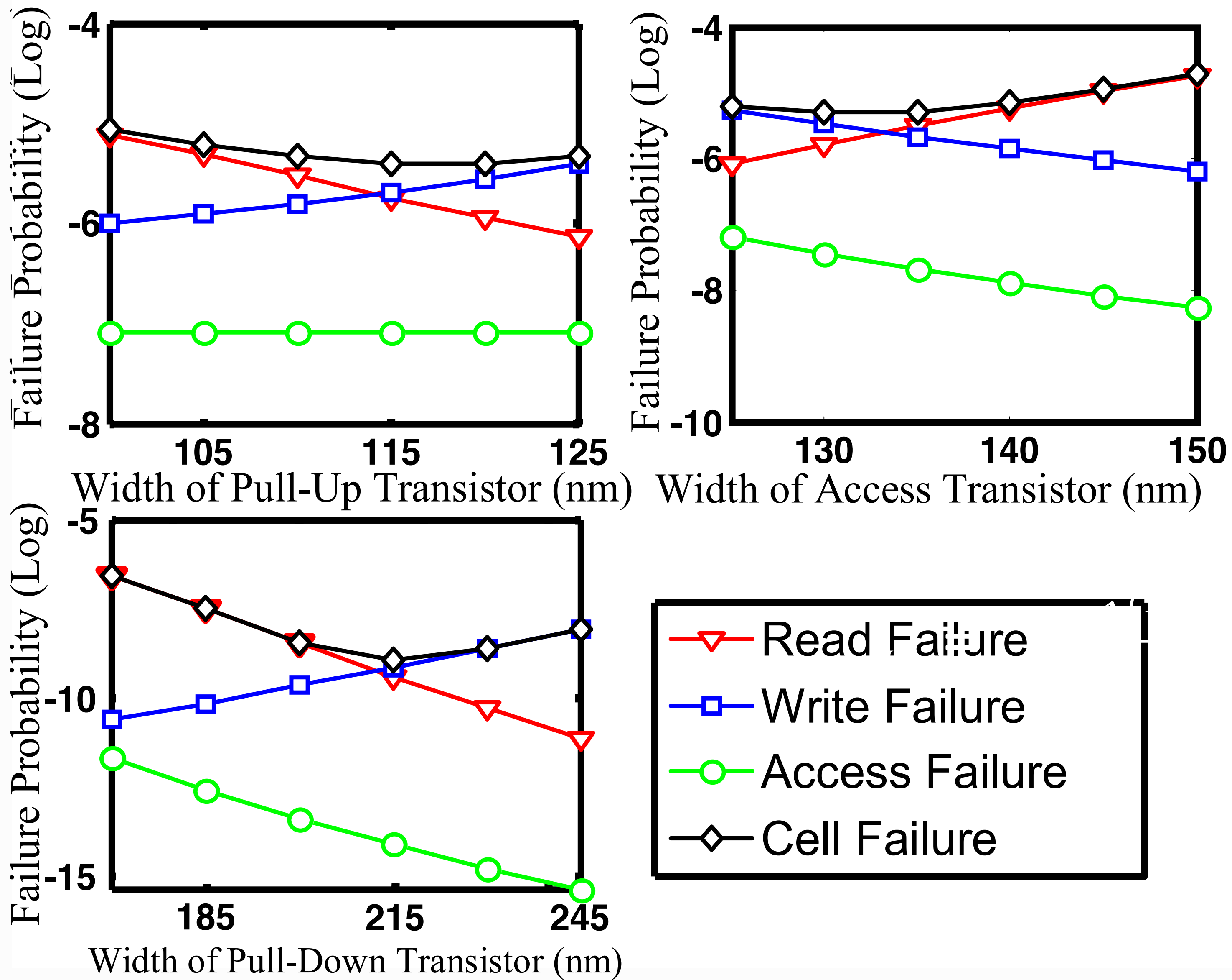
Cell Failure

Larger redundancy

(1) more column to replace (less memory failure).

(2) smaller cell area (larger cell failure).

Transistor Sizing



Question

- Array redundancy

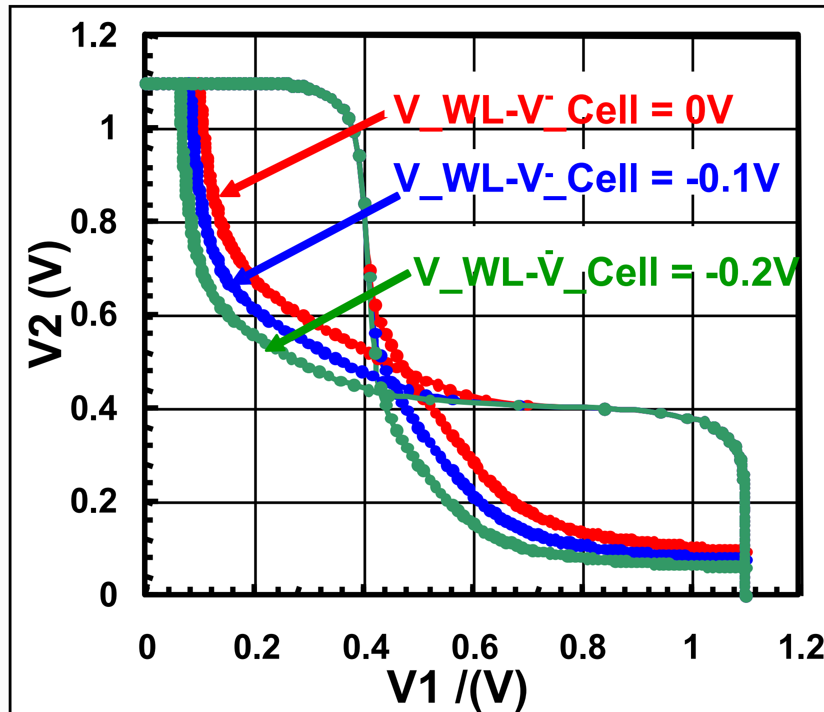
a) Improves cell stability

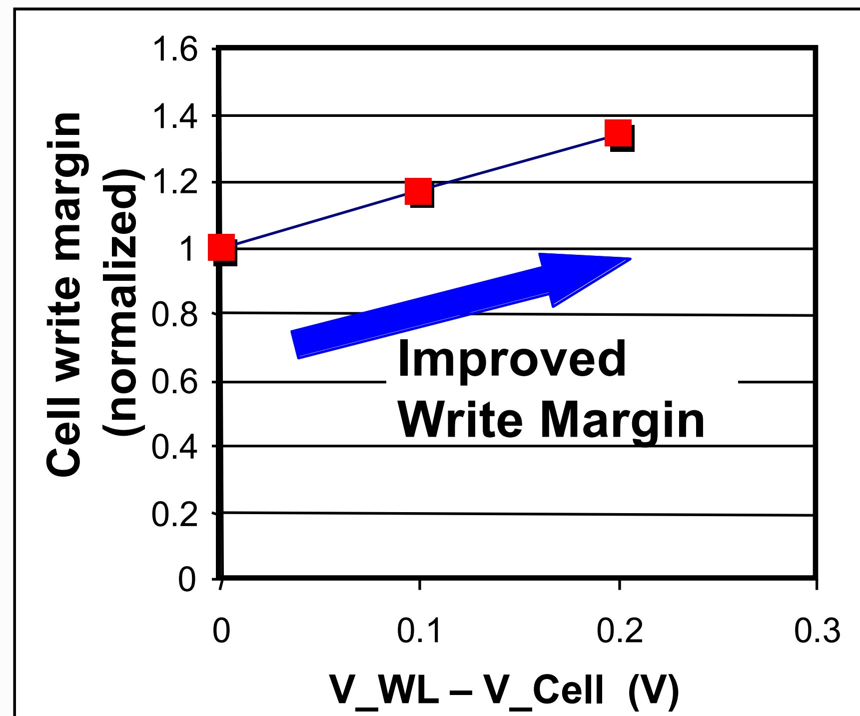
b) Degrades cell performance (i.e increases read and write times)

c) Does not require any change to cell peripheral circuits

d) Row redundancy is better than column redundancy

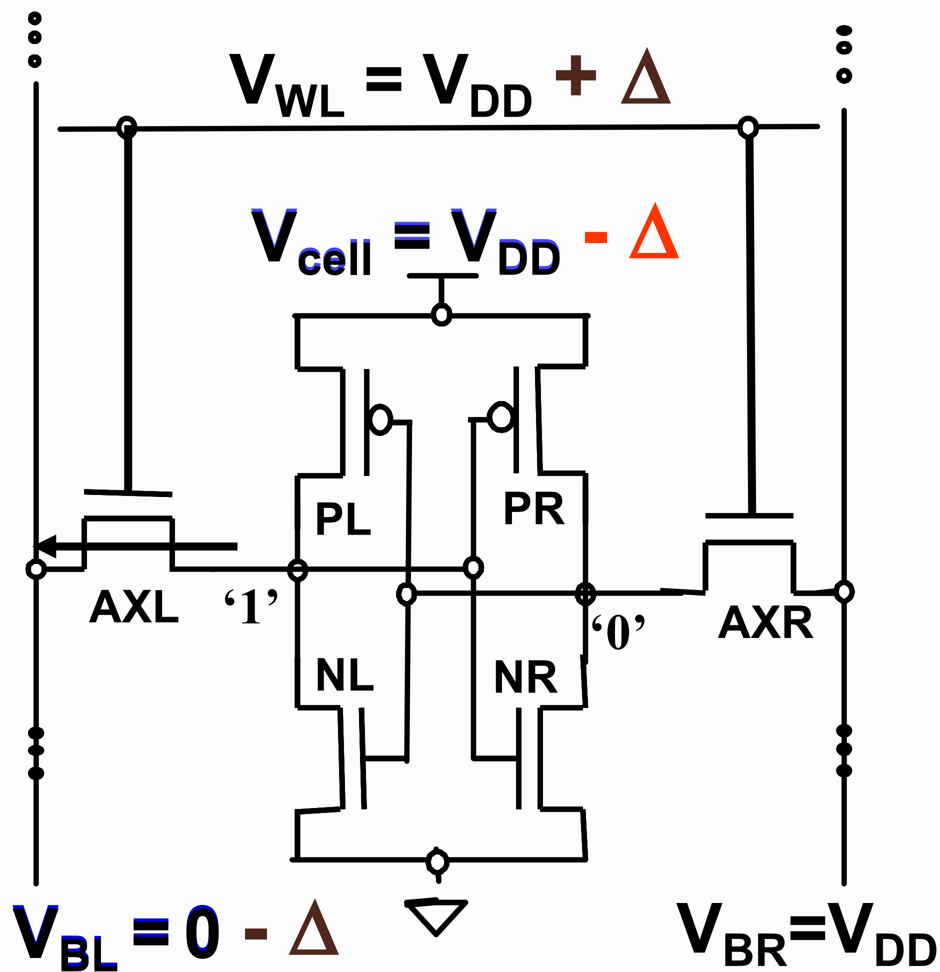
Example: Multi-VCC for SRAM Cell





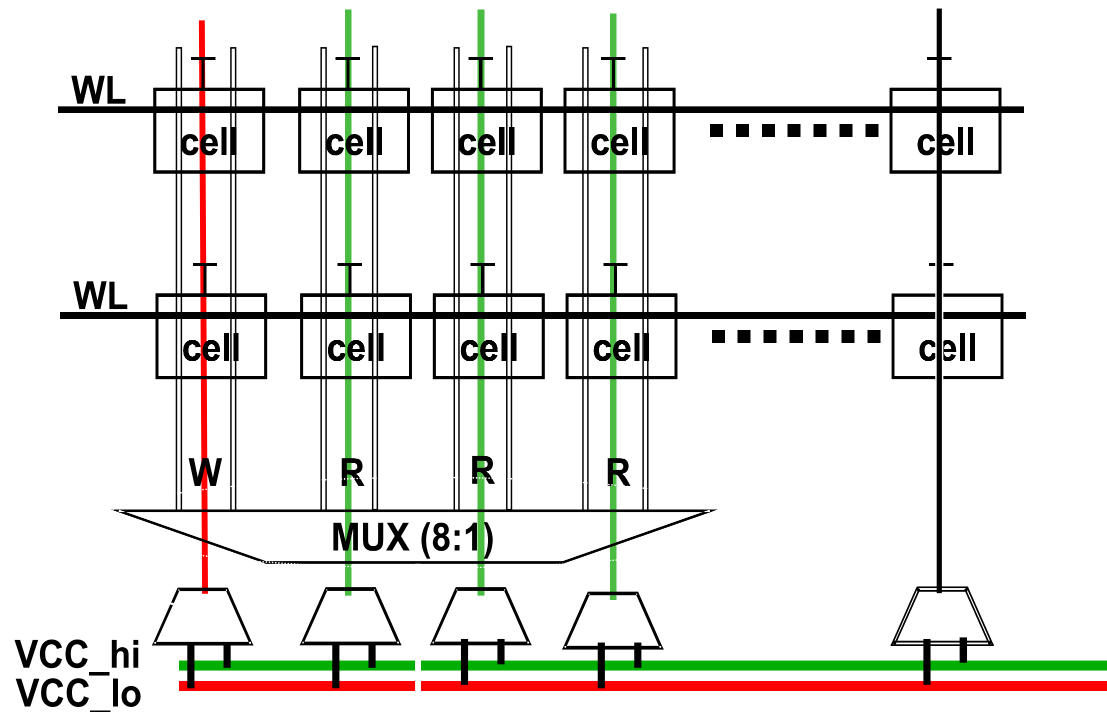
- Create differential voltage between WL and Cell to decouple the Read & Write
  - Write: V_WL > V_Cell
  - Read: V_WL < V_Cell

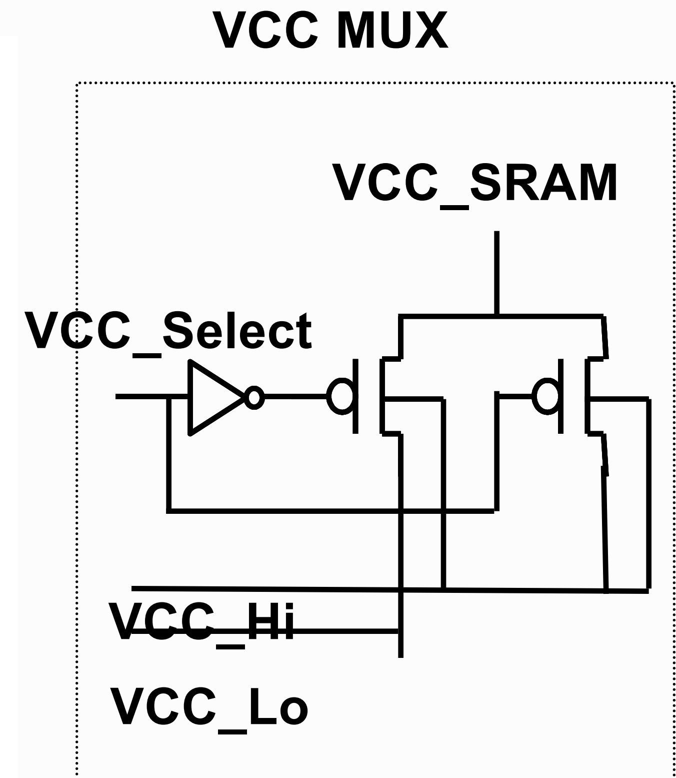
Dynamic Circuit Techniques for Variation Tolerant SRAM



	Read	Write
V_{WL}	Lower V_{WL} => lower V_{read} (weak AX)	Higher V_{WL} => Strong AX helps discharge
V_{cs}	Higher V_{cs} => lower V_{read} (strong PD) Higher V_{trip}	Lower V_{cs} => Weak PUP
V_{BL}	Weak impact	Negative V_{BL} for 0 => strong AX helps discharge

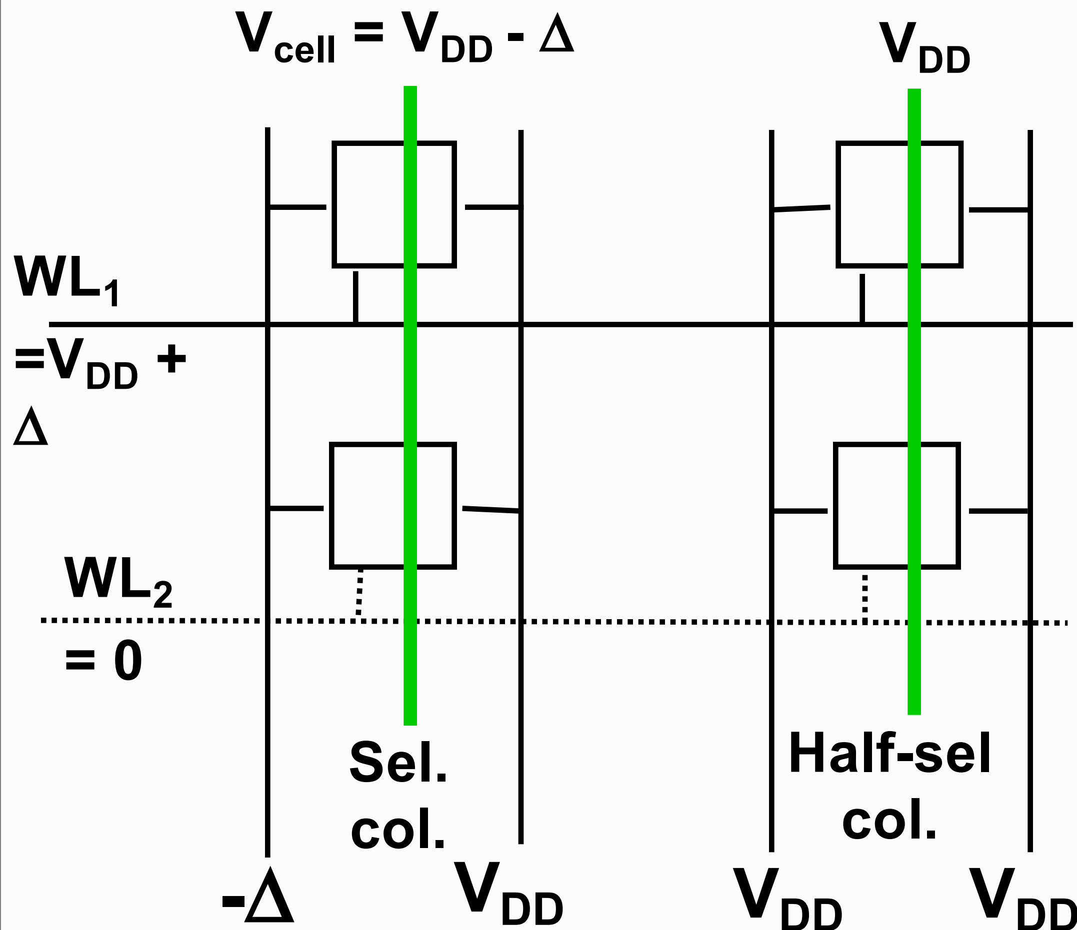
Example: Dual-Vcc based Dynamic Circuit Techniques





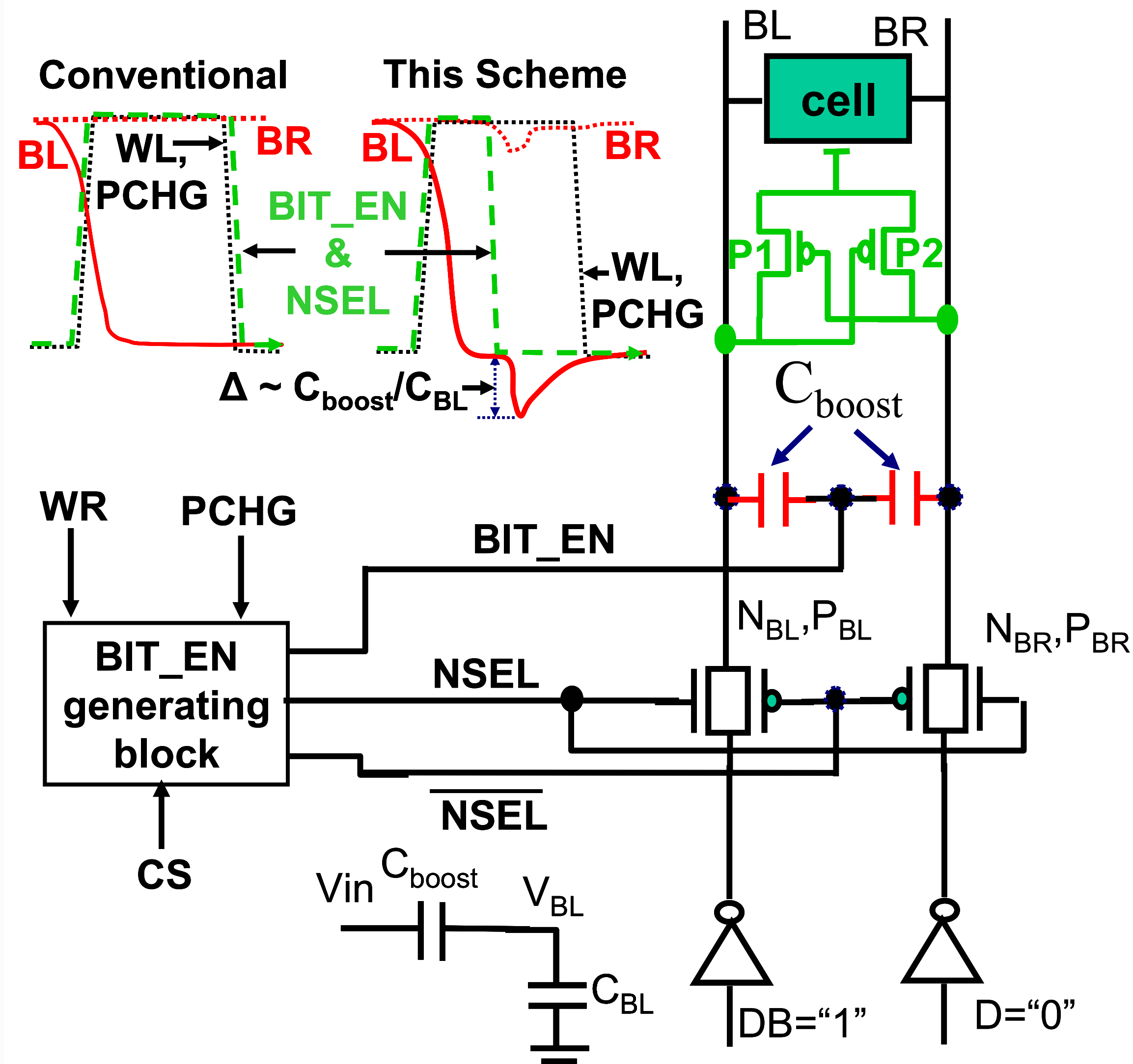
- Dynamic VCC MUX is integrated into subarray
- VCC selection is along column direction to decouple the Read & Write

Implementation Consideration: Half-Select Stability



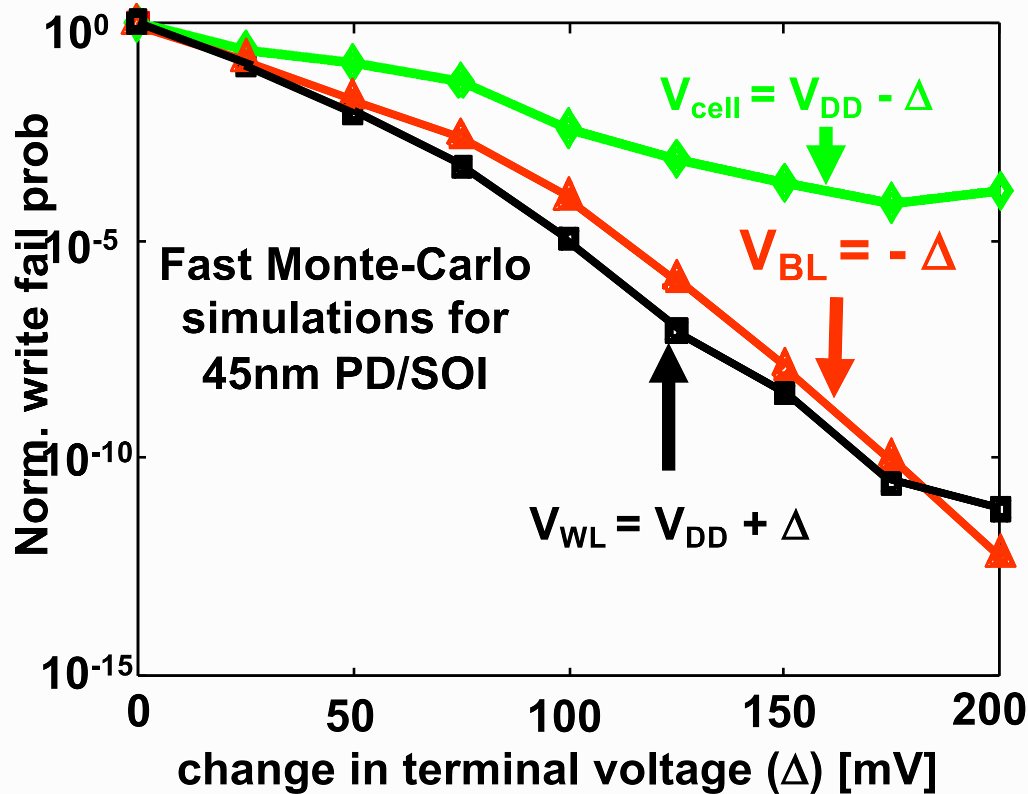
- **Higher V_{WL}**
  - **– Row-based scheme**
  - **– Degrades half-select read stability of the unselected columns**
- **Lower V_{cell} or negative bit-line**
  - **+ Column-based scheme**
  - **+ Half-select read stability remains same**

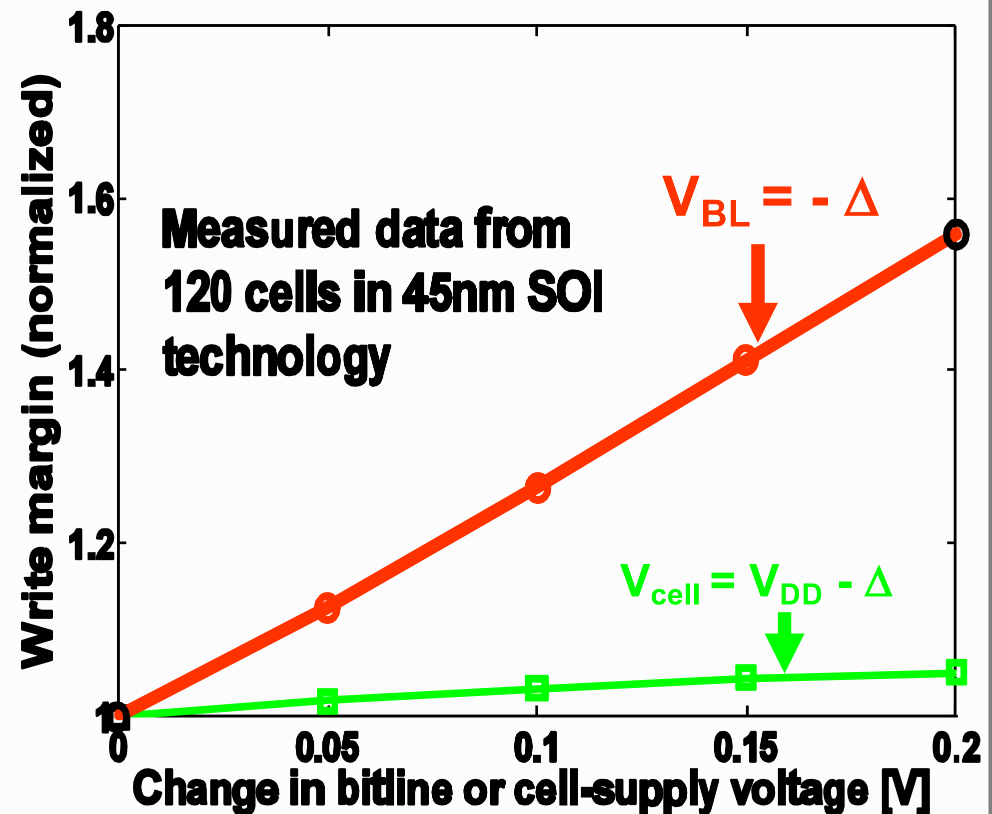
Negative Bit Line Scheme



Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Effectiveness Considerations: Writability improvement

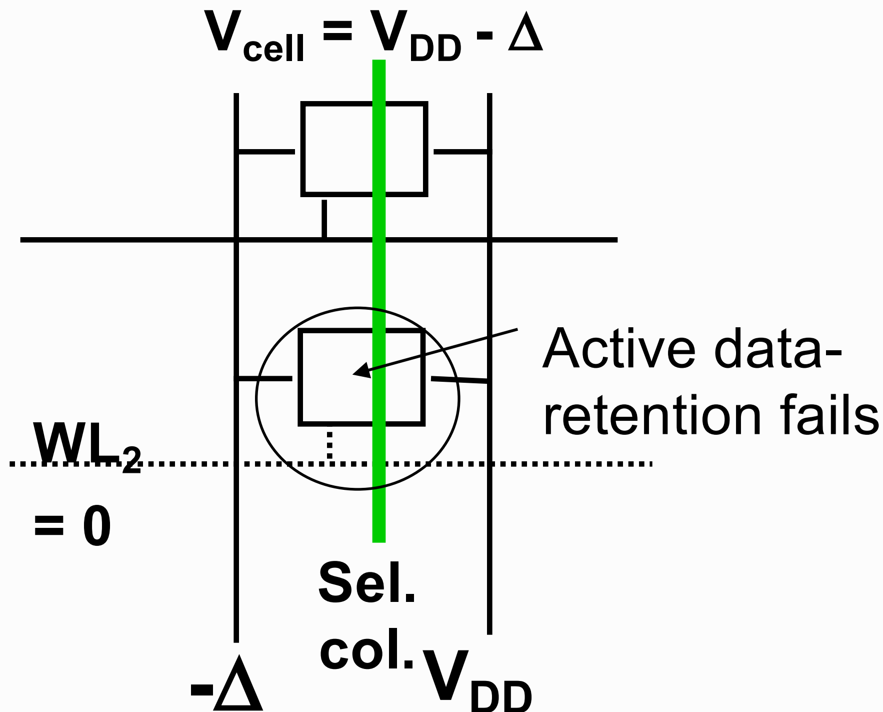


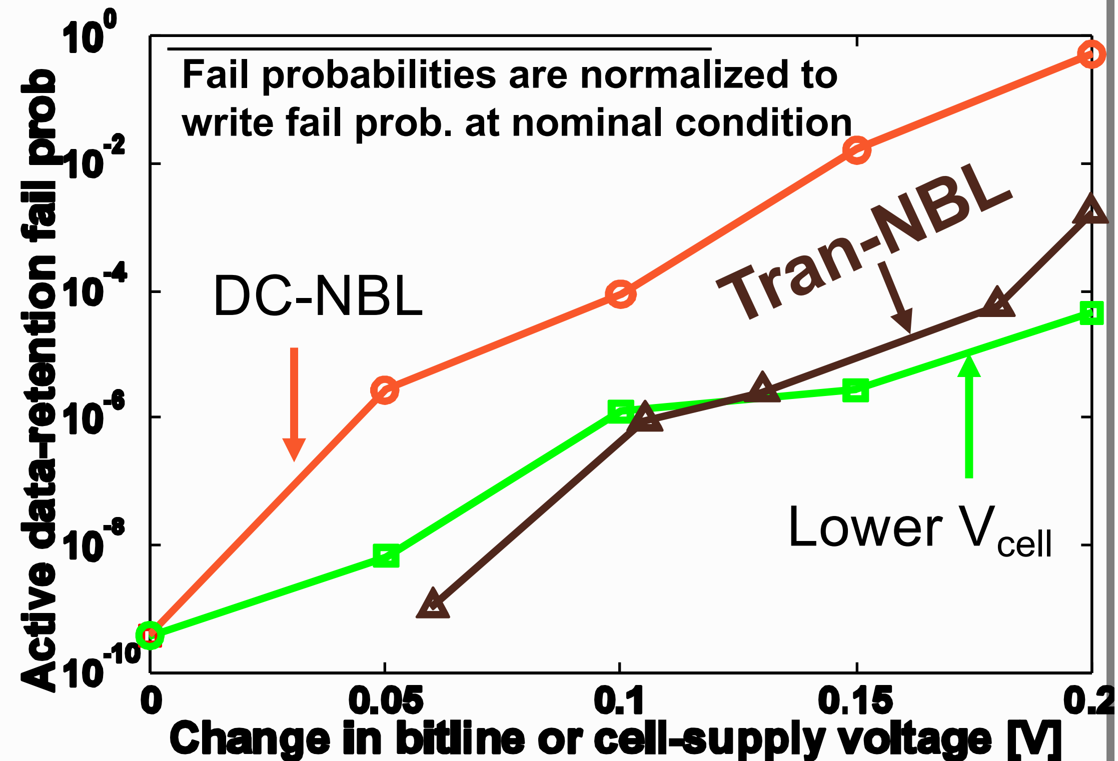


- Various dynamic schemes have different effectiveness in improving writability for similar read stability
  - Higher V_{WL} is most effective

Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Impact on Active Data-Retention





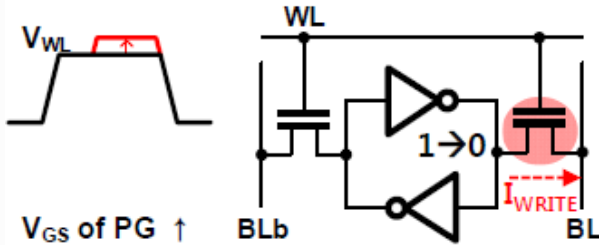
- Column based read-write control adversely impact the active data-retention failures
  - DC negative bitline has higher active data-retention failures
  - Tran-NBL and lower V_{cs} have comparable failure rates

Source: S. Mukhopadhyay, R. Rao et. al, TVLSI 2009

Assist Methods

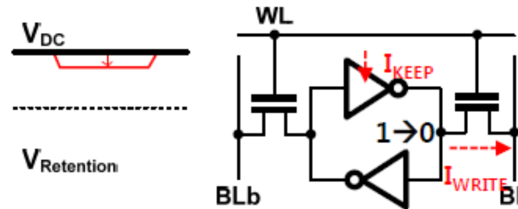
WLOD *(WL Overdrive)*

- Strengthen PG



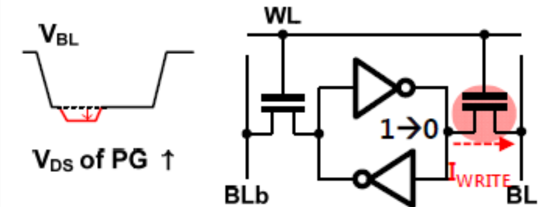
VCDL *($V_{DD,CELL}$ Lowering)*

Weaken PU



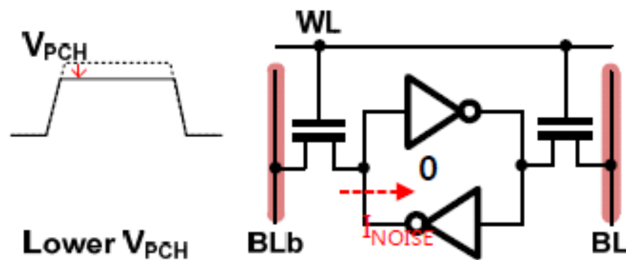
NBL *(Negative BL)*

- Strengthen PG



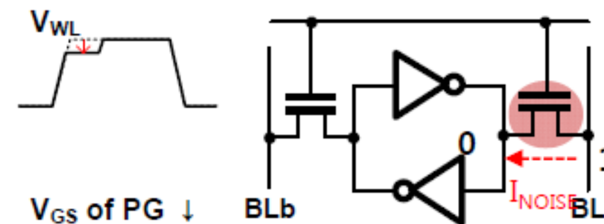
SBL *(Suppressed BL)*

Weaken BL noise



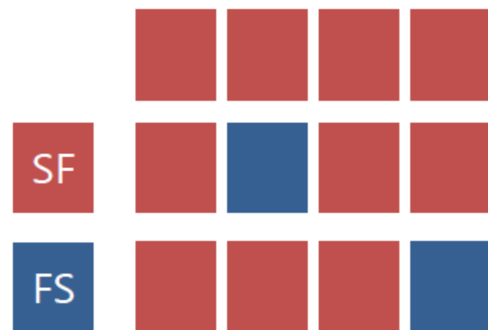
WLUD *(WL Underdrive)*

- Weaken PG

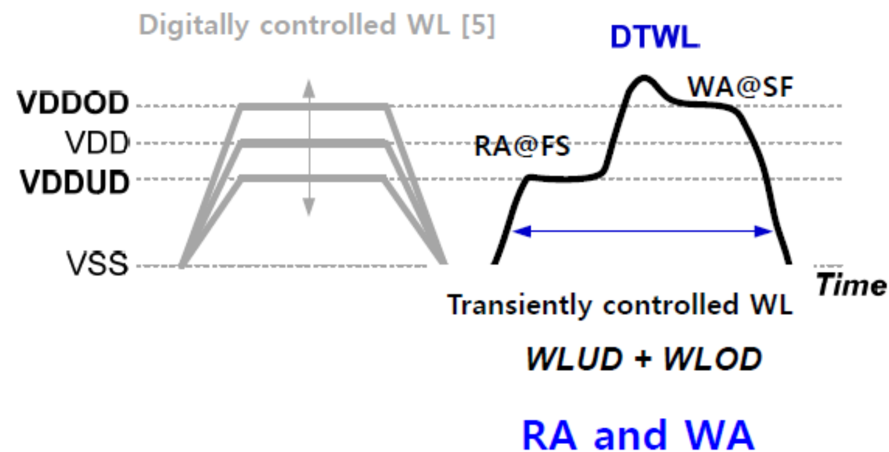


Proposed Dual-Transient WL (DTWL)

- Dual-Transient WL (DTWL) controls WL transiently
- DTWL provides mix-up assist for read and write
  - Covers different process-corner
  - DTWL mitigate the impact of WLOD (WA)



different process-corner



WLUD + WLOD

RA and WA

Question

- Of the various assist methods

a) Negative bit line scheme does not help 8-T sram cell

b) Word line under drive does not help 8-T sram cell

c) Word line over drive does not help 7-T conditionally decoupled sram cell

d) VCDL does not help any kind of assymetric sram cell

Block Diagram