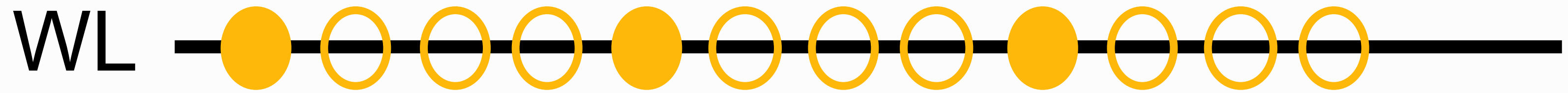
Class Exercise

- ❑ Build a schematic of a 6T – SRAM cell with minimum sized PFETs, Pull down = 3*PFET size, and Access transistor = 2* PFET size. Simulate it and plot butterfly curve for margins
- ❑ Change Pull down size to 4*PFET size and re-simulate
- ❑ Change Access transistor size to 3*PFET size and re-simulate
- ❑ Change pull up device size to 2 original size and re-simulate

Column Select and Half-Select Issue

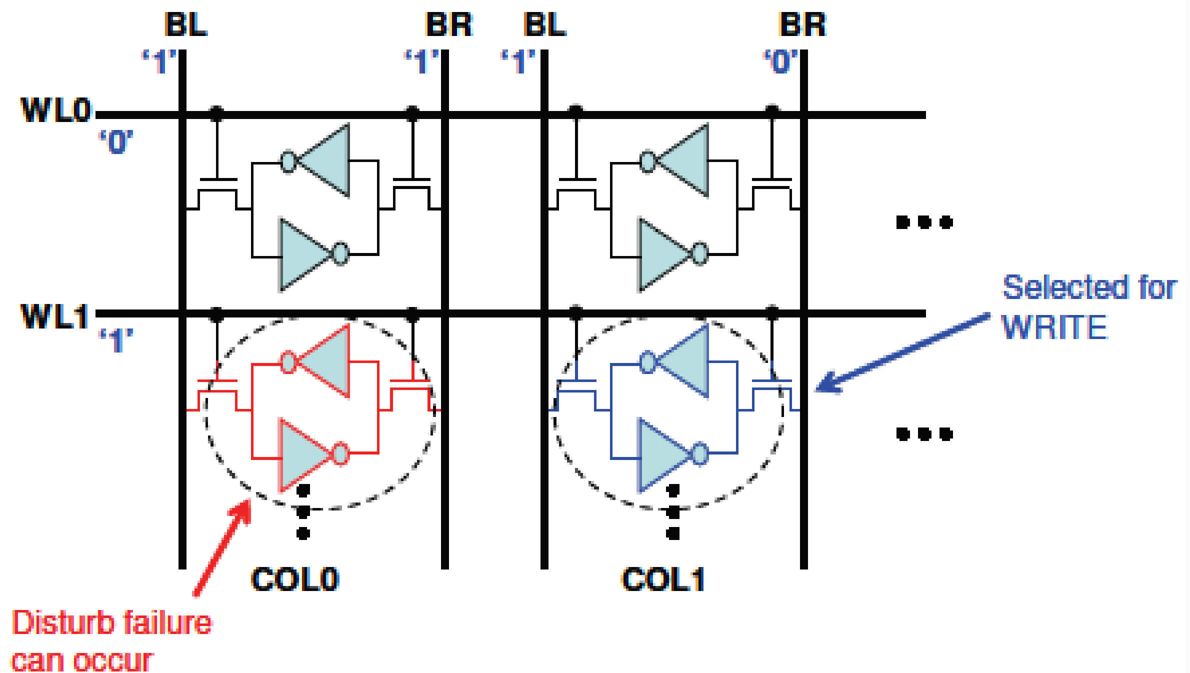


selected column

non-selected column

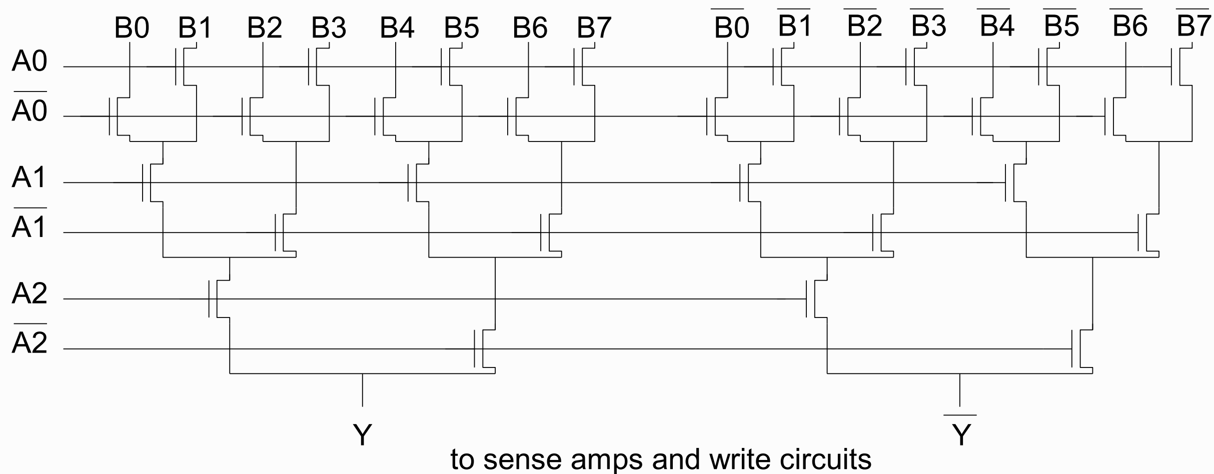
Prevents multiple-bit soft error

Better aspect ratio



Column Multiplexing

Sometimes, we read subset of bit line data (e.g: 128 columns → 16bit data I/O)
➔ Need to select part of bit lines to read-out.



No need to use complementary pass-gates. Only NMOS pass-gate is used. Why?

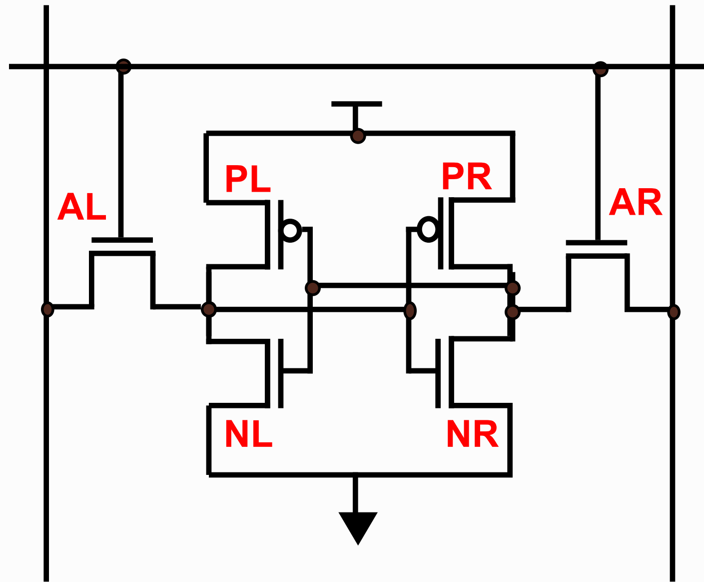
Learning Objectives for SRAM

- ❑ Articulate memory hierarchy and the value proposition of SRAMs in the memory chain + utilization in current processors
- ❑ Explain SRAM building blocks and peripheral operations and memory architecture (with physical arrangement)
- ❑ Articulate commonly used SRAM cells (6T vs 8T), their advantages and disadvantages
- ❑ Explain the operation of a non-conventional SRAM cells, and their limitations
- ❑ Explain commonly used assist methods
- ❑ Explain how variations impact memory cells

Topics

- Alternative Cell Types (6 to 10T), Asymmetric Cells, Sub-threshold Cells, Low – leakage cells

The Balancing Act



Large N: Better READ performance. If too large, trip voltage of inverter becomes so low that cell becomes unstable.

Large A: Better Performance. If too large, storage node voltage goes high during READ, causing cell flip

Large P: Increase stability. If too large, hard to WRITE

6-T Single Ended Read

R/WWL
WWL
PL
PR
AL
AR
Qb
Q
NL
NR
WBL
R/WBL

- Split word line for Read and Write
- Single-ended Read / Differential Write
- Full swing domino Read with short bit line

READ : R/WWL = VDD and WWL = GND

WRITE: R/WWL = VDD and WWL = VDD

Refresher Question

- Decreasing the size of only one side of NFET transistors will improve the cell

a) **Cell density**

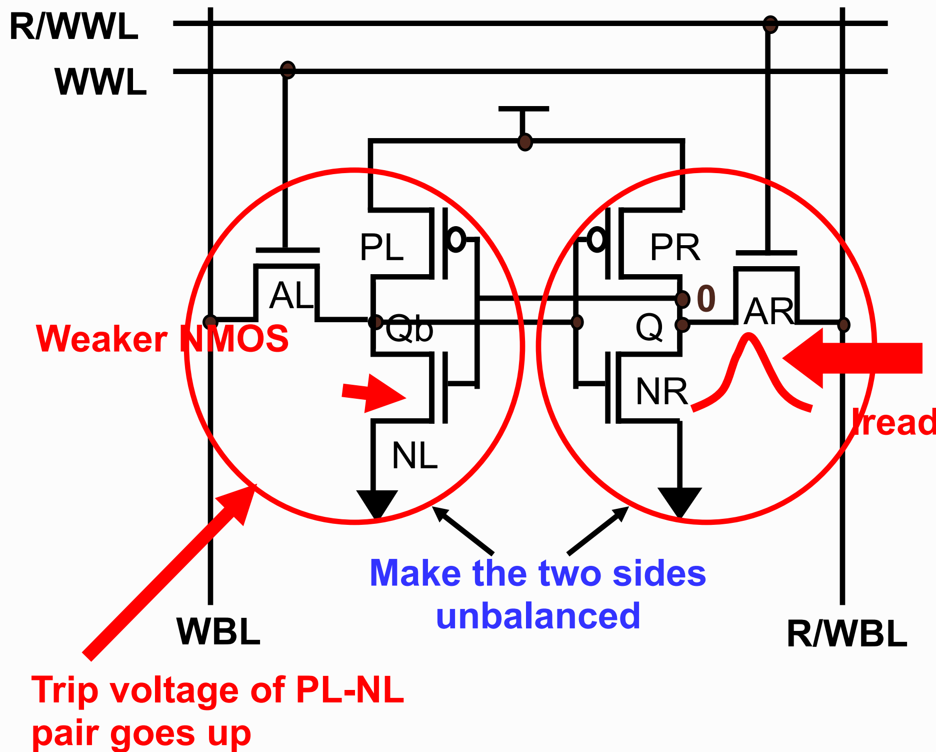
b) Read margin

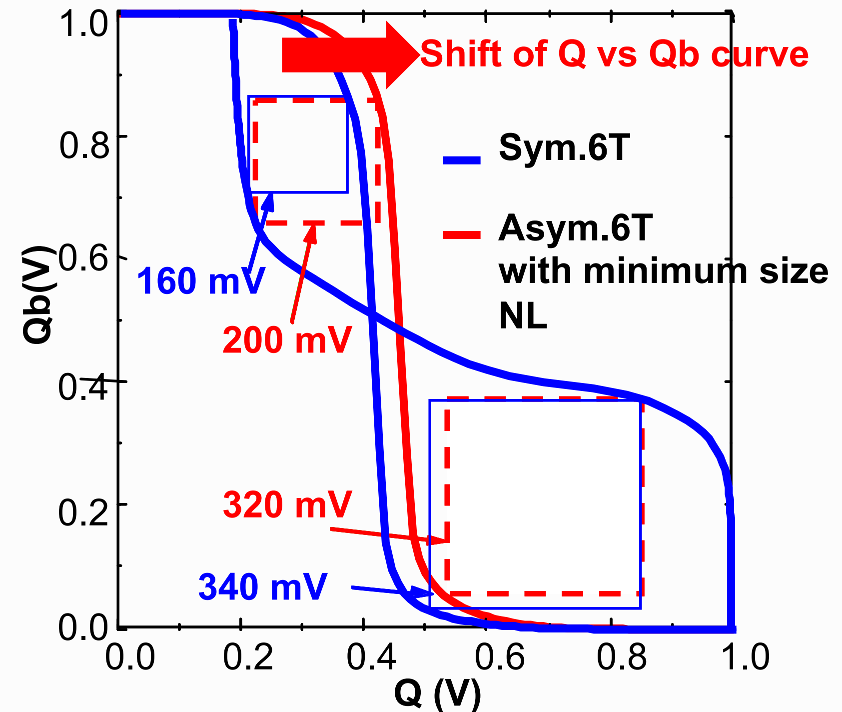
c) Write margin

d) Hold margin

Asymmetrical 6T SRAM: Device Sizing

- Read word-line separated from Write word-line
- Single-ended Read, differential Write



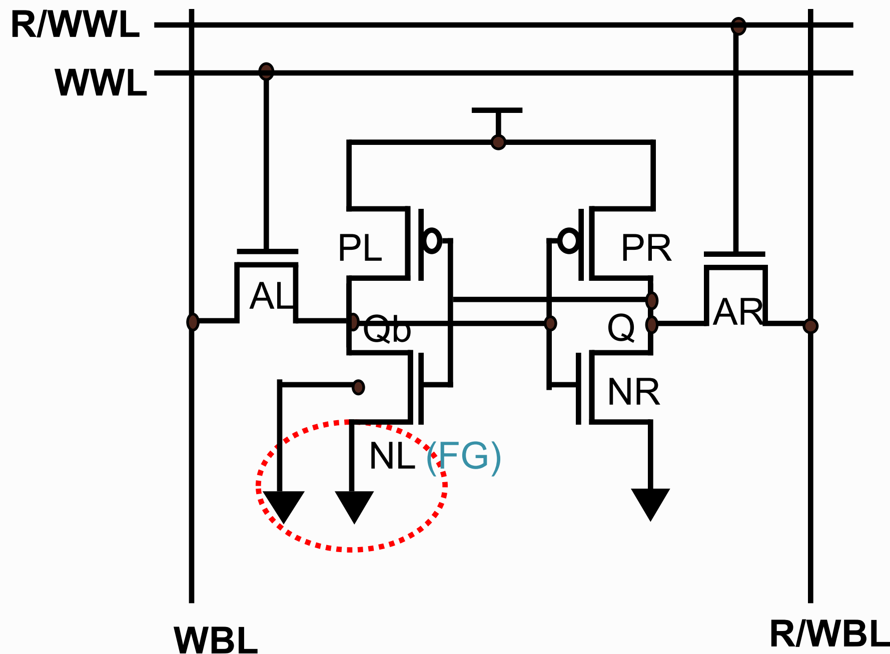


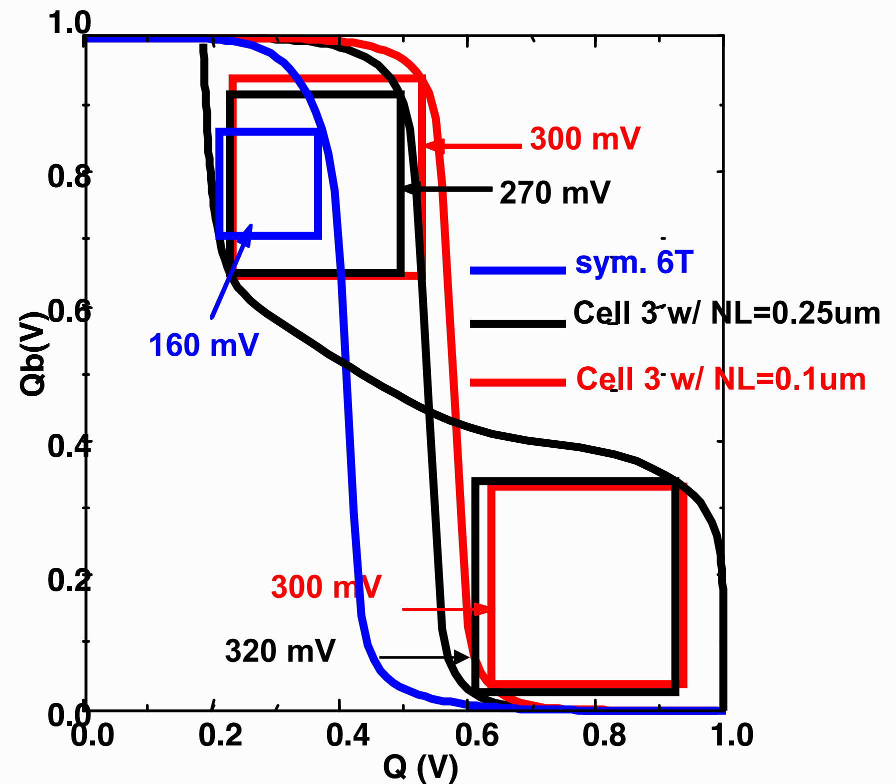
Asymmetry could be achieved through VT selection as well

(J. Kim, ESSCIRC, 2006)

6T Asym SRAM in Double Gate Technologies

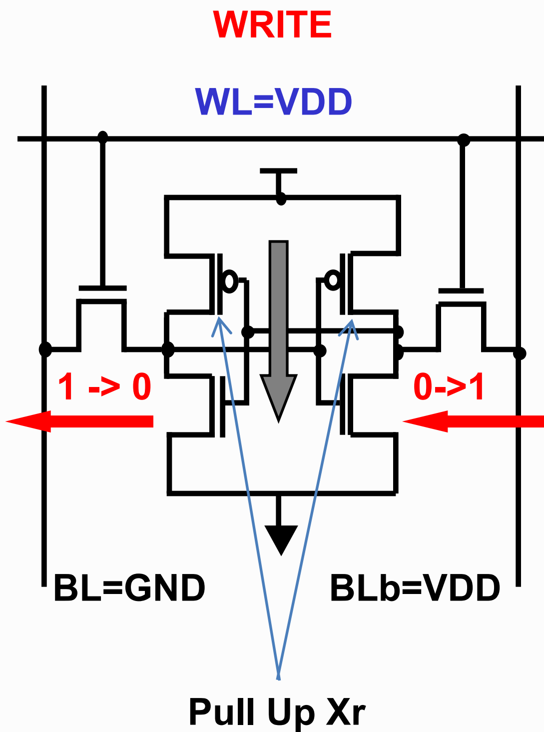
- Bias back-gate of NL to GND. Front-gate as cell device & sizing down NL
- Left and Right SNM become comparable
  - Optimal SNM of asymmetrical cell

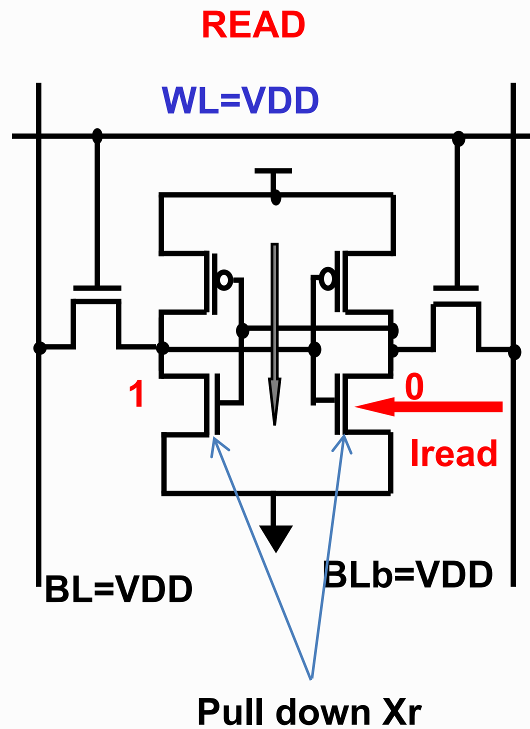


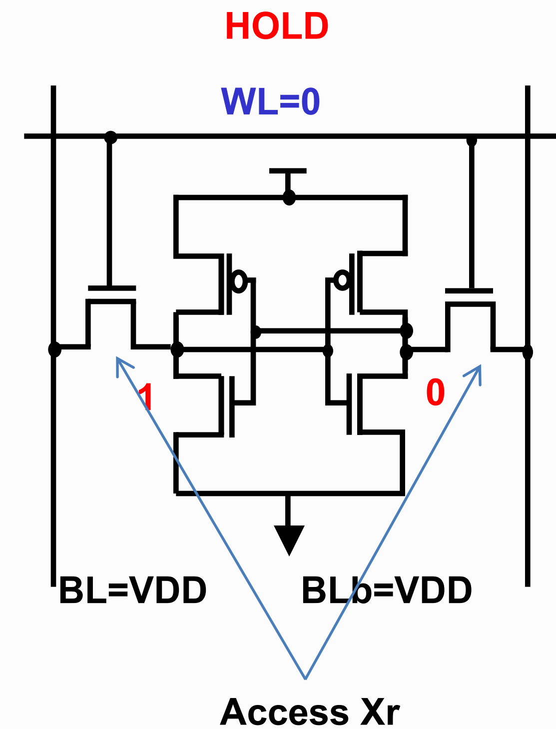


(J. J. Kim et al., ESSCIRC, 2006)

Workhorse 6T-Cell





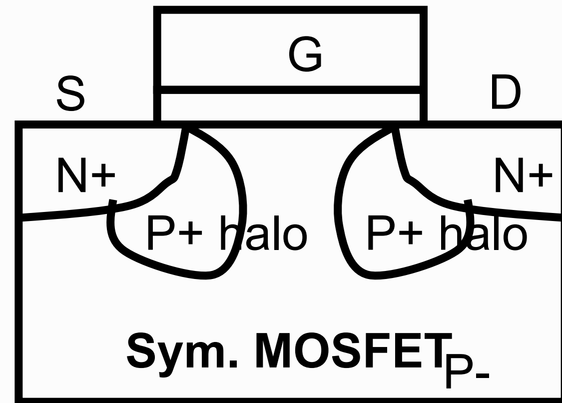


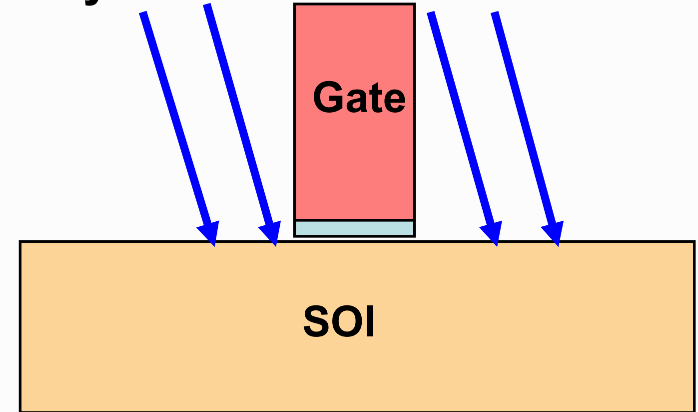
Access Xr: On
Data driven on bit - lines
Data Flipped by over-coming pull-up / pull – down Xrs

Acess Xr: On
BL, Blb pre-conditioned, and then floated, one line discharges thru the cell (Iread), voltage sensed, Data Retained

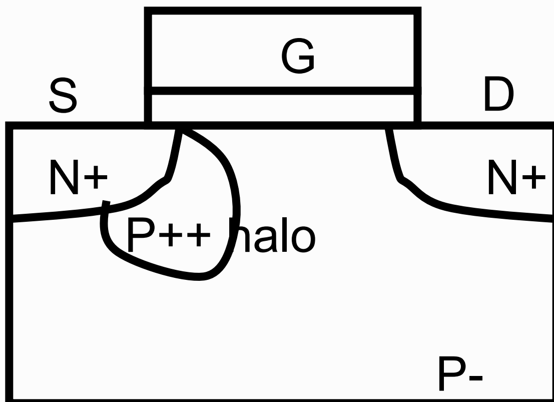
Access Xr : Off
Data Retained, due to back-to-back inverters

Asymmetric MOSFET

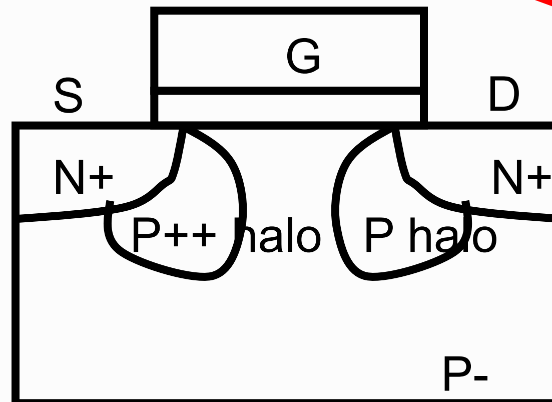




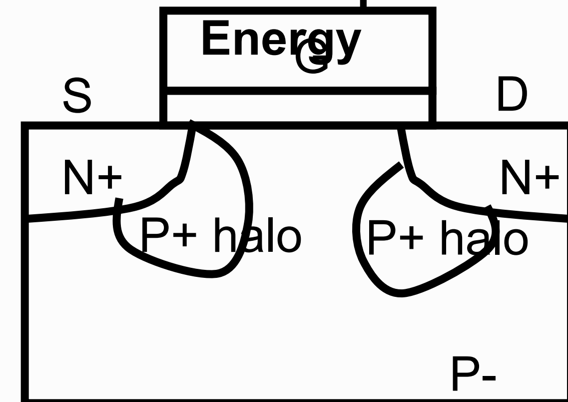
Single Sided Halo



Modified Halo



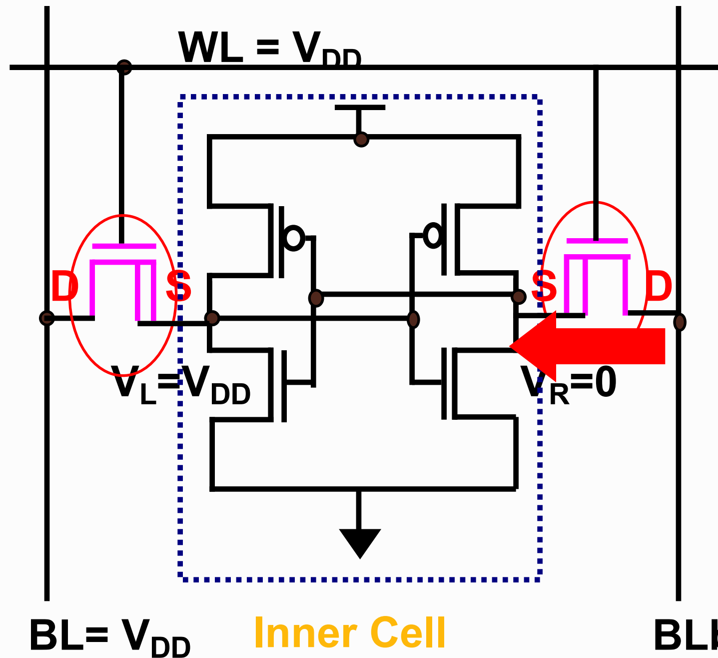
Modified Implant Energy

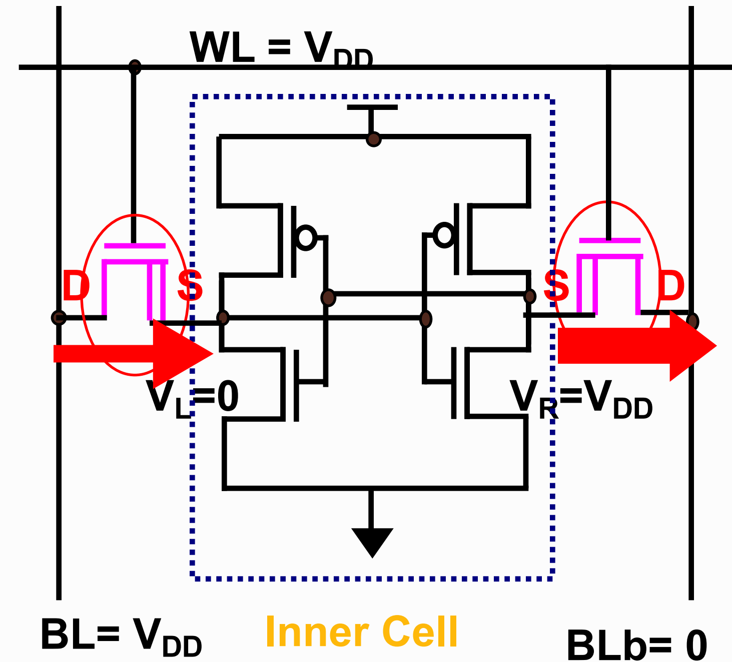


Asymmetric MOSFET can be realized in multiple ways

Net Effect: I (drain – source) ≠ I (source – drain)

Asymmetric Access Transistors





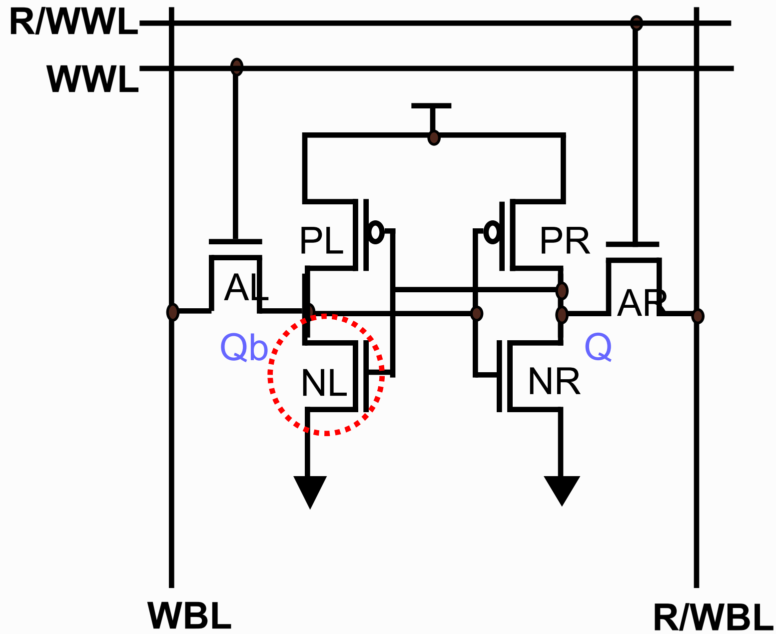
Read Operation

- Access Transistor in Fwd Mode
- Weaker than in Sym. Case
- Read Disturb Noise Reduced

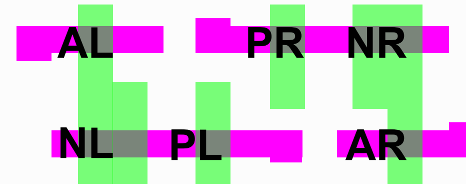
Write Operation

- L and R Access Transistor in Fwd and Rev Mode respectively

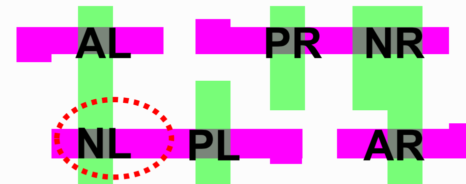
Asymmetric 6-T Cells



Sym

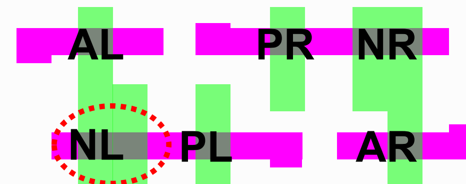


Asym Size



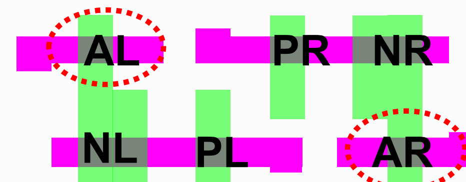
Straight Active region

Asym Vt



Higher Vt doping

Asym Device



S-D are distinct

(J. Kim, CICC 2010, J. Kim EDL 2011)

Question

- Which of the following is not true wrt asymmetric 6-T sram cell

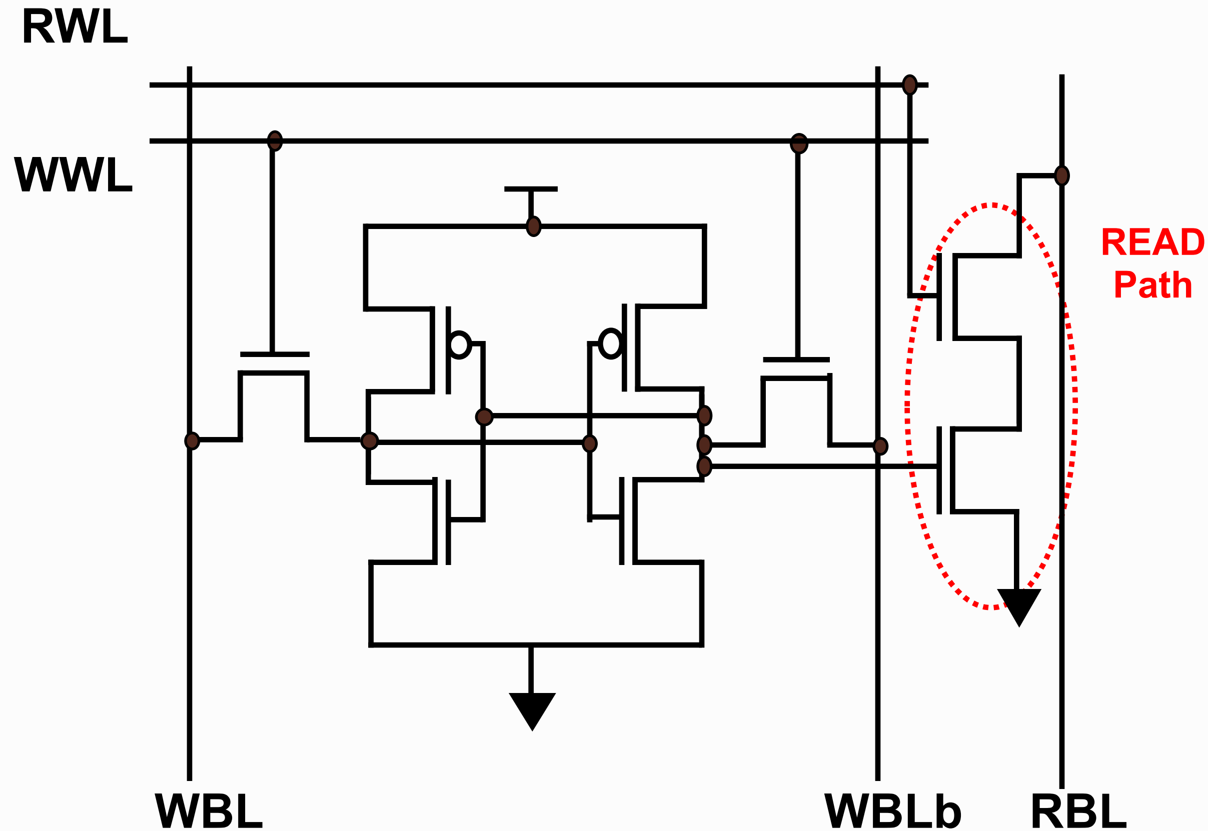
a) Assymetric transistors can be used for pull down and access transistors

b) Assymetric sizing based sram cell has reduced pull down width on the side opposite to the read bit-line

c) Assymetric VT based sram cell does not provide any area benefit

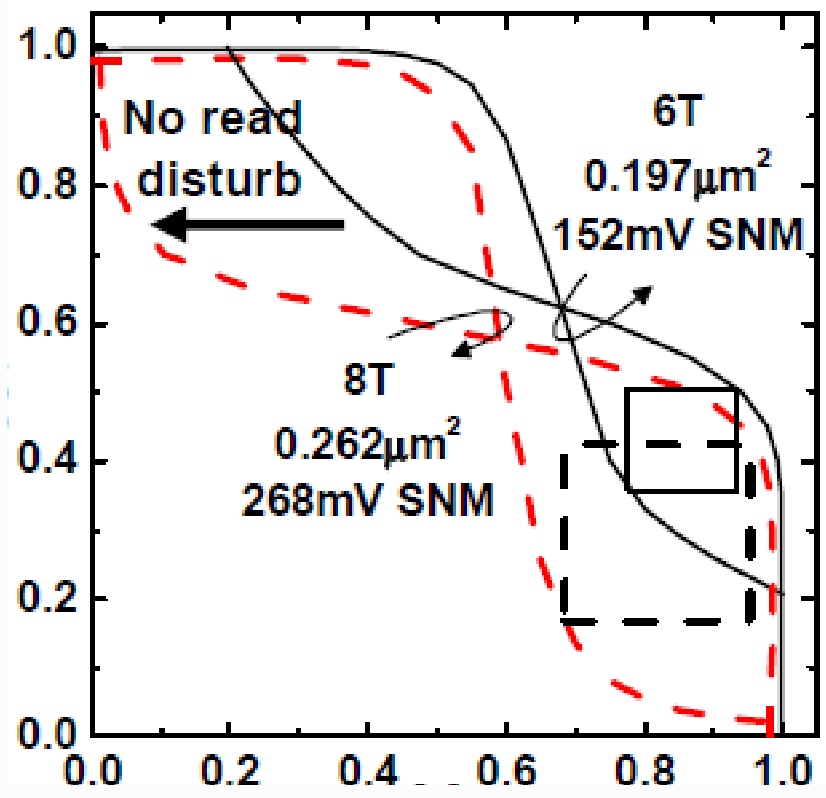
d) All asymmetric transistor sram cells need single ended read

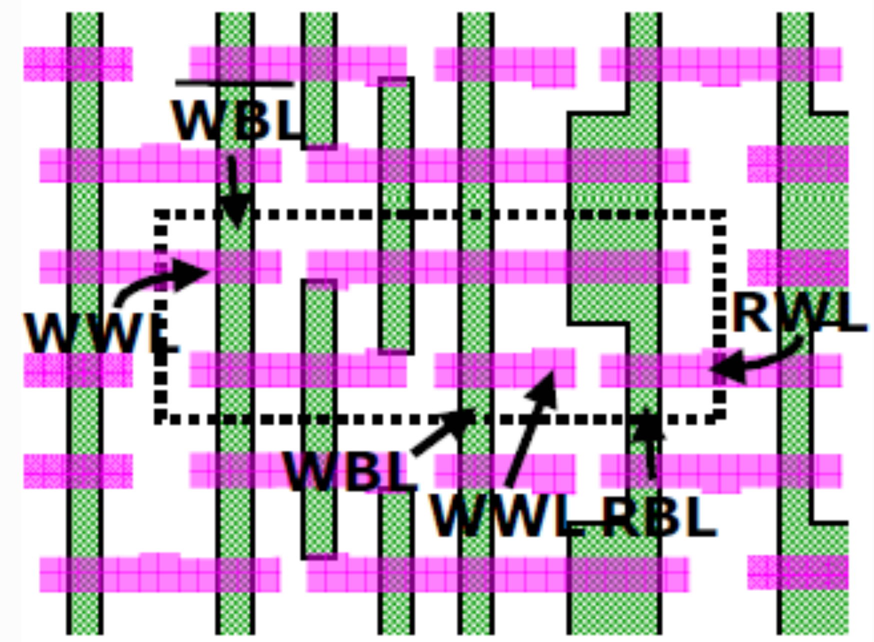
Decoupled Read – Write Bitlines



(L. Chang et al, VLSI Symp 05)

Decoupled Read – Write Bitlines

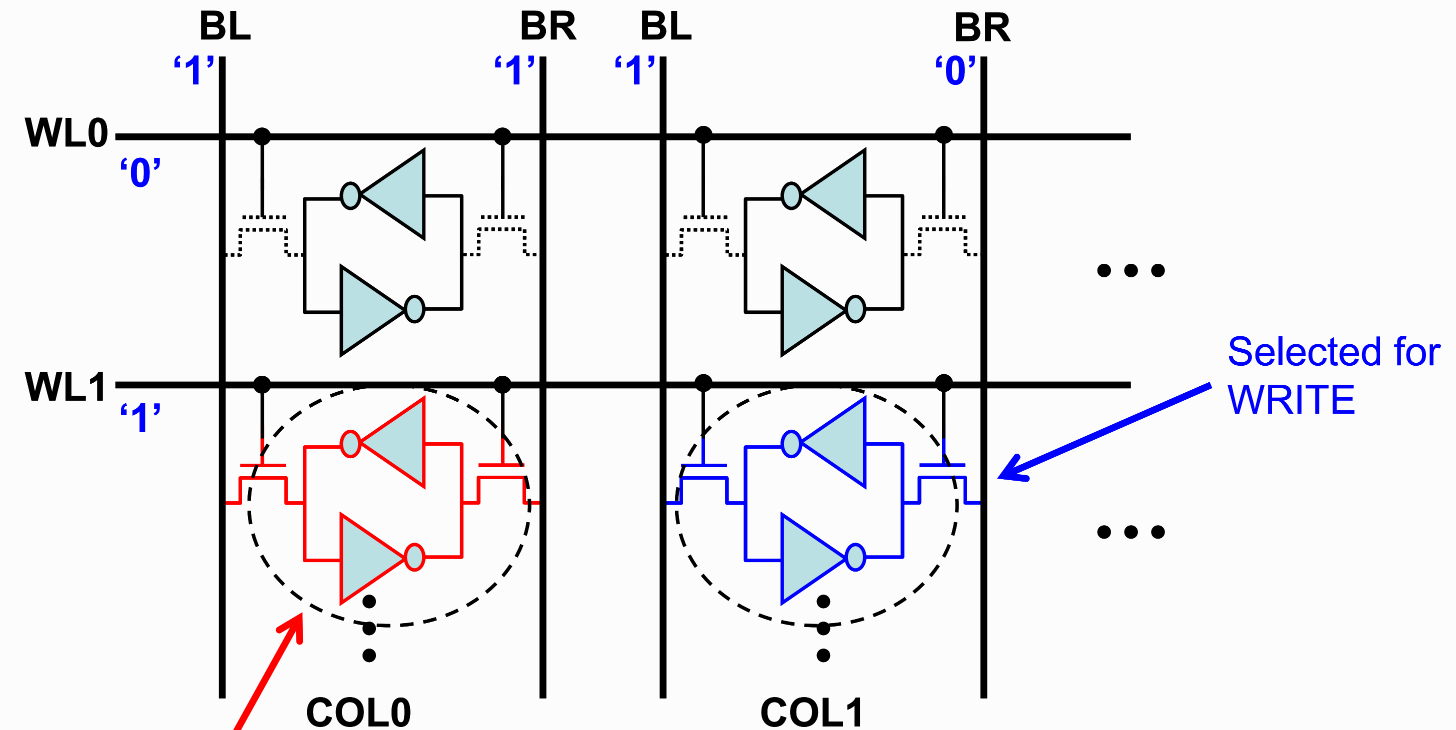




(L. Chang et al, VLSI Symp 05)

Half-Select Disturb

- During a Read or Write operation, half-selected cells on the selected word-line are actually experiencing “Read” operation
  - Disturb similar to Read-disturb



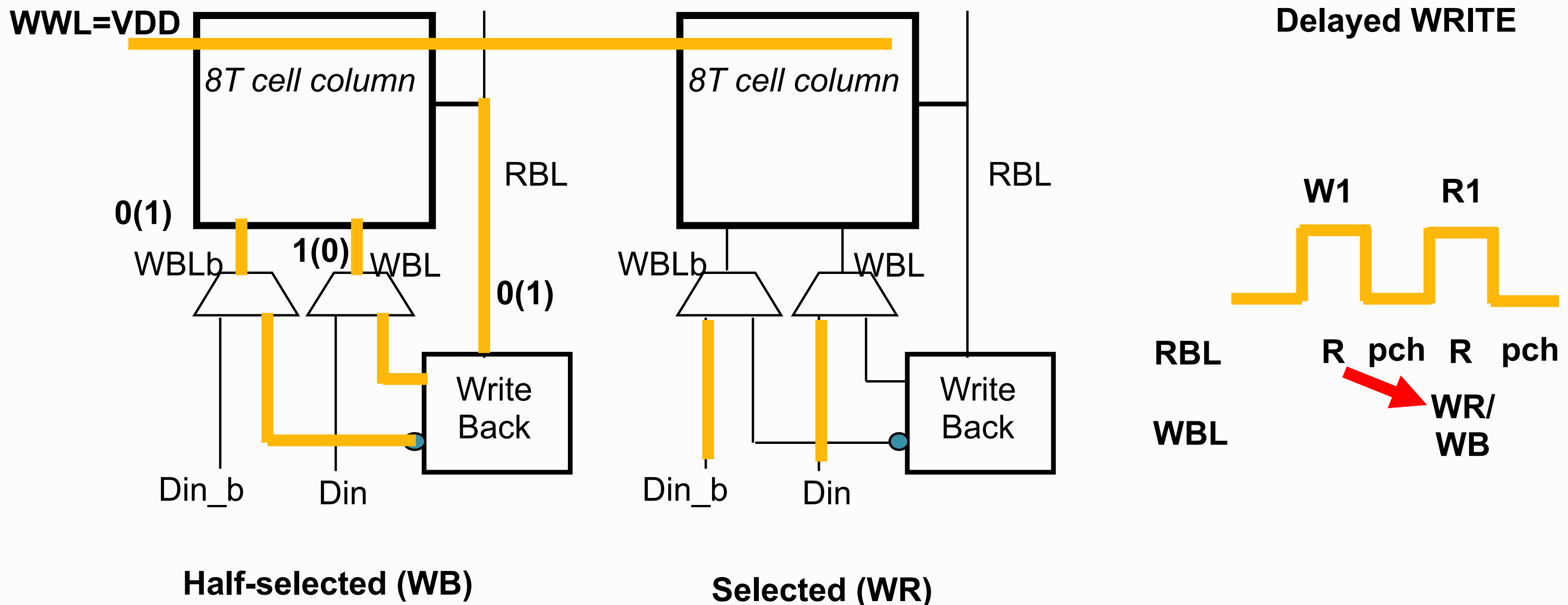
Half-Select in 8T

- Array architecture approach
  - No column select. Floorplan such that all bits in a word are spatial adjacent

- Gated Write wordline signal (Byte Write)
  - Local Write wordline "on" only for the selected block

- Write-back scheme
  - RWL activated even during Write, all cell data in selected WL read out to D-latches
  - Dataout is then written back to half-selected cells

Delayed Read-Modify-Write



- Allow the column-select in 8T cell array by replacing "WRITE" with "READ-MODIFY-WRITE"
- One cycle delayed WRITE: Relaxed timing, No bandwidth loss

Question

- Which of the following is true wrt decoupled Read-Write 8T SRAM Cell

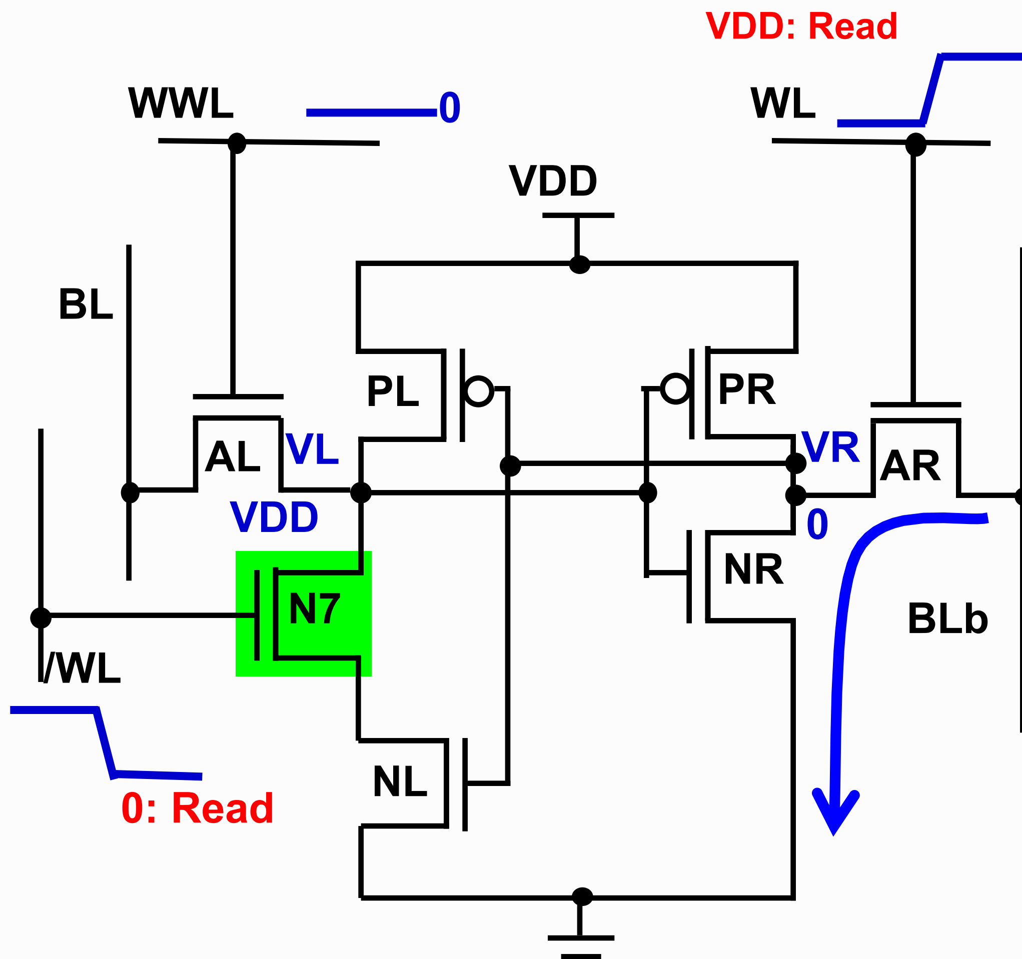
a) The RBL needs to be on the side of the BL-bar

b) It is possible to be read and write to the different cell in the same column

c) The 6-T portion of the SRAM cell is optimized for 'hold' operation

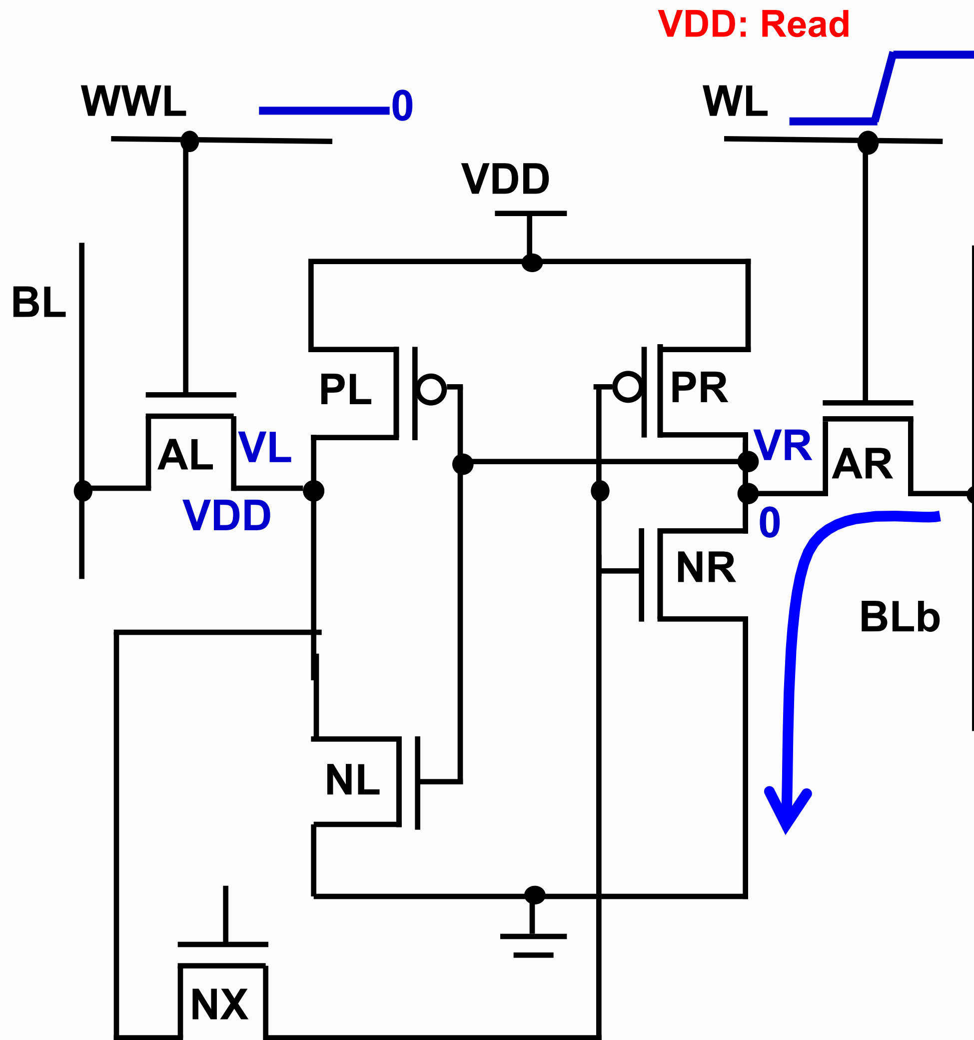
d) Memory folding cannot be done with 8-T cells

Conditionally decoupling regeneration

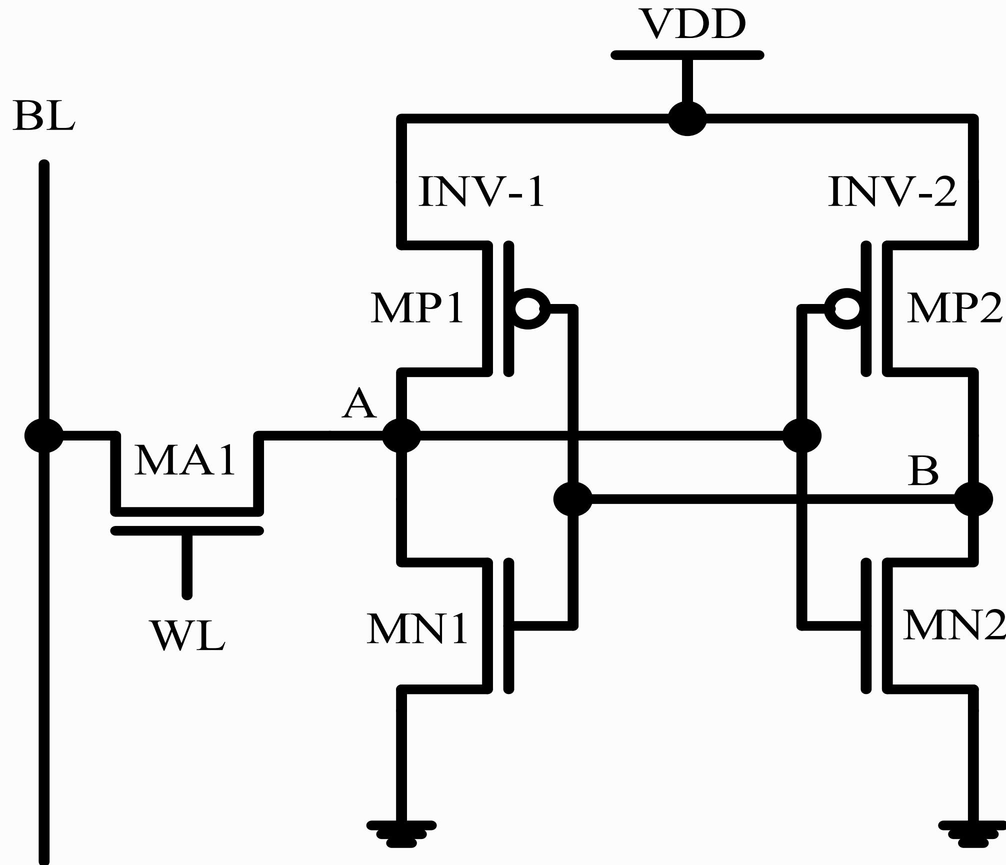


(K. Takeda et al, ISSCC 05)

Conditionally decoupling regeneration



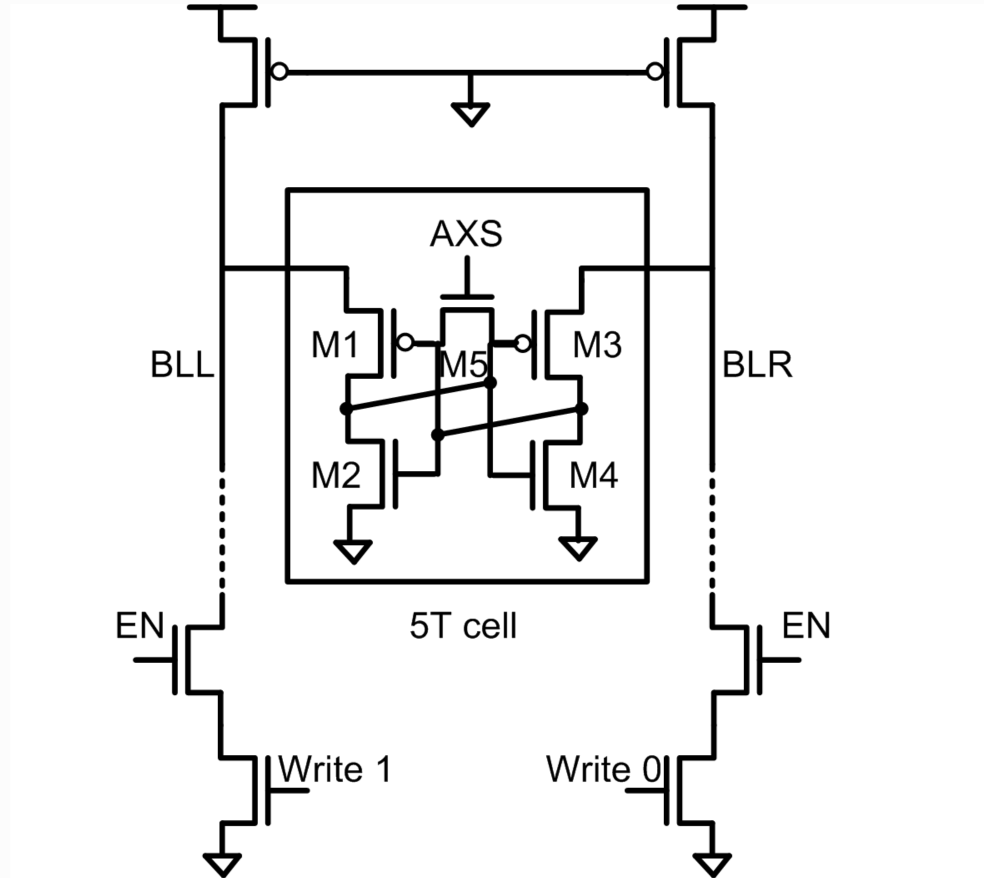
5T SRAM



5T Sram with floating ground

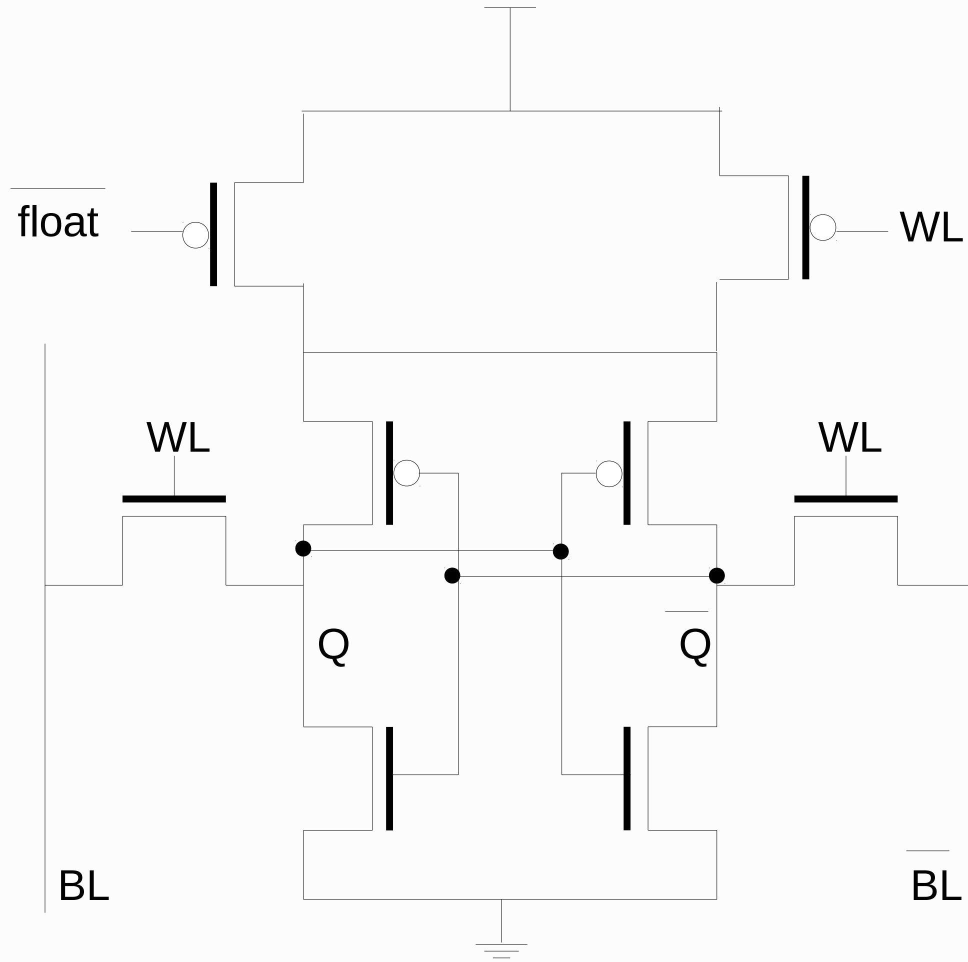
(K. Takeda et al, ISSCC 05)

Portless SRAM cell

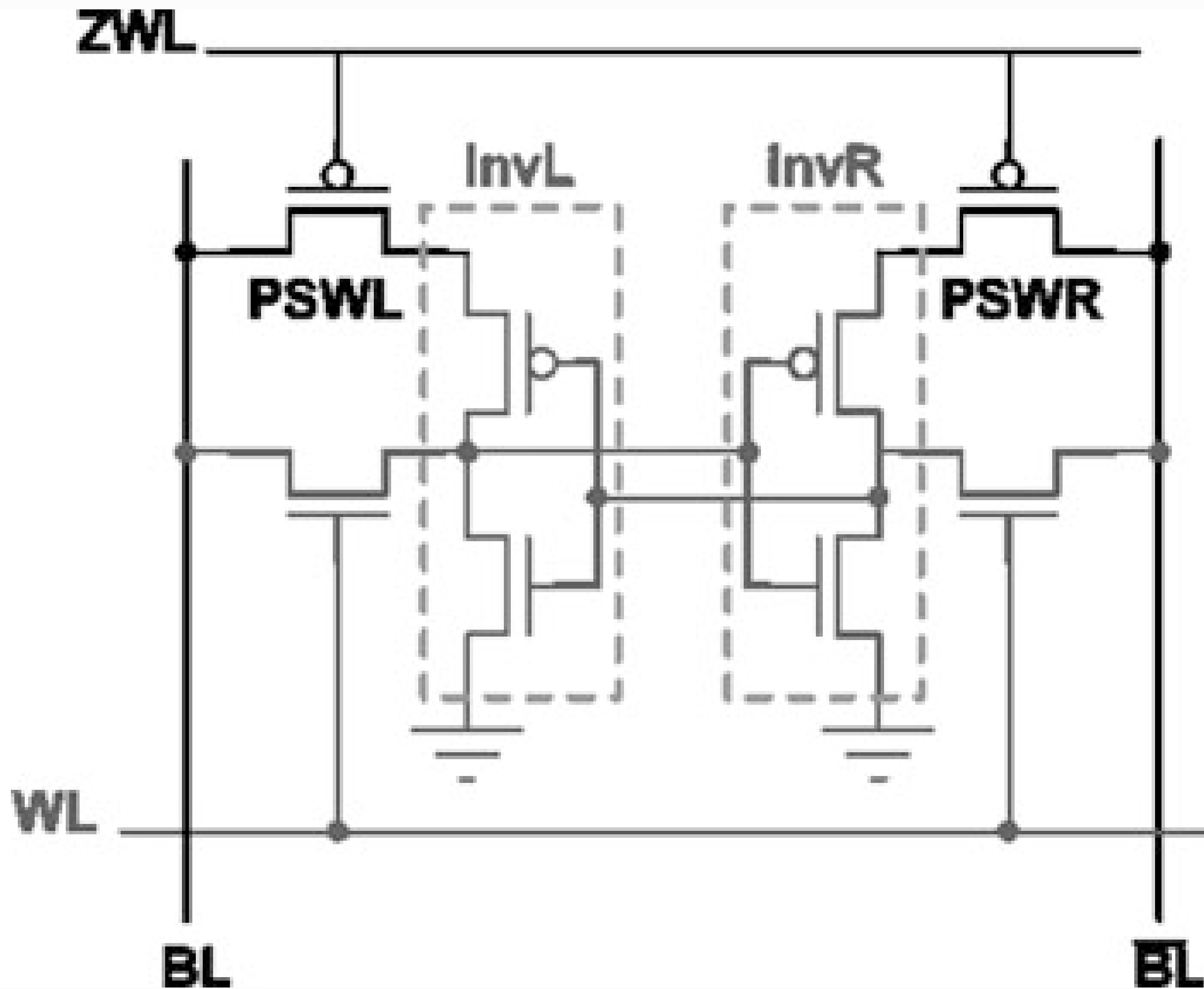


(K. Takeda et al, ISSCC 05)

Modifying power supply

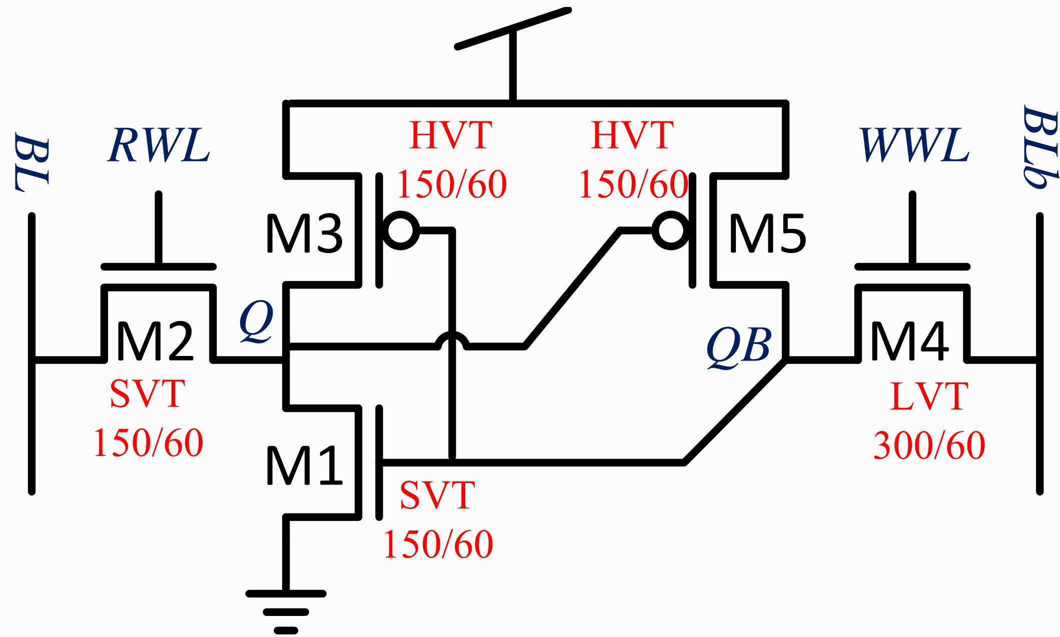


Differentially Data Aware Power Supplied



(Chang, 2009a)

5T SRAM



(Adam , et. al)

Question

- Which of the following is not a useful approach

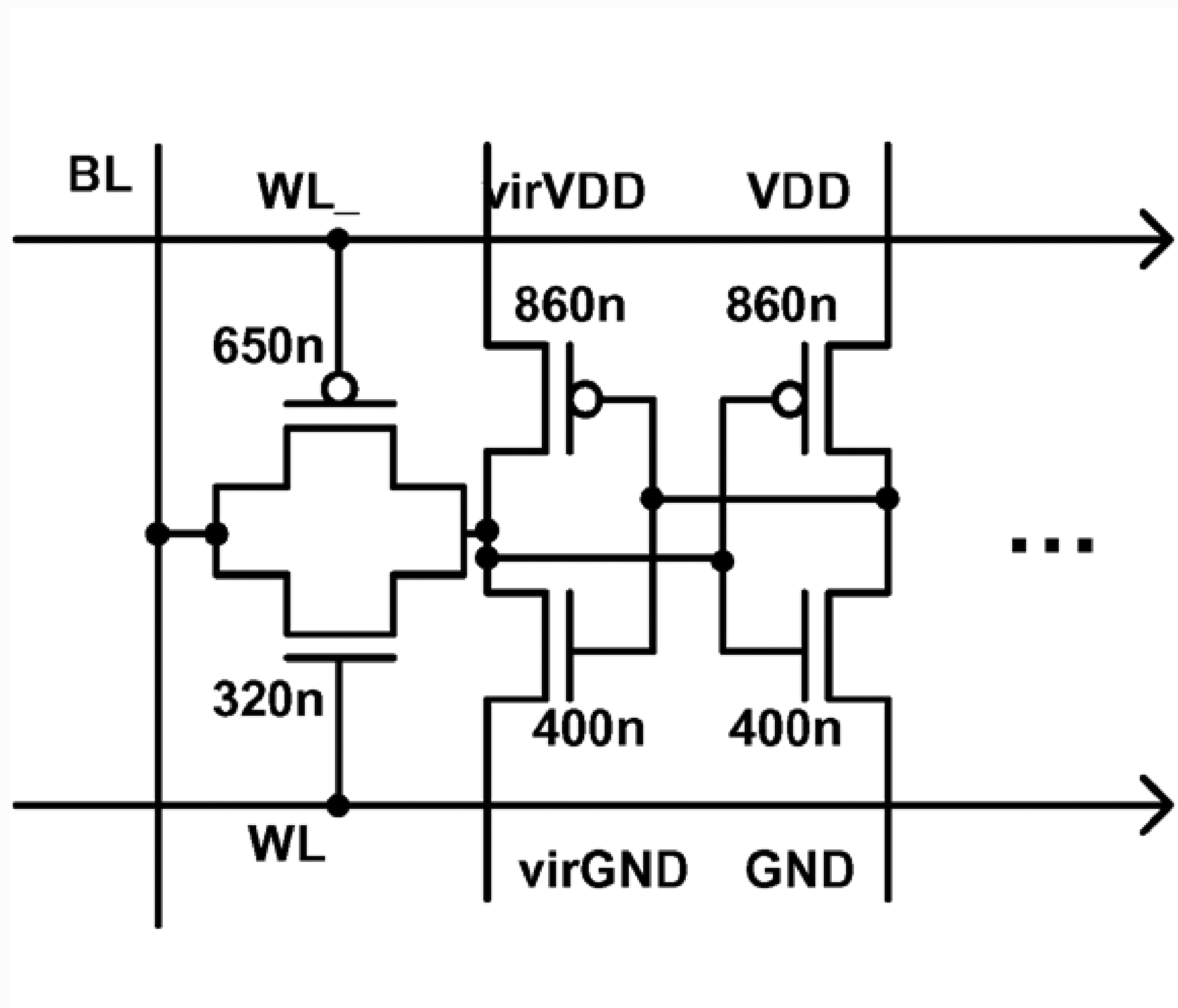
a) Conditionally break the back to back inverters during read operation

b) Conditionally break the back to back inverters during write operation

c) Conditionally float the cell supply depending on the data being written

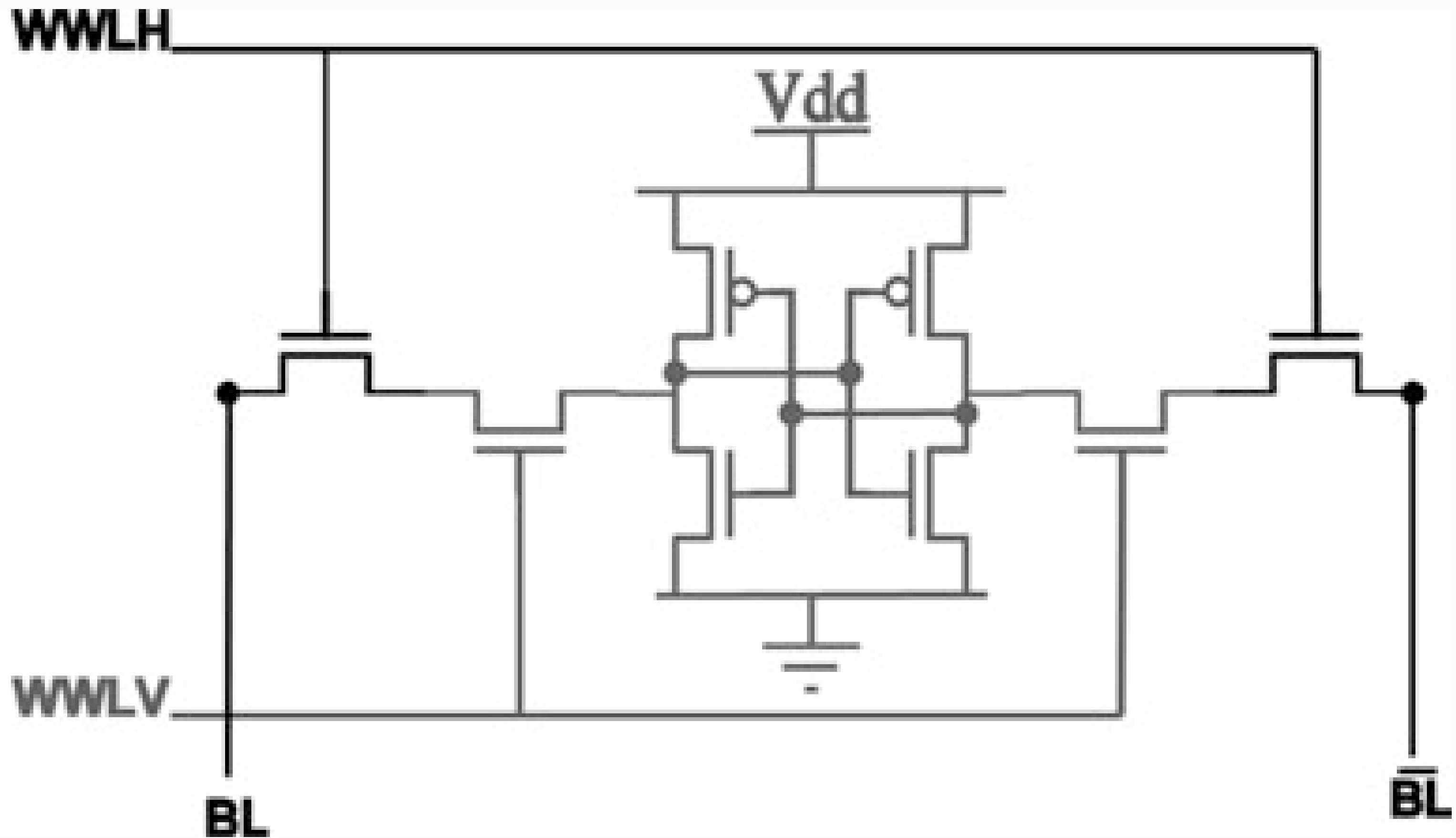
d) Conditionally disconnect the ground connection during write operation

Sub-threshold 8-T SRAM



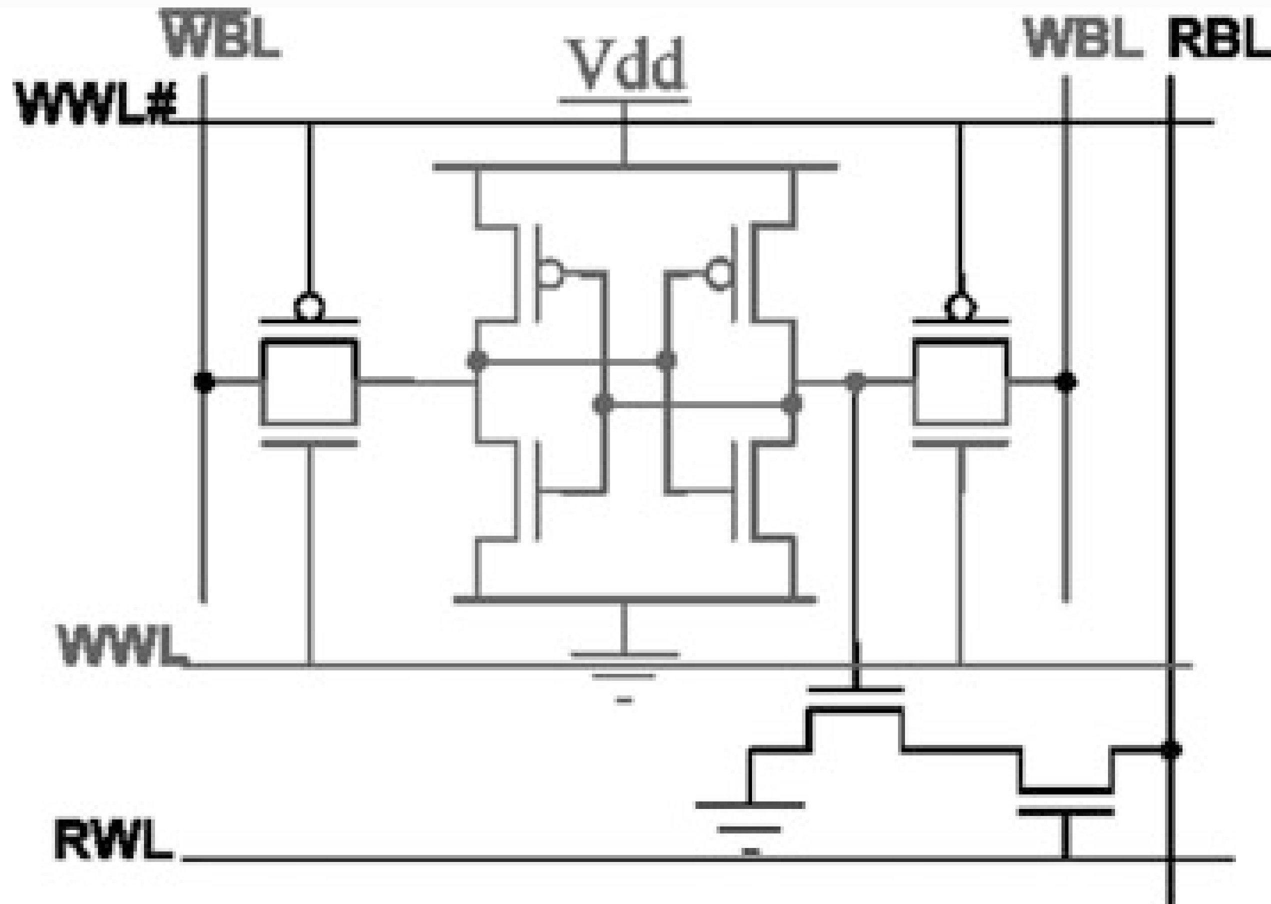
(B. Zhai, JSSC 08)

Horizontal and Vertical Word Line Cell



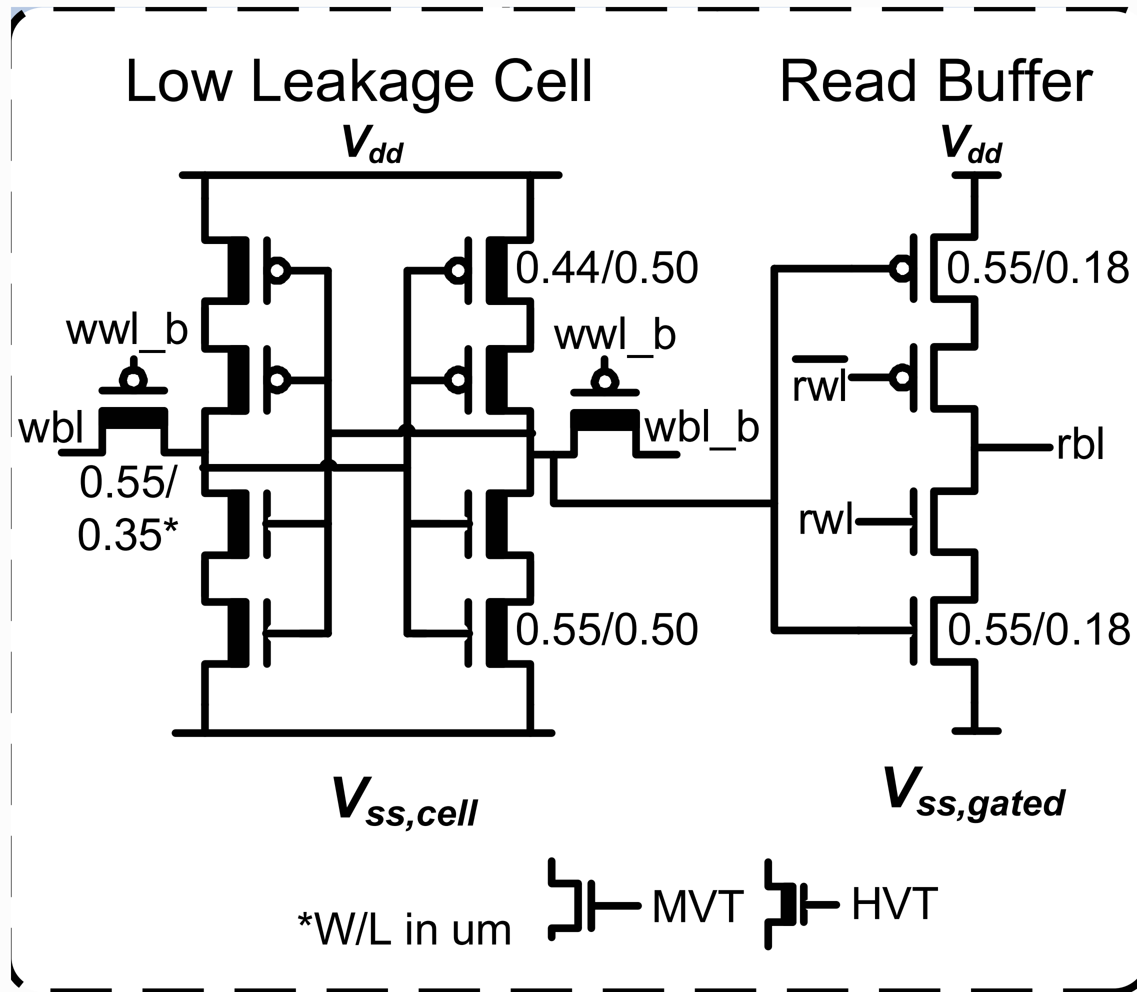
Yaabuchi, 2009

Dual Ended Transmission Gate Cell



(Agarwal, 2010

Low leakage SRAM



The Phoenix Processor: A 30pW Platform for Sensor Applications

(S. Hanson , VLSI Symp '08)

Question

- An SRAM cell with multiple word lines (read or write)

a) Enables both read and write operation at the same time

b) Reduces cell access failure due to ’beneficial’ coupling

c) Is likely to become wiring limited as technology scales

d) Improves hold margin of the cell

Next Class

- Impact of variation on sram stability and assist circuits

References

- **A 40 nm Sub-Threshold 5T SRAM Bit Cell with Improved Read and Write Stability**

Adam Teman, Student Member, IEEE, Anatoli Mordakhay, Janna Mezhibovsky and Alexander Fish, Member, IEEE

- **A Variation-Tolerant Sub-200 mV 6-T Subthreshold SRAM**

Bo Zhai, Scott Hanson, *Student Member, IEEE*, David Blaauw, *Member, IEEE*, and Dennis Sylvester, *Senior Member, IEEE*

- **The Phoenix Processor: A 30pW Platform for Sensor Applications**

Mingoo Seok, Scott Hanson, Yu-Shiang Lin, Zhiyoong Foo, Daeyeon Kim, Yoonmyung Lee, Nurrachman Liu, Dennis Sylvester, David Blaauw

References

- Agarwal et al., A 32 nm 8.3 GHz 64-entry 9 32b **Variation Tolerant Near-Threshold Voltage Register File**. Symposium on VLSI Circuits Digest of Technical Papers, pp. 105–157 (2010)
- B.H. Calhoun et al., **A 256 k Sub threshold SRAM Using 65 nm CMOS**. Proceedings of IEEE International Solid-State Circuits Conference (ISSCC), pp. 628–629, Feb 2006
- L. Chang et al., **Stable SRAM Cell Design for the 32 nm Node and Beyond**. Symposium on VLSI Circuits Digest of Technical Papers, pp. 128–129 (2005)
- L. Chang et al., **An 8T-SRAM for variability tolerance and low-voltage operation in high- performances caches**. IEEE J. Solid-State Circuits, 43, 4, April (2008)

References

- M.F. Chang et al., A Differential Data Aware Power-supplied (D2AP) **8T SRAM Cell with Expanded Write/Read Stabilities for Lower VDDmin Applications.** Symposium on VLSI Circuits Digest of Technical Papers, pp. 156–157 (2009a)
- I.J. Chang et al., **A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS.** IEEE J. Solid-State Circuits 44(2), 650–658 (2009b)
- T.H. Kim et al., **A High-Density Sub threshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme.** Proceedings of IEEE International Solid-State Circuits Conference (ISSCC), pp. 330–331, Feb 2007

References

- T. Suzuki et al., 0.5 V, 150 MHz, **Bulk-CMOS SRAM with Suspended Bit-Line Read Scheme**, Proceedings of IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 354–357, Sept 2010
- K. Takeda et al., **A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications.** IEEE J. Solid-State Circuits 41(1), 113–121 (2006)
- K. Utsumi et al., **A 65 nm low power CMOS platform with 0.495 lm2 SRAM for digital processing and mobile applications.** Proceedings of IEEE Symposium VLSI Technology, pp. 216–217 June 2005
- M. Yabuuchi et al., **A 45 nm low-standby-power embedded SRAM with improved immunity against process and temperature variations.** Proceedings of IEEE International Solid-State Circuits Conference, pp. 326–327, Feb 2007