EE6361 – Advanced Topics in VLSI

Assignment – 1 – 28 January 2017
Due: 13th February 2017 (11:59 PM)
Instructions:

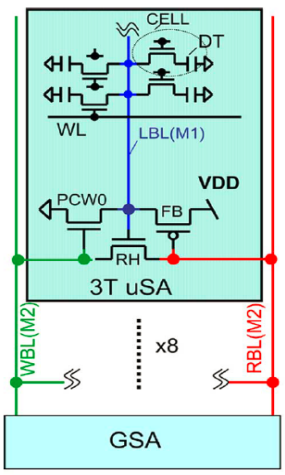
1. Submit only a soft copy as a PDF (NO WORD DOC please)
2. Exact submission procedure will be made clear within a week
3. Keep the answers crisp and precise

Given:

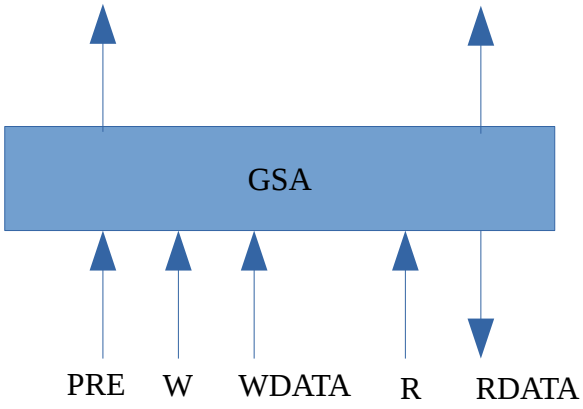
1. All transistors are modelled using the Berkeley PTM 22nm LP and HP models
2. G = Gate , D = Drain , S = Source, B = Body
3. Deep trench capacitor in this technology = 20fF, Series resistance = 5KΩ
4. Use the LP (Low power) NFET as the access device of the eDRAM cell
5. Use the HP (High performance) FETs for other circuitry like sense amp etc
6. For all FETs: L = 25nm and Wmin = 50nm
7. VDD = 0.8V

Questions

1. Characterise the LP and HP NFETs to extract
    1. Threshold voltage – Defined as the VG when ID = (W/L)I_{TH} where I_{TH} = 300nA and VD = VDD
    2. The gate voltage at which GIDL sets in
2. For an eDRAM in this technology specify the operating voltages of the following assuming that the threshold variation is ~15% of the mean value
    1. BL
    2. WL
3. Model a single Bit-line slice with N cells connected to 3T-μSA as shown below
    - Model the load from N-1 cells using a single transistor with m = N-1
    - Assume that LBL metal capacitance is negligible
    - Assume that the WBL and RBL are driven directly / initialized in the simulation
    - Answer the following:
    1. What are the sizes of the cell access device, PCW0, RH and FB? Justify
    2. Simulate the waveforms for a WRITE 1
    3. Indicate the pre-charge, signal development and write back phases on a READ1 waveform
    4. Set N to 32, 64 and 128 and compare the Write and read times



4. **BONUS question**: Assume that the GSA has the following input/ output



PRE	W	WDATA	R	RDATA	WBL	RBL
1	X	X	X		1	1
0	0	0	0	Float low	0	Float High
0	1	0	0	Float low	1	1
0	1	1	0	Float low	0	0
0	0	X	1	DATA	0	Float High

Design the logic circuit in the GSA to implement the above truth table.