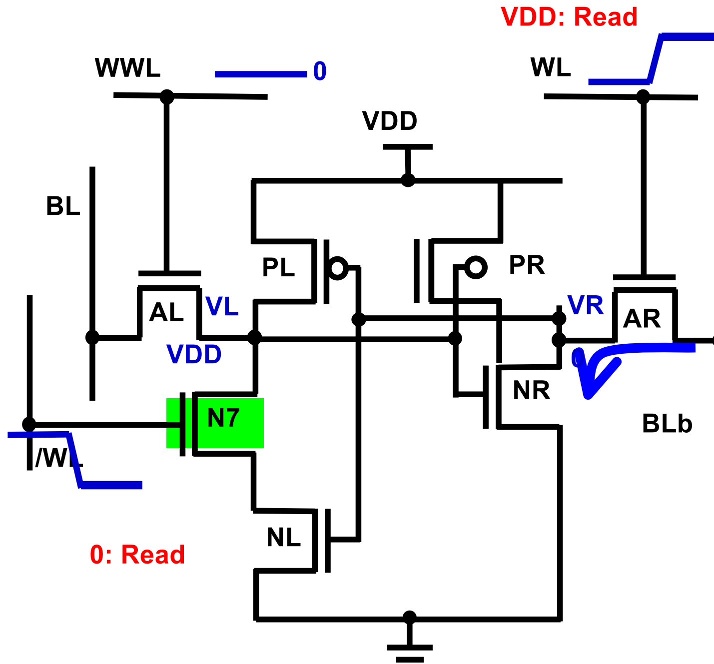
Advanced VLSI Circuits

Due: March 23, 2017

1. For a conditionally decoupled cell shown, for each of the failure mechanisms (listed in the table), fill in the cells with one of **{-ΔV$_T$, +ΔV$_T$ or NA}** to represent the worst-case variation condition for that failure mechanism. [16]



	PL	*PR*	*NL*	*NR*	*AL*	*AR*	*N1*	*N2*
Hold Failure								
Access Failure								
Read Failure								
Write Failure								

2. For a 2read-1write 8-KB instruction cache, implemented using single ended read sram cells. The array is byte-readable and double-byte writeable, and a 4-way column multiplexing is used. Hierarchical bit-line scheme is not used. [14]

No. of address bits: ………………………………

No. of row address bits: ………………………………

No. of column address bits: ………………………………

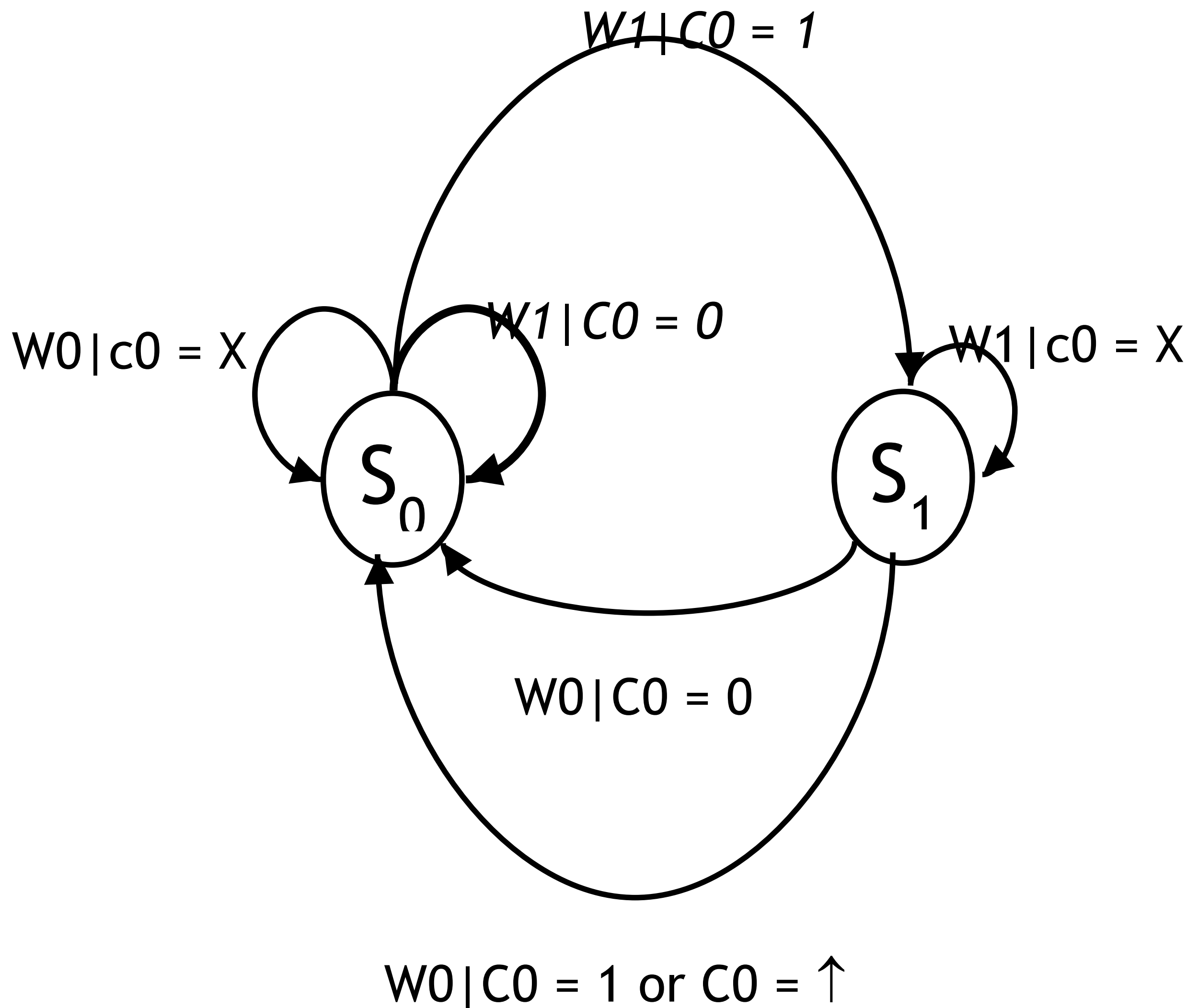
No. of output bits: ………………………………

No. of cells of any bitline: ………………………………

No. of cells on any wordline: ………………………………

Type of cell considered (draw schematic)

3. A memory is known to have the following transition diagram. Can you define a test pattern to test these faults and explain which steps will capture which fault [14]



4. Write an < 5 sentences abstract for the paper *A 64Mb SRAM in 32nm High-k Metal-Gate SOI Technology with 0.7V Operation Enabled by Stability, Write-Ability and Read-Ability Enhancements* by H. Pilo [6]