EE 5311 Digital IC Design Tutorial 4

	$t_{setup}(ps)$	$t_{pcq}(ps)$	$t_{pdq}(ps)$	$t_{ccq}(ps)$	$t_{cdq}(ps)$	$t_{hold}(ps)$
Flop	65	50	N.A	35	35	30
Latch	25	50	40	35	35	30

1. An implementation of a D Flip-flop is show in Fig. 1. Answer the following
   1. Is this a static or dynamic flip-flop?
   2. Is this positive edge triggered or negative edge triggered?
   3. Calculate t_{setup}, t_{CQ} and t_{hold} for this flop in terms of the transmission gate and inverter delays
   4. Analyse this flop for clock overlap issues and compare with the C2MOS implementation. What's the key difference?

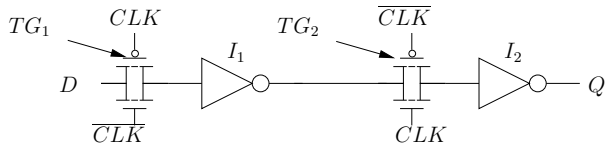

Figure 1: D Flip-flop

2. An implementation of a sequential element is show in Fig. 2. Answer the following
   1. Is this a latch (level triggered) or a flip flop (edge triggered)?
   2. Is it static or dynamic?
   3. Construct a positive edge triggered D flip-flop using this sequential element.
   4. For the DFF constructed above, calculate t_{setup}, t_{CQ} and t_{hold} in terms of the transmission gate and inverter delays. Assume that $\overline{CLK}$ is generated from CLK with an ideal inverter (0 delay).

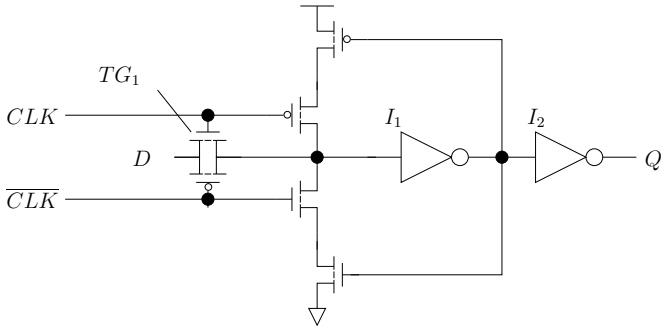

Figure 2: Sequential Element

3. Shown in Fig. 3 is an implementation of a dynamic flip flop. The transistors are sized to achieve equal rise and fall delay while minimizing the area. Assumptions:
   - CLK and $\overline{CLK}$ are ideal and have no overlap
   - All transitions are instantaneous.

   (a) Plot the waveforms of Q_m and Q for the first cycle when the input D is as shown in the Fig. 3. Mark all steady state voltage values.

   (b) Which of the two signals Q_m / Q look unusual? Why? Can you suggest a fix for the problem?

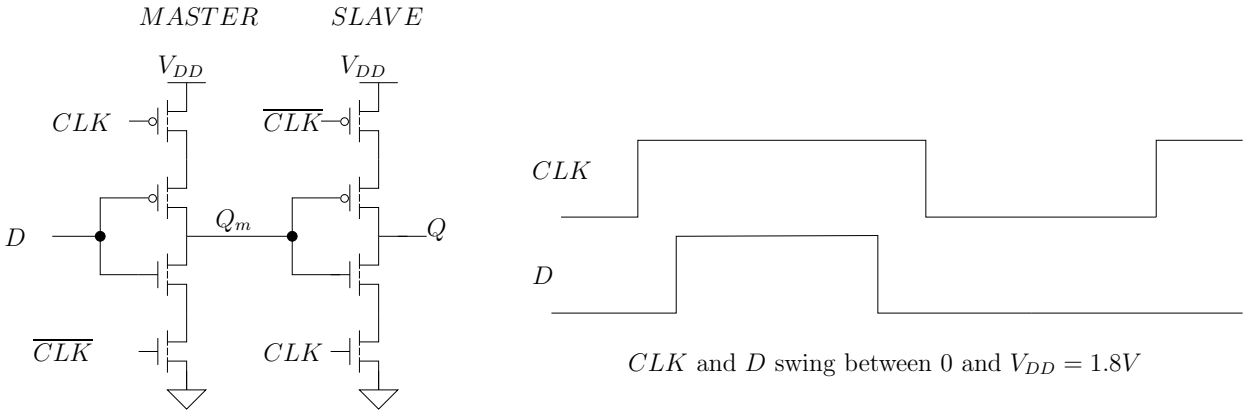

Figure 3: Question 3:Erroneous Dynamic Flip Flop

(c) If the minimum clock period at which the faulty circuit works is T_{min}, what is the corresponding value for the "corrected "circuit?

4. For each of the following sequencing styles, determine the maximum logic propagation delay available within a 500 ps clock cycle. Assume there is no clock skew and no time borrowing
   1. Flip-Flop
   2. Two-phase tansparent latches
5. Repeat the above when clock skew can be up to 50 ps.
6. Assuming there is no clock skew, determine the minimum logic contamination delay in
   1. each clock cycle for a Flip-Flop
   2. each half cycle for a two-phase transparent latches with 50% duty cycle
   3. each half cycle for a two-phase transparent latches with 60 ps of non-overlap between the phases
7. Repeat the above question if the clock skew between any two elements can be up to 50 ps
8. Suppose one cycle of logic is particularly critical and the next cycle is nearly empty, Determine the maximum amount of time the first cycle can borrow into the second for each of the following sequencing styles when there is no clock skew
   1. each clock cycle for a Flip-Flop
   2. each half cycle for a two-phase transparent latches with 50% duty cycle
   3. each half cycle for a two-phase transparent latches with 60 ps of non-overlap between the phases
9. Repeat the above when the maximum clock skew can be 50 ps
10. For the path show in Fig. 4 determine which latches borrow time and if any setup time violations occur. Assume there is no clock skew and that latch delays are accounted for in the propagation delays Δ's. Repeat for cycle times of 1200, 1000 and 800 ps.
    1. $\Delta_1 = 550ps$; $\Delta_2 = 580ps$; $\Delta_3 = 450ps$; $\Delta_4 = 200ps$;
    2. $\Delta_1 = 300ps$; $\Delta_2 = 600ps$; $\Delta_3 = 400ps$; $\Delta_4 = 550ps$;
11. For the path show in Fig. 5, determine the minimum clock period at which the circuit will operate correctly for each of the following logic delays. Assume clock skew is zero and and that latch delays are accounted for in the propagation delay Δ's.

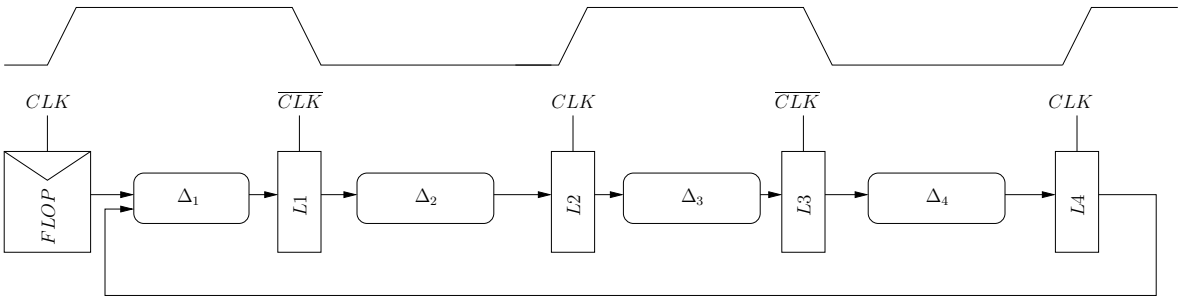

Figure 4: Sequential path-1

1. $\Delta_1 = 300ps$; $\Delta_2 = 400ps$; $\Delta_3 = 200ps$; $\Delta_4 = 350ps$;
2. $\Delta_1 = 300ps$; $\Delta_2 = 400ps$; $\Delta_3 = 400ps$; $\Delta_4 = 550ps$;
3. $\Delta_1 = 300ps$; $\Delta_2 = 900ps$; $\Delta_3 = 200ps$; $\Delta_4 = 350ps$;

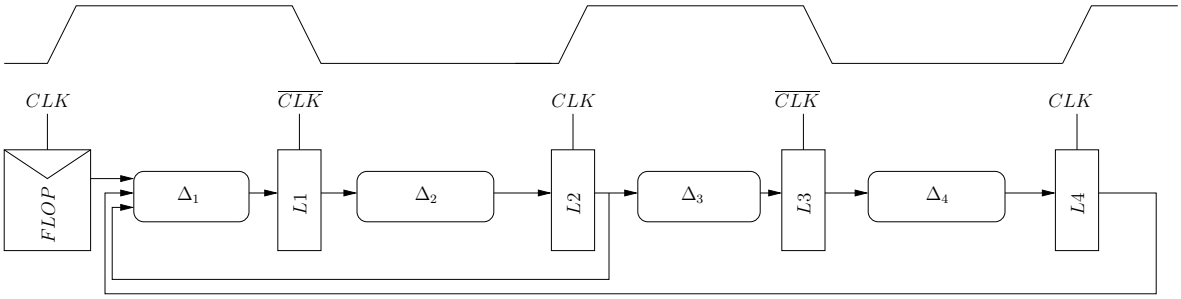

Figure 5: Sequential path-2

12. Repeat the above exercise for the case when clock skew is 100 ps
13. A finite state machine is shown in Fig. 6 where the INVERTER has a delay of $100ps$, the AND gate has a delay of $200ps$ and the XOR has a delay of $300ps$. Answer the following.
    1. What is the critical path of this system?
    2. What is the maximum clock frequency that can be used on this system?
    3. After the clock edge arrives at D flip-flops, what is the earliest time when the output Y is guaranteed to be valid and stable?

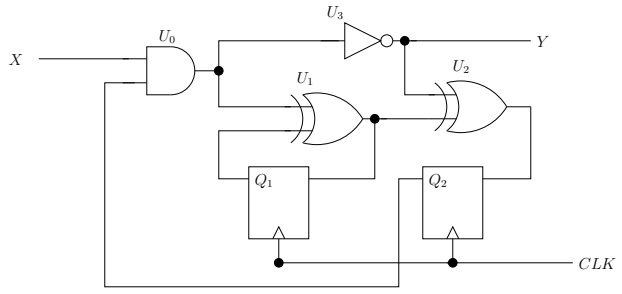

Figure 6: Finite State Machine

14. Determine the minimum clock period at which the following sequential paths will operate correctly. The delay values are $\Delta_1 = 550ps$; $\Delta_2 = 580ps$; $\Delta_3 = 450ps$; $\Delta_4 = 200ps$; Assume clock skew is zero and latch delays are accounted for in the propagation delay Δ's i.e. $T_{cq} = T_{setup} = T_{dq} = 0$
    (a) Path shown in Fig. 7A
    (b) Path shown in Fig. 7B
    (c) If clock skew $T_{skew} = 50ps$, how does the minimum clock frequency change in the above cases?

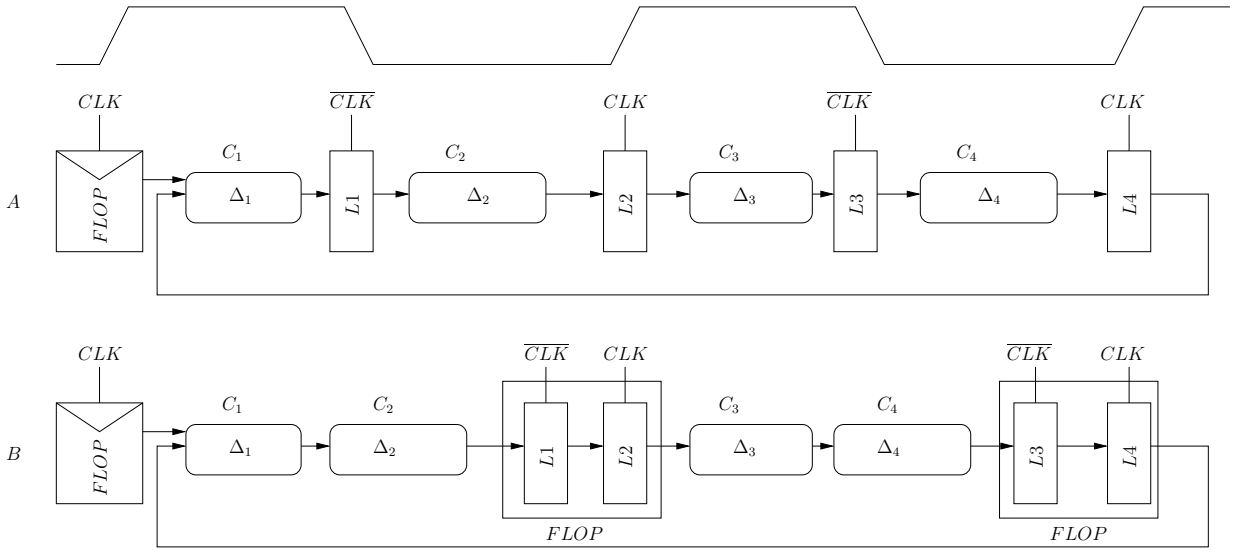

Figure 7: Question 14: Sequential Path