EE 5311 Digital IC Design Tutorial 3

$\mu_n C_{ox} = 160\mu A/V^2$	$\mu_p C_{ox} = 80\mu A/V^2$	$W_{min} = 4\lambda = 0.36\mu$	$L_{min} = 2\lambda = 0.18\mu$	$V_{T_n} = \lvert V_{T_p}\rvert = 0.4V$
$V_{Dsat_n} = 0.35V$	$\lvert V_{Dsat_p}\rvert = 0.6V$	$V_{DD} = 1.8V$		

Note: For the portions requiring a SPICE simulation, you need to submit the simulation plots along with notes on how you measured the delays.

1. Compute the logical effort from each input of an AOI gate ($Y = \overline{AB + CD}$) to the output.
2. Sketch the schematic of a 12-input OR gate using NANDs and NORs of no more than 3 inputs each.
3. Sketch a pseudo-nMOS gate that implements the function $F = \overline{A(B + C + D) + EFG}$
4. Sketch a Hi-Skew NAND3 gate and calculate the logical effort and the parasitic effort
5. Sketch a Lo-Skew NOR4 gate and calculate the logical effort and the parasitic effort
6. Sketch a 3-input CVSL OR/NOR gate.
7. Sketch a dynamic footed and unfooted 3-input NAND and NOR gate. Label the transistor widths and derive the logical effort for each input.
8. Repeat the above exercise for a psuedo nMOS implementation. This time also evaluate the logical effort for the rise as well.
9. Sketch a 4:1 multiplexer given 4 input signals D_0, D_1, D_2, D_3 and two select signals S_0, S_1 using
   1. Only static CMOS logic
   2. combination of Static CMOS logic and Transmission gates

   How many transistors does each implementation require?
10. Design an domino circuit to compute $F = (A + B)(C + D)$ as fast as possible. Each input may present a maximum of 30λ of transistor width. The output must drive a load equivalent to 500λ of transistor width. Choose the transistor sizes to achieve least delay and estimate normalized delay.
11. Design the static CMOS implemenation for the above case with exactly the same capacitance constraints.
12. A pseudo nMOS inverter is designed such that the pMOS transistor width is half that of the nMOS transistors. What is V_{OL}? What are the rise and falling logical efforts?
13. The function $Y_N = \oplus_{i=1}^{N} A_n$ represents an N input XOR gate that operates on inputs $A_1 \ldots A_N$. Y_N needs to be implemented in static CMOS logic with minimum area so that the worst case pull up/ down strengths are identical to that of a reference static CMOS inverter. Assume that both true and complement versions of the inputs are available. Answer the following.
    (a) Derive the condition on N for which the inverting or mirror property holds for Y_N i.e the PMOS stack is the mirror image of its NMOS stack.
    (b) Sketch the static CMOS implementation of Y_3 and calculate the logical effort for each input.
14. Design a 64 leaf node Clock Distribution Network(CDN) using symmetric static CMOS inverters on the lines of a 4 leaf node version shown in Fig. 1. The specifications are as follows:
    - The source CLK drives a unit (reference) inverter which is the maximum load it can drive.
    - The delay at all the leaf nodes (1-64) should be equal and minimum with reference to the source.

- The load capacitance at each leaf node is equivalent to a width of 6144λ

(a) What are the sizes of the NMOS and PMOS devices in each inverter?

(b) Calculate the power dissipated by the CDN at a $V_{DD} = 1.8V$ when the CLK switches at 100MHz if the energy of a reference inverter was characterized to be $4fJ$ at $V_{DD} = 1.5V$ for a single charge-discharge cycle with no load capacitance.

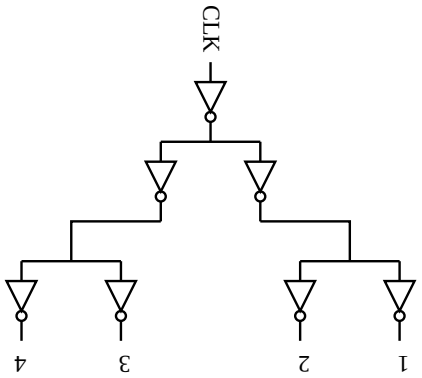

Figure 1: Question 14: Four leaf node clock tree

15. You are asked to build a buffer to drive a load of C_L subject to the constraint that the first stage of the buffer can present a maximum capacitance of 12λ (that is, a minimum sized inverter: NMOS width = 4λ, PMOS width = 8λ) to the previous stage driving it.

    (a) For $C_L = 50\lambda$, how many stages will you choose, and what should be the sizes of the transistors at each stage to minimize total delay through the buffer? Assume transistor sizes need not be multiples of λ.

    (b) If you enforce the condition that transistor sizes must be integer multiples of λ, how much does the delay change - does it increase or decrease?

    (c) Repeat both parts above for $C_L = 500\lambda$

    (d) Repeat both parts above for $C_L = 5000\lambda$

16. An OR gate can be implemented using either of the two following equations: $Y = \overline{\overline{A + B}}$ or $Y = \overline{\overline{A}.\overline{B}}$. In the first case, you use a NOR gate followed by inverter, in the second case, you have 3 stages: inverter, NAND, then again inverter. Assume you must implement in such a way that the input capacitance at the first stage must be at most 50λ.

    (a) Which implementation will you choose if you need to drive a final load of 200λ? How will you choose sizes of the gates?

    (b) Which will you choose if you need to drive 5000λ?

17. What function is implemented by the circuit in fig. 2. What considerations are necessary when sizing the transistors?

18. Sketch the Cascode Voltage Switch Logic implementation of a 2:4 decoder. You may assume that you have both true and complement version of the inputs available. Using this decoder sketch a 4:1 Mux with minimum transistor addition.

19. In the circuit shown below (Fig. 3) all gates are symmetric Static CMOS gates. If the input inverter can present a maximum of 24λ width equivalent of capacitance and the load presents 256λ, answer the following

    (a) What is the minimum path delay?

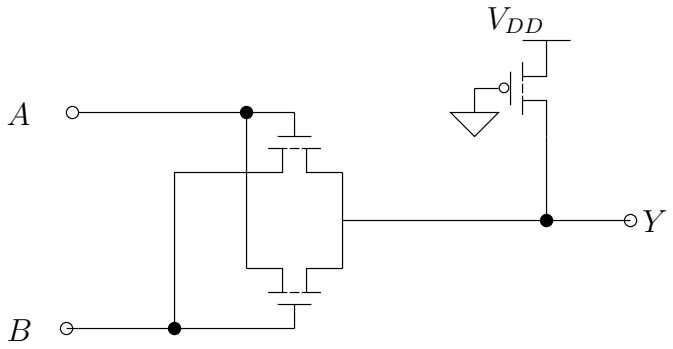

Figure 2: Mystery Circuit.

(b) For what gate capacitances of the NAND3, NOR2 and final inverter is the minimum delay achieved?

(c) What are the absolute sizes of the NMOS and PMOS transistors for each of the gates?

(d) The energy of a unit inverter($Wp/Wn = 8\lambda/4\lambda$) was characterized at $V_{DD} = 1V$ and was found to be $2fJ$ for a single charge-discharge cycle with no load capacitance. Calculate the dynamic power of the circuit in Fig 3 when connected in a configuration shown in Fig 4. You may assume a clock of frequency $f = 1MHz$ with 70% duty cycle is connected to the input A and $V_{DD} = 1.5V$

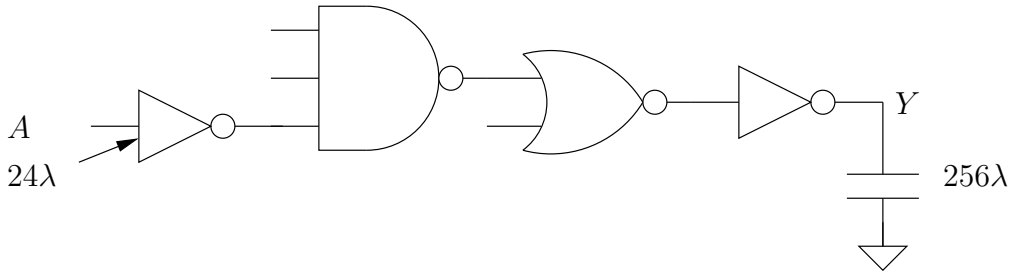

Figure 3: Question 19

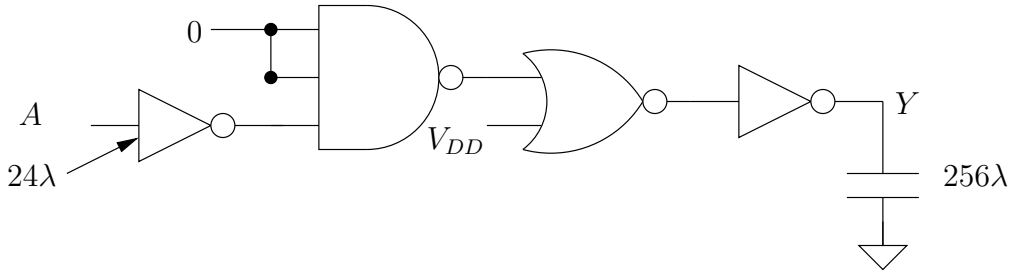

Figure 4: Dynamic Power Configuration

20. A pseudo-NMOS inverter is designed to have a $V_{OL} = 48mV$ when $V_{DD} = 1.8V$. Answer the following
    (a) What is the ratio of W_p/W_n?
    (b) What is the pull up logical effort?
    (c) What is the pull down logical effort?
21. A standard cell library consists of only NAND2 gates, implemented in static CMOS logic, sized for symmetric rise and fall delays. Answer the following.

(a) Construct a symmetric inverter by tying the inputs of the NAND gate appropriately. What is the logical effort (g) and parasitic effort (p) of the symmetric inverter?

(b) A logic path built using n standard cells with path effort F needs to drive a very large load capacitance. The path needs buffering with $(N-n)$ symmetric inverters. If you were given a standard CMOS inverter with logical effort 1 and parasitic delay p_{inv}, set up the equation to derive the optimum stage effort $\hat{\rho}$ by inserting buffers. $\hat{\rho}$ will actually be a function of p_{inv} and we denote it by $\hat{\rho}(p_{inv})$. Note: Obtaining a closed form expression won't be possible. Set up the equation which, when solved numerically, gives the answer.

(c) If you now had to use the symmetric inverter, that you just designed with the NAND2 gate(instead of the standard inverter), set up the equations to obtain the optimum stage effort (ρ) in this buffering scheme. This time the answer will be a function of both g and p, which we will denote by $\rho(g,p)$. Show that $\rho(g,p) = g\hat{\rho}(p/g)$.

Ignore any logical inversion that occurs because of odd number of inverters in both cases.

22. **SPICE Sim**:

(a) Use a SPICE simulation to compute the delay of a minimum size inverter driving another minimum size inverter.

(b) Similarly, find delay of a single two-input NAND gate – assume one input is at 1 and the other is toggling.

(c) For the NAND gate, repeat with the other input stuck to 1 – this should show the difference in delay between the two inputs.

(d) Repeat for both inputs toggling together.

23. **SPICE Sim**: Logical effort

(a) In the SPICE simulation for delay of an inverter, set it up so that each inverter is K times larger than the previous inverter. Plot the delay through the inverter as a function of K.

(b) Use a single stage inverter driving a fixed capacitance of size C and plot the delay as a function of C.

(c) Repeat using a NAND2 gate.

(d) From the slopes and intercepts of the delay vs capacitance plots above, find the logical effort and parasitic effort of the gates.