$\mu_n C_{ox} = 160\mu A/V^2$ $\mu_p C_{ox} = 80\mu A/V^2$ $W_{min} = 4\lambda = 0.36\mu$ $L_{min} = 2\lambda = 0.18\mu$ $V_{T_n} = |V_{T_p}| = 0.4V$
$V_{Dsat_n} = 0.35V$ $|V_{Dsat_p}| = 0.6V$ $V_{DD} = 1.8V$
Reference Inverter: $W_n = 4\lambda$ and $W_p = 8\lambda$

1. Compute the mid-point voltage (V_M) for each of the following CMOS inverters.

    1. $W_p = 6\lambda, W_n = 4\lambda$

    2. PMOS of size 10, NMOS of size 7

    3. Reference inverter

    4. PMOS size 4, NMOS size 8

   For each of the configurations, show which region of operation the two transistors are in, and jus-
   tify your assumptions after computing the value of V_{DS}. Verify your results using SPICE simulations
   (SPICE sims need not be submitted).

2. For each of the transistor configurations shown:
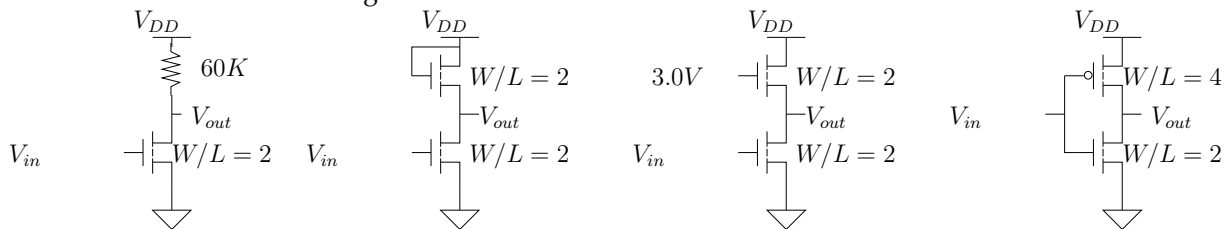
    • What will be the output voltage when input is $V_i = 0$?

    • What will be the output voltage when input is $V_i = V_{DD}$?

    • Which of the circuits has current dissipation when idle? Under what conditions does this happen?
      What is the static power dissipation of the circuits for each input configuration?

    • Calculate V_{OH} and V_{OL} for each circuit.

3. A reference CMOS inverter is connected to the following outputs. In each case, estimate the propagation
   delay of the inverter. Assume that for the 180nm technology, $RC = 5ps$. (Assume the capacitance for
   MOS transistors is $2fF/\mu$ of transistor width for 180nm tech).

    • Another reference CMOS inverter

    • Another CMOS inverter of size: PMOS 10, NMOS 8

    • A fixed external capacitance of 5fF

   Note: For the portions requiring a SPICE simulation, you need to submit the simulation plots along
   with notes on how you measured the delays.

4. For the RC tree structure shown, derive and estimate the propagation delay from node 1 to node 5 using
   Elmore's delay formula. All resistances are $10K\Omega$ and call capacitors are $1.0fF$. Use a SPICE simulation
   to check the result, and comment on the accuracy of the estimate. Do the SPICE simulation for both
   cases: (a) node 5 initially at 0 with V_i going from 0 to V_{dd} and (b) node 5 initially at V_{dd} and V_i going
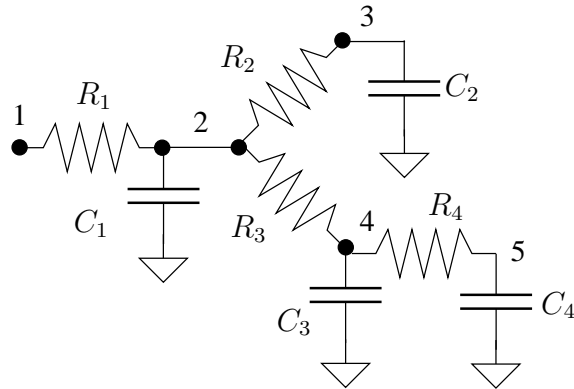   from V_{dd} to 0.

Figure 1: Elmore delay tree. $R = 10K\Omega$, $C = 1.0fF$

5. For the pass transistor configurations shown below, determine the final voltage on the capacitor
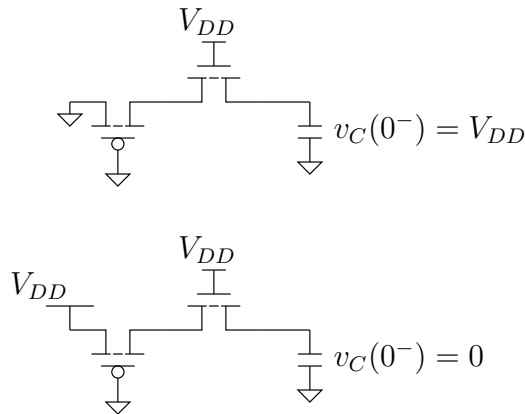

Figure 2: Pass transistors

6. Derive an expression for the trip point ($V_{in} = V_{out} = V_M$) of a long channel inverter.

7. Derive an expression for the gain of an inverter at the trip point ($V_{in} = V_{out} = V_M$).

8. Please read this paper on stacking effect to understand the detailed derivation for short channel devices.

   S. Narendra, S. Borkar, V. De, D. Antoniadis and A. Chandrakasan, "Scaling of stack effect and its application for leakage reduction," ISLPED'01: Proceedings of the 2001 International Symposium on Low Power Electronics and Design (IEEE Cat. No.01TH8581), Huntington Beach, CA, USA, 2001, pp. 195-200. doi: 10.1109/LPE.2001.945400

   Note: The symbols and notation is quite messed up and is not as per the usual convention. For example λ_d is used for the DIBL coefficient. Not CLM parameter.