$$
\begin{array}{llll}
\mu_{n} C_{o x}=160 \mu A / V^{2} & \mu_{p} C_{o x}=80 \mu A / V^{2} & W_{\min }=4 \lambda=0.36 \mu & L_{\min }=2 \lambda=0.18 \mu \\
V_{\text {sa }_{n}}=0.35 \mathrm{~V} & \left|V_{\text {Dsat }}\right|=0.6 \mathrm{~V} & V_{D D}=1.8 \mathrm{~V} & V_{T_{n}}=\left|V_{T_{p}}\right|=0.4 V
\end{array}
$$

Note: $L_{\text {min }}=2 \lambda$ and $W_{\text {min }}=4 \lambda$ is a convention used to represent transistor dimensions in terms of the technology length $\lambda$. For example, in 180 nm process $L_{m i n}=180 \mathrm{~nm}=2 \lambda$. This is different from the channel length modulation parameter.

1. An inverting path in a circuit is defined as a path from a signal $A$ to another signal $B$ such that whenever there is a rising transition on $A$, the signal at $B$ either remains the same as what it was earlier, or has a falling transition. A simple example is a NOT gate: when input rises, output must fall.
(a) Which of the following gates: AND, NAND, OR, NOR, NOT are inverting, and which are noninverting?
(b) Can an XOR gate be classified as inverting or non-inverting?
2. Consider an NMOS transistor with $V_{S}=0.8 \mathrm{~V}, V_{G}=1.8 \mathrm{~V}, V_{D}=1.0 \mathrm{~V}, \gamma=0.4 \sqrt{V}$. What will be the threshold voltage of the transistor under these operating conditions assuming $\psi_{S}=0.6 \mathrm{~V}$
3. Estimate the gate capacitance of a minimum-sized PMOS transistor $(W=4 \lambda)$. Gate oxide thickness is $40 \AA$.
4. Estimate the drain diffusion capacitance of an NMOS transistor under two conditions: (a) drain is at 0 V , (b) drain is at $V_{D D}$. The area of the drain diffusion is $4 \lambda \times 5 \lambda$. Assume the substrate is grounded. The transistor has $C_{J}=0.98 \mathrm{fF} / \mu \mathrm{m}^{2}, m_{J}=0.36, C_{J s w}=0.22 \mathrm{fF} / \mu \mathrm{m}, m_{J s w}=0.10$, and $\psi_{0}=0.75 \mathrm{~V}$ at room temperature.
Note: This problem is worked out in the book by Rabaey et al. The idea is for you to go through the same exercise and understand the issues involved. To solve the above problem, you need to (a) refresh your understanding of depletion region capacitance in the reverse biased junctions and (b) understand the difference between the bottom level of the diffusion and the sidewall junctions. The main point of the problem, however, is to get a feel for the sizes of capacitances and the numbers involved. The rest of it is just using a formula.
5. Consider a PMOS transistor of size $8 / 2$. For each of the following cases, indicate the region of operation of the transistor, and calculate the drain current $I_{D}$.
6. $V_{G S}=0, V_{D S}=-V_{D D}$
7. $V_{G S}=-V_{D D}, V_{D S}=0$
8. $V_{G S}=-1.0 \mathrm{~V}, V_{D S}=-0.2 \mathrm{~V}$
9. $V_{G S}=-0.6 \mathrm{~V}, V_{D S}=-1.0 \mathrm{~V}$
10. $V_{G S}=-V_{D D}, V_{D S}=-V_{D D}$
11. Consider a NMOS transistor of size $4 / 2$. For each of the following cases, indicate the region of operation of the transistor, and calculate the drain current $I_{D}$.
12. $V_{G S}=0, V_{D S}=V_{D D}$
13. $V_{G S}=V_{D D}, V_{D S}=0$
14. $V_{G S}=1.0 \mathrm{~V}, V_{D S}=0.2 \mathrm{~V}$
15. $V_{G S}=0.6 \mathrm{~V}, V_{D S}=1.0 \mathrm{~V}$
16. $V_{G S}=V_{D D}, V_{D S}=V_{D D}$

Repeat the above questions when the transistor size is $40 / 20$. What is the main difference you can expect?
7. (a) What will be the maximum current that can be delivered by an NMOS transistor of size 4/2? For what conditions of drain, gate, source voltages will you get this current?
(b) How much will the current be for a transistor of size 40/20?
(c) SPICE Sim: Simulate the $I_{D}$ vs $V_{G S}$ for $V_{D S}=V_{D D}$ for transistors of different $\mathrm{W} / \mathrm{L}$ keeping $\mathrm{W} / \mathrm{L}$ ratio constant but increasing the sizes. Note how the velocity saturation effect decreases as overall length increases.
8. (a) Calculate the threshold voltage of a NMOS device when the body is biased at $V_{B S}=-0.11 \mathrm{~V}$. Assume that $\psi_{S}=0.25 \mathrm{~V}$
9. (a) Calculate the equivalent resistance of an NMOS transistor that is discharging a capacitor from $V_{D D} \rightarrow V_{D D} / 2$ with its gate connected to $V_{D D}$. The transistor has a $W / L=8 \lambda / 2 \lambda$
For the circuit in Fig. 1, assume that the transistor is a long channel device and is in saturation for the time, $t_{\text {delay }}$, when discharging the capacitor down to $V_{D D} / 2$. The transient response can be analysed in two different ways:- One is to treat the NMOS as a resistor with equivalent resistance $R_{e q}$ and other is to consider it as an ideal current source.


Figure 1: Question 9
(a) Derive an expression for $R_{e q}$
(b) Show that both these methods give approximately the same value of $t_{\text {delay }}$
(c) Plot the transient response, extrapolating both models all the way down to zero. Show the salient features of the curve.

