Note:

- The unit inverter is as defined in the spreadsheet where you entered your group details.
- All widths are to be scaled with respect to the unit inverter that has been assigned to your group
- The length is also greater than 2λ for many groups. This is a legitimate way of controlling leakage.
- Technology $\lambda = 300nm$.
- Model File: C5_models.txt (uploaded on Moodle)

1 Problem Statement

Design an 8 bit array multipler with a single stage pipeline. The idea is to show that the frequency of operation can be doubled and data can be fed to the multiplier at twice the rate through pipelining. This would require the following components

- NAND2/ AND2 gate
- Full adder
  - Carry out generation circuit
  - Sum generation circuit
- Flip flop for pipelining

You will build your library with the above components and submit each one as an assignment. The exact deliverables for each assignment is given below

2 Assignment 1: Two Input AND Gate - Due 20 Sep 2017

Design a 2-input unit AND gate by cascading a NAND2 with an INVERTER.

2.1 Deliverables

- Scheamtic of NAND2, INVERTER and AND2 gate
- DRC and LVS clean NAND2, INVERTER and AND2 gate
- Characterized rise and fall delay of the NAND2 gate as a function of Fan out 0-8 (NAND2 driving identical copies of itself). Use the RC extracted netlist of the NAND gate - The procedure to do this will be communicated shortly.

2.2 Submission

A single PDF showing

- The schematic and layout of each gate
- DRC and LVS results
- Rise and Fall delay of the NAND2 gate tabulated vs fan out

3 Assignment 2: Carry Out Circuit of a Full Adder - Due 27 Sep 2017

Design the Carry Out part of the Full Adder.

3.1 Deliverables

- Transistor schematic of the Carry out circuit
- DRC and LVS clean layout of the Carry out circuit
- Sizes of the transistors

3.2 Submission

A single PDF showing

- The schematic and layout of CARRY OUT circuit
- DRC and LVS results
- Simulation in IRSIM AND SPICE to show correct functionality

4 Assignment 3: Sum Generation Circuit of a Full Adder - Due 9 Oct 2017

Design the SUM part and complete the Full Adder.

4.1 Deliverables

- Transistor schematic of a complete Full Adder circuit
- DRC and LVS clean layout of the Full Adder circuit
- Sizes of the transistors in the SUM part

Guidelines

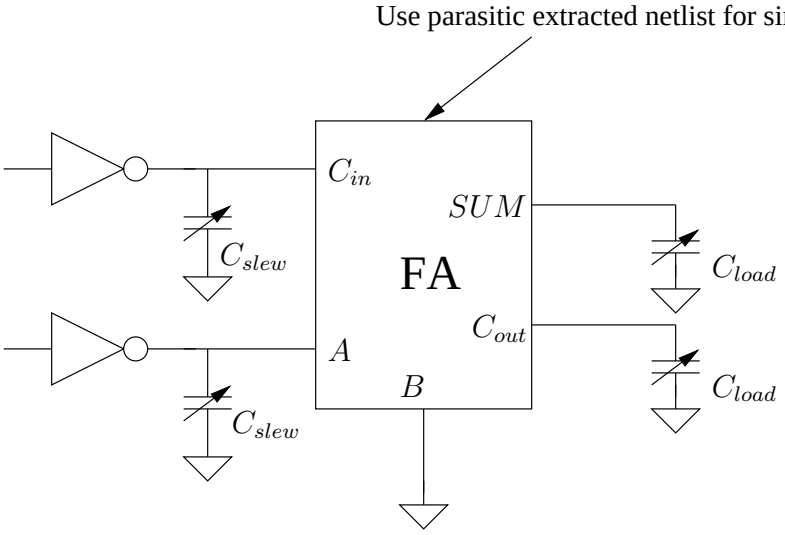
- The V_{DD} and GND lines should run in Metal-2
- The $V_{DD} - GND$ pitch should be the same for all cells (NAND, AND, Full adder)
- Break wide transistor into smaller parallel ones - This will help reduce the Y dimension
- Aspect ration of the cell should be reasonably close to a square.

4.2 Submission

A single PDF showing

- The schematic and layout of FA circuit. Mark the dimensions of the layout
- DRC and LVS results
- Simulation in SPICE to show correct functionality of a Full Adder
- Characterize the delay (time takes from 50% input to 50% output) and output slew (time taken to go from$10\% - 90\%$ of the output) as shown in the figure below
    1. Vary C_{slew} from $10fF - 200fF$ in steps of $10fF$ to vary the input slew
    2. Vary C_{Load} from $10fF - 500fF$ in steps of $50fF$ to vary the load cpacitance
    3. For each step of C_{slew} measure input slew S_{in} of the input

4. Create a table of the output delay of SUM as a function of S_{in} of A and C_{Load} (C_{in} should be tied to the appropriate supply)
5. Create a table of the output slew of C_{out} as a function of S_{in} of C_{in} and C_{Load} (A should be tied to the appropriate supply)



5 Assignment 4: Flip Flop Desgin - Due 13 Oct 2017

Design a D Flip Flop.

5.1 Deliverables

- Transistor schematic of a D Flip Flop Master and Slave Stage
- DRC and LVS clean layout of the Flip Flop
- Sizes of the transistors.
- Characterized delays of the flip flop.

5.2 Submission

A single PDF showing

- The schematic and layout of the Flip Flop circuit. Mark the dimensions of the layout
- DRC and LVS results
- Simulation in SPICE to show functionality of the Flip Flop
- Characterized delay numbers in a table

6 Final Submission: 8 Bit Multiplier Design with and without Pipelining - Due 6 Nov 2017

With that, you now have all the components to do the layout of a pipelined multiplier. This final submission does NOT require a layout

6.1 Deliverables

- Transistor schematic of an 8 bit multiplier, with and without pipelining, with the components you built

6.2 Submission

The complete ELECTRIC library(.jelib) with

- Scheamtic of the 8 bit multiplier without a pipeline
- Schematic of the 8 bit multiplier with a single stage pipeline
- Scheamtic and layout of all sub blocks from previous assignments - DRC and LVS clean

A single PDF showing

- Design of the 8 bit multipler
- Area estimate of the multipler without pipeline
- Maximum operating frequency of the Multiplier (without Pipeline)
- Location of the flip flop to double the frquency of operation
- SPICE simulation showing the frequency of operation with and without pipelining