EE5311- Digital IC Design

Module 5 - Sequential Circuit Design

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November 9, 2018

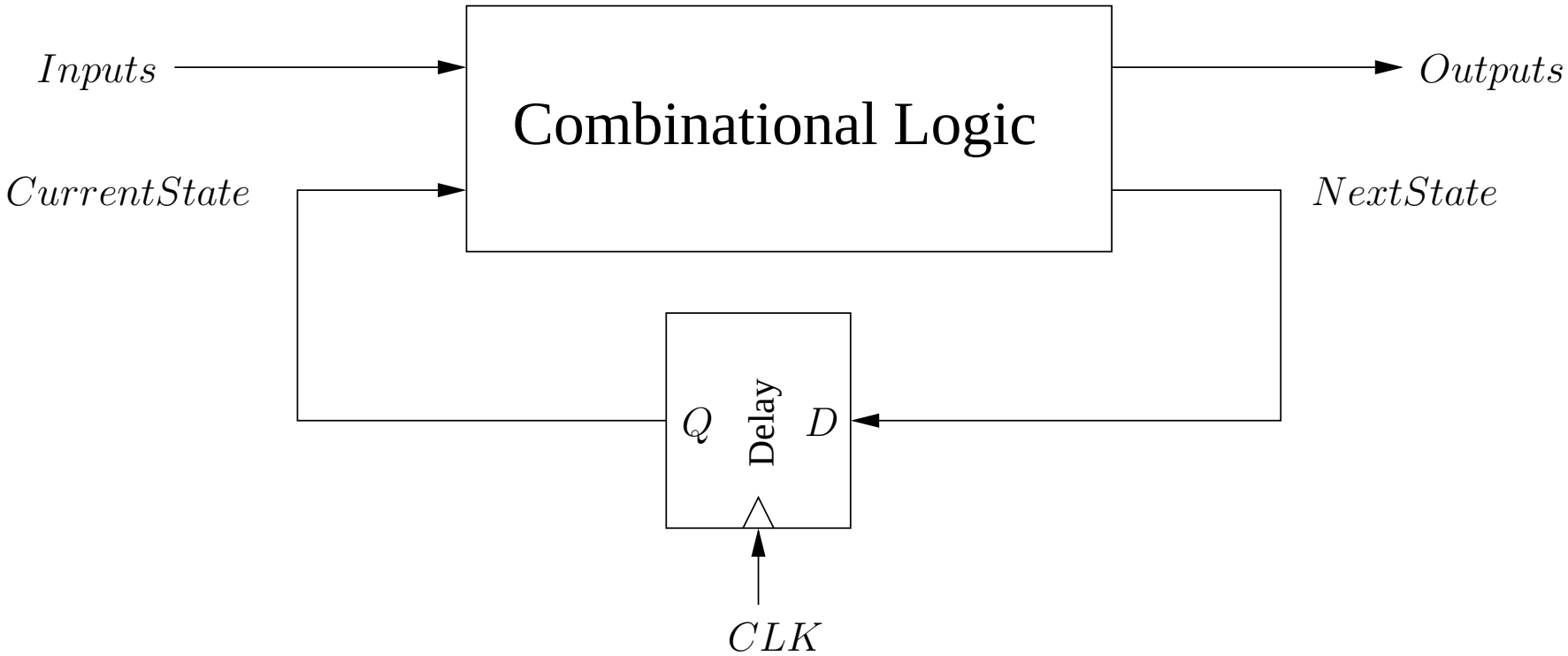
Learning Objectives

- Build elementary sequential circuits like latches and flip flops - Static and Dynamic
- Identify devices that affect set up and hold time
- Derive max and min delay constraints for latch/ flip flop based pipeline systems
- Account for clock skew in a pipelined system
- Analyse time borrowing across half cycles and across cycles
- Calculate the maximum clock frequency of operation of a pipelined system

Outline

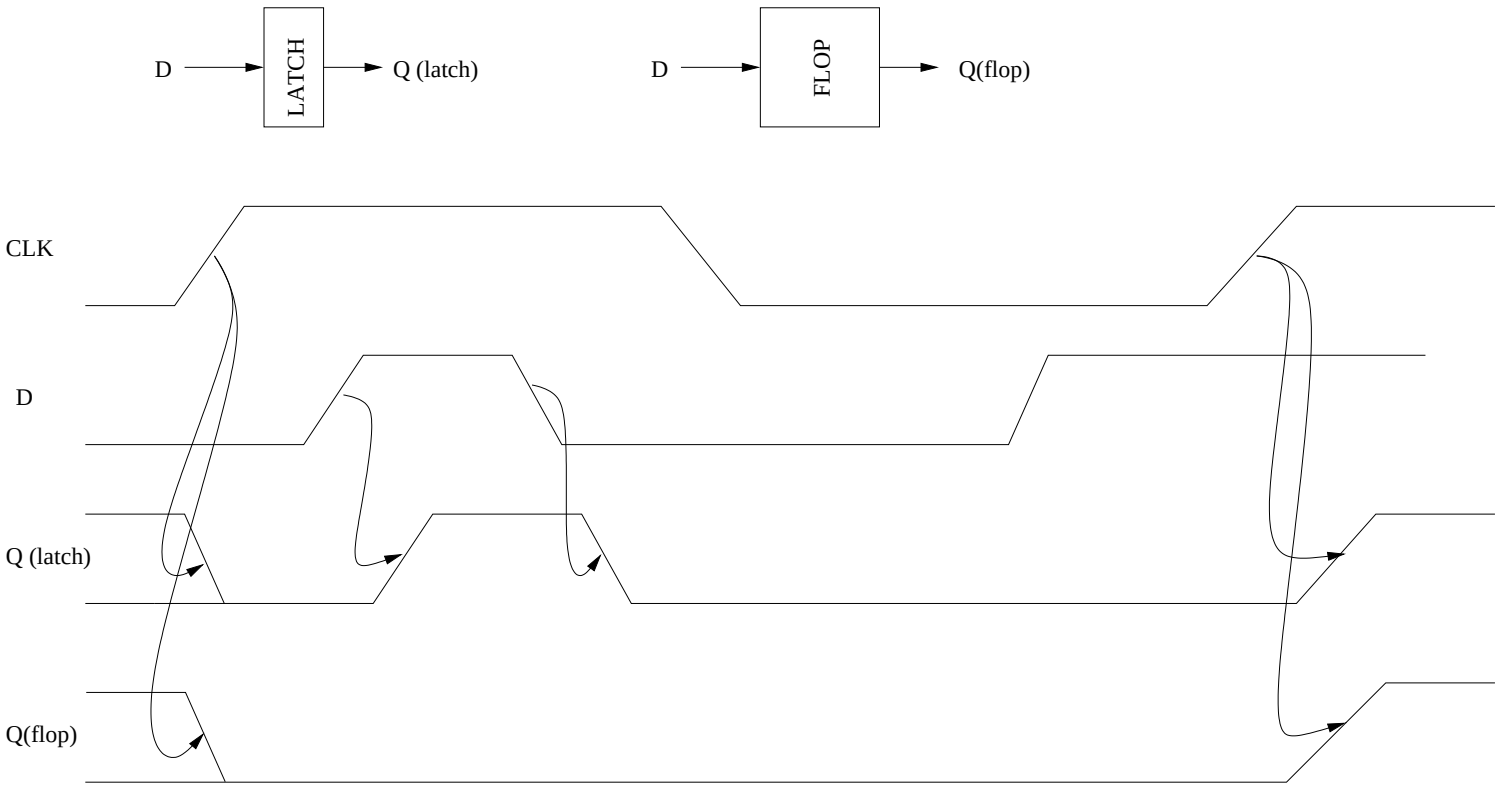
- Finite State Machines
- Sequencing Elements
- Sequencing Methods
  - Flip flop
  - Latch
- Delay definitions
- Circuit Implementations of Latch/ Flop
  - Static
  - Dynamic
- Max delay constraints
- Min delay constraints
- Time Borrowing

Finite State Machines



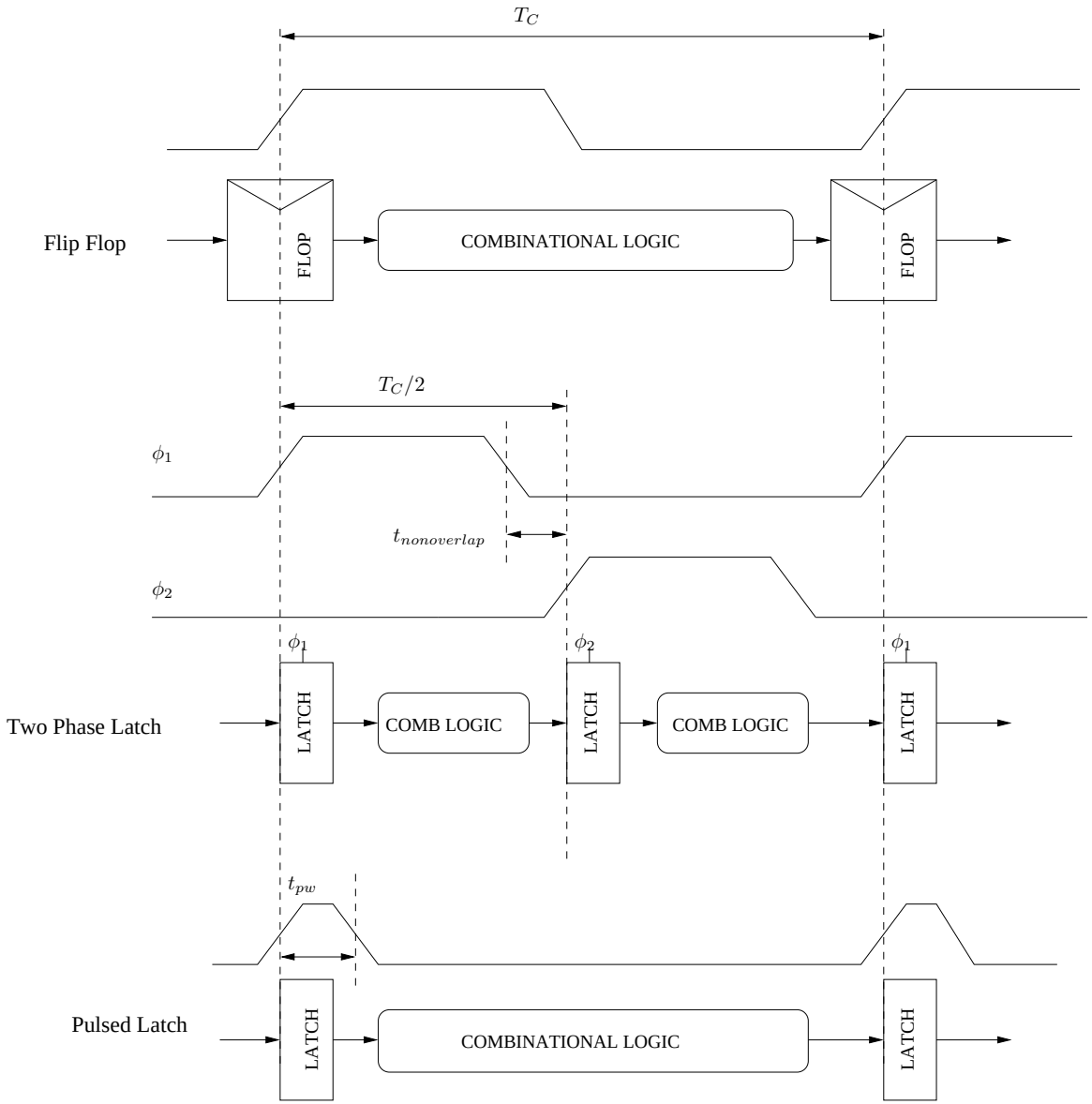
Ability to feed data back to combinational circuits requires delays

Sequencing Elements



- Latch - Transparent when CLK=1, samples on the falling edge
- Flop - Samples on the rising edge

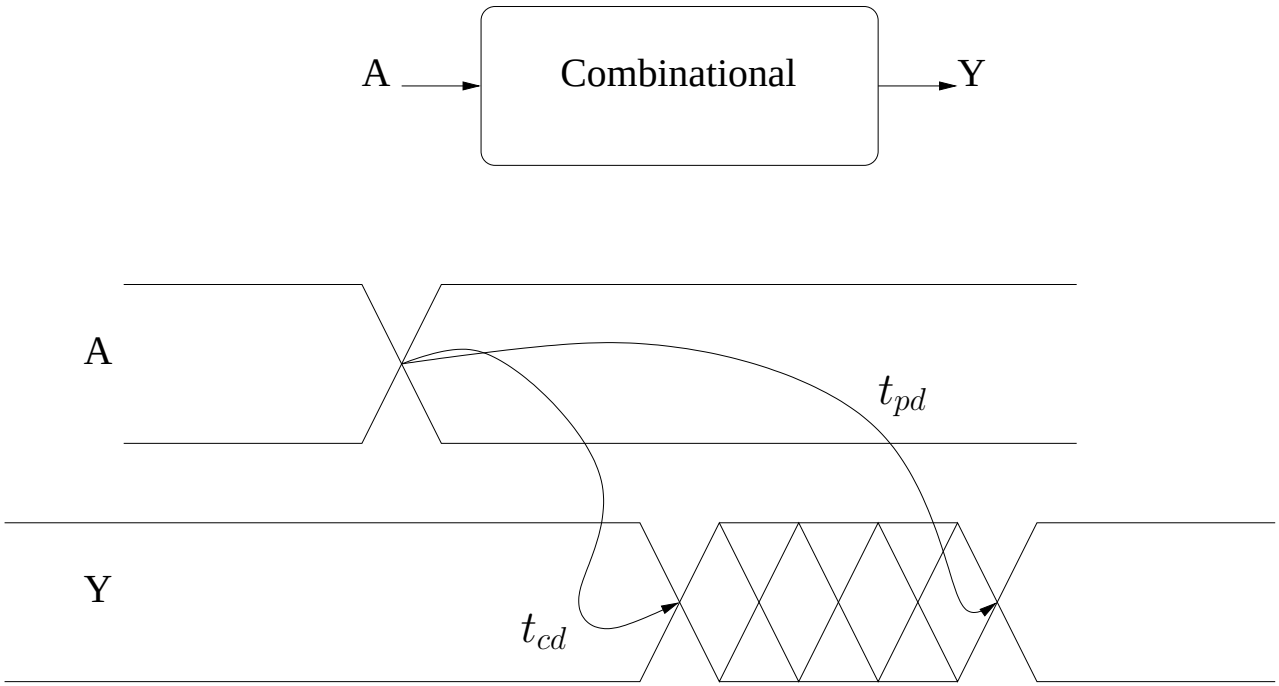
Sequencing Methods



Timing Notation

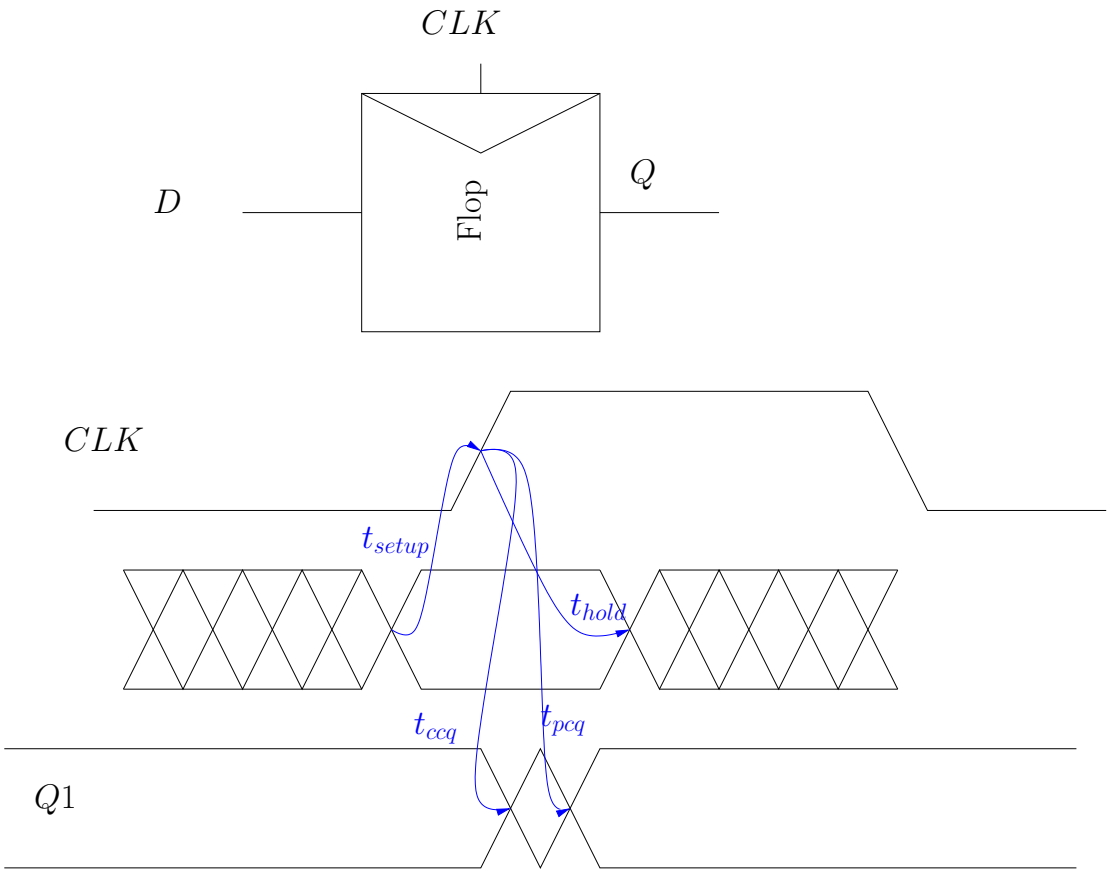
Term	Name
t_{pd}	Logic Propagation Delay
t_{cd}	Logic Contamination Delay
t_{pcq}	Latch/ Flop Clock-Q Propagation Delay
t_{ccq}	Latch/ Flop Clock-Q Contamination Delay
t_{pdq}	Latch D-Q Propagation Delay
t_{cdq}	Latch D-Q Contamination Delay
t_{setup}	Latch/ Flop Setup Time
t_{hold}	Latch/Flop Hold Time

Combinational Logic Delay



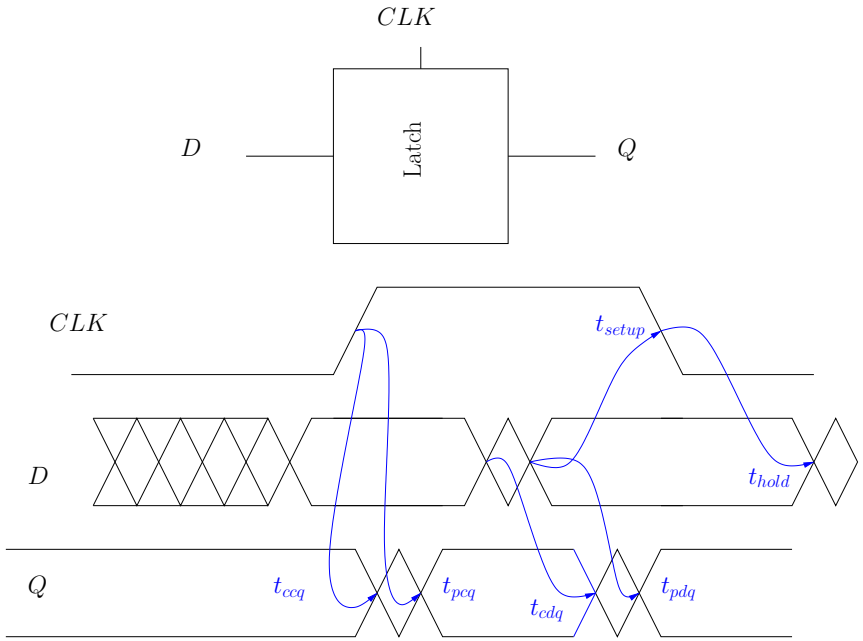
- t_{cd} - Contamination delay - Min delay through the circuit
- t_{pd} - Propagation delay - Max delay through the circuit

Flip Flop Delay



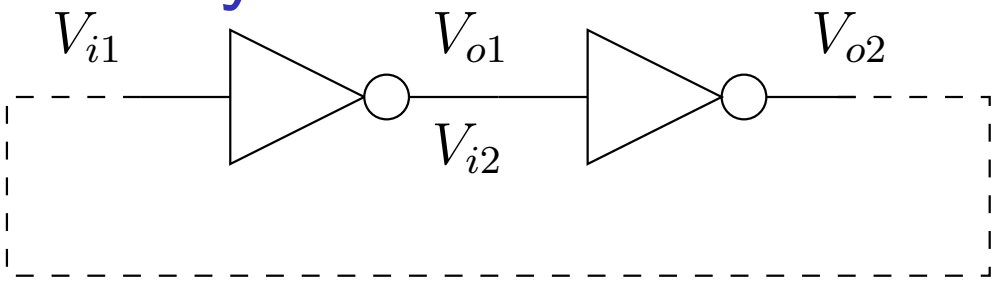
- t_{ccq} - Contamination Clock-Q delay
- t_{pcq} - Propagation Clock-Q delay
- t_{setup} - Set up time
- t_{hold} - Hold time

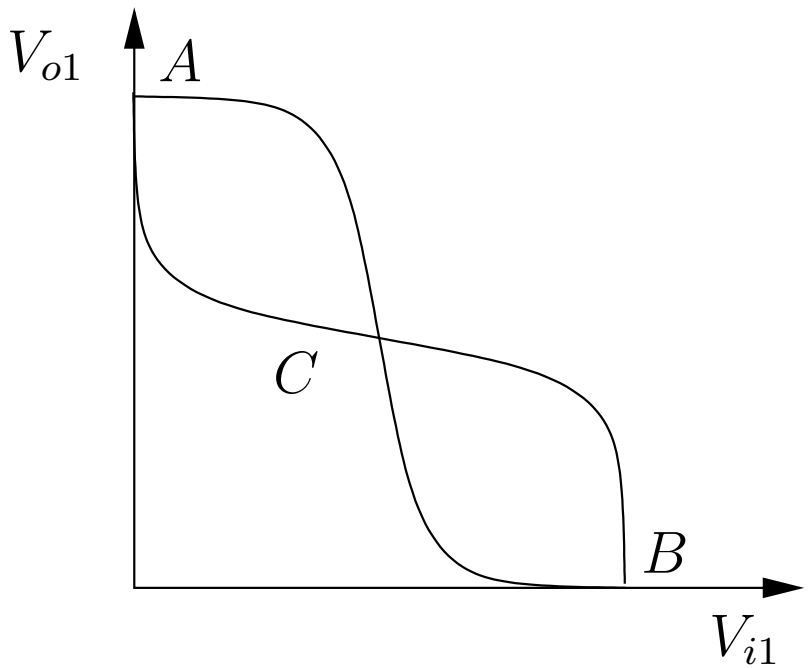
Latch Delay



- t_{ccq} - Contamination Clock-Q delay
- t_{pcq} - Propagation Clock-Q delay
- t_{cdq} - Contamination D-Q delay
- t_{pdq} - Propagation D-Q delay
- t_{setup} - Set up time
- t_{hold} - Hold time

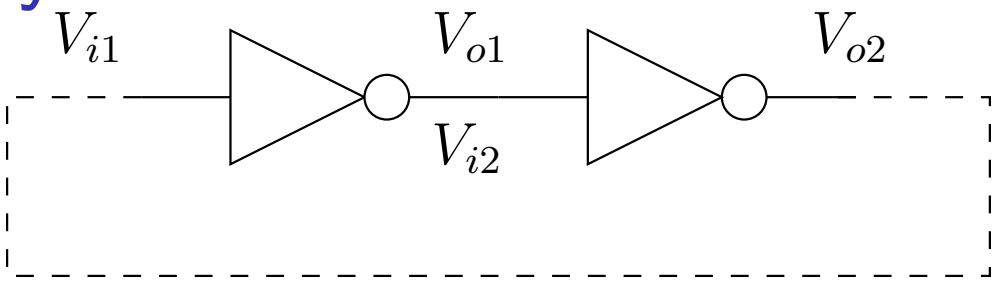
Bistability

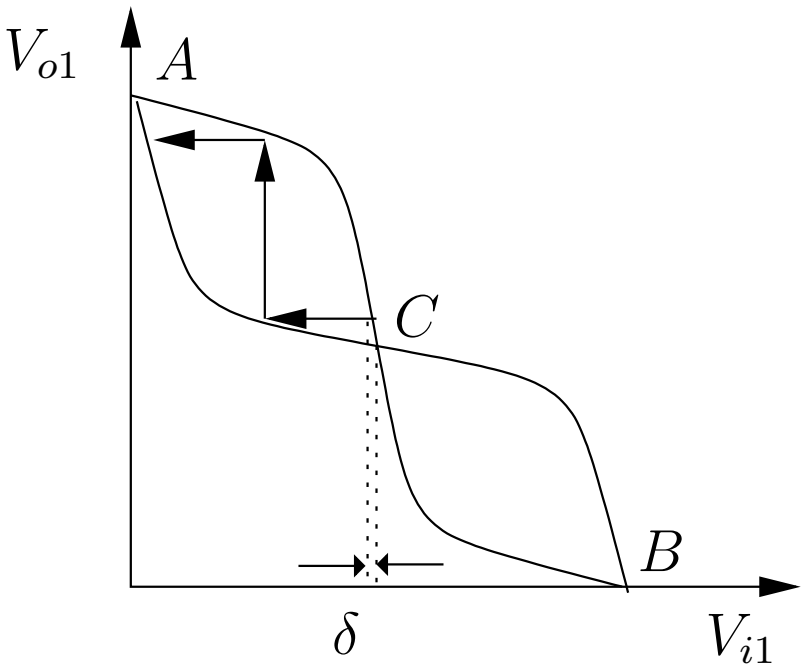


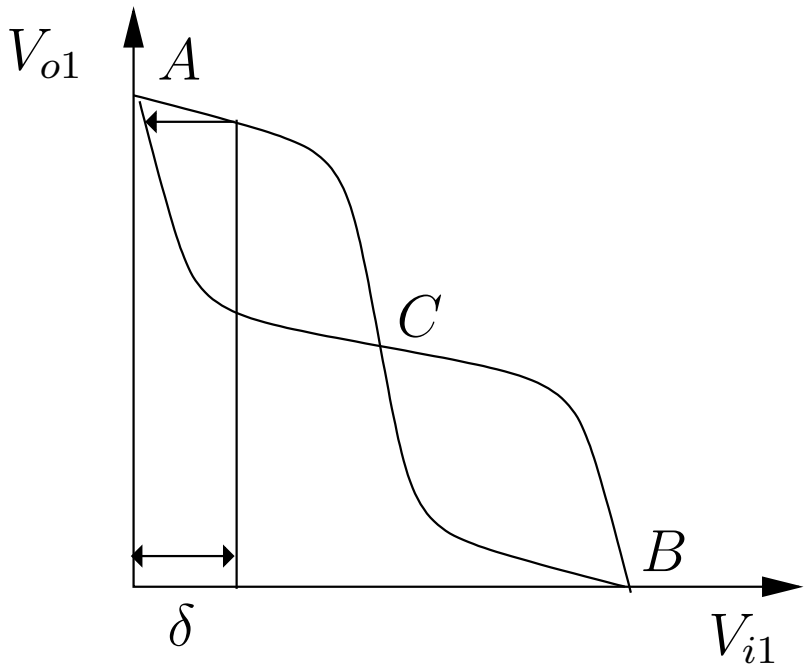


- A and B are stable operating points
- C is a *Metastable* point

Metastability





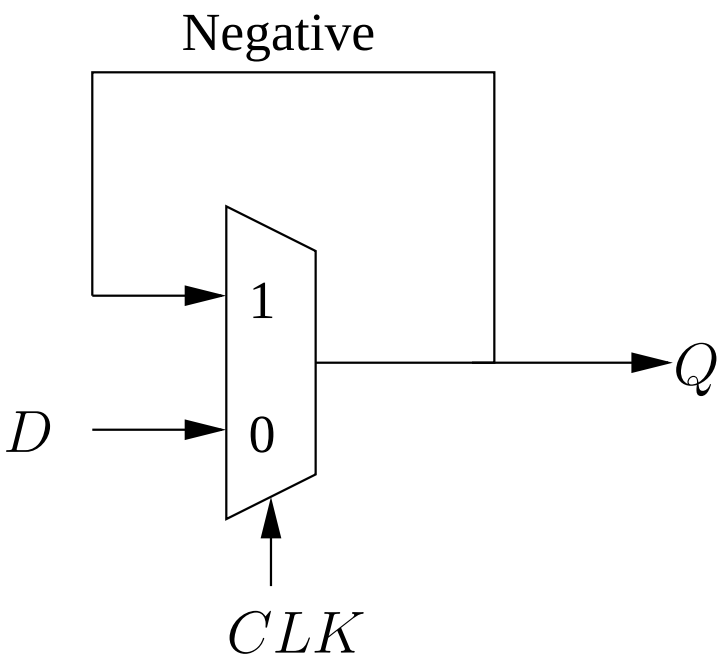


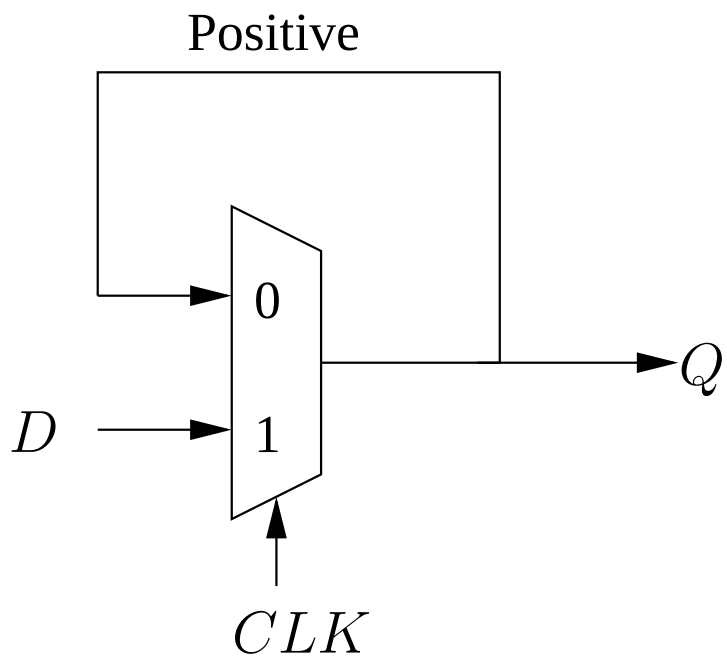
- C - A small noise will take the output to either 0 or V_{DD}
- A, B - Stable points which is inmmune to large noise

Switching Bistable States

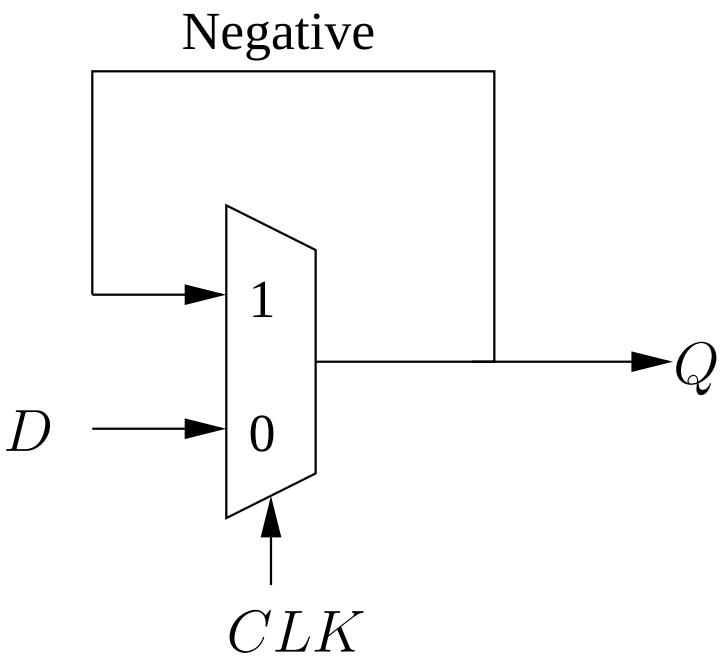
- Breaking the Feedback loop - Multiplexer based latch
- Overpowering Feedback loop - Common in SRAMs

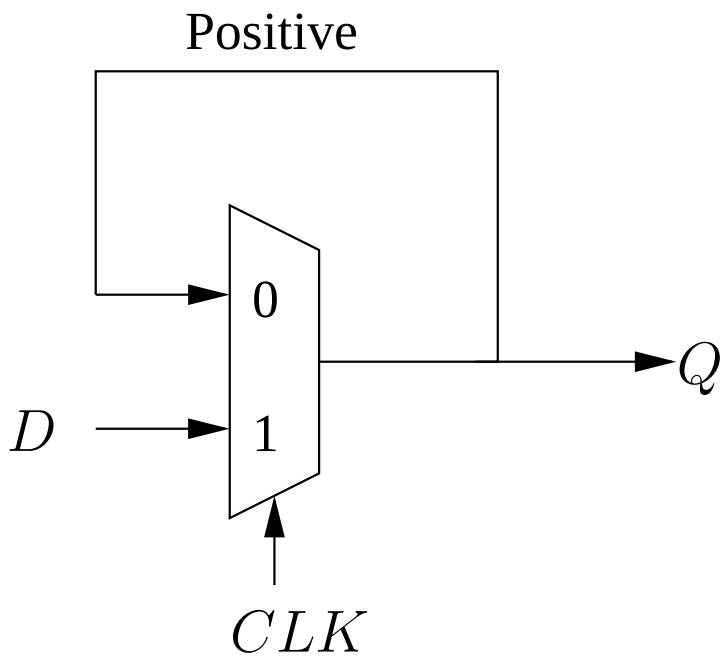
Multiplexer Based Latches



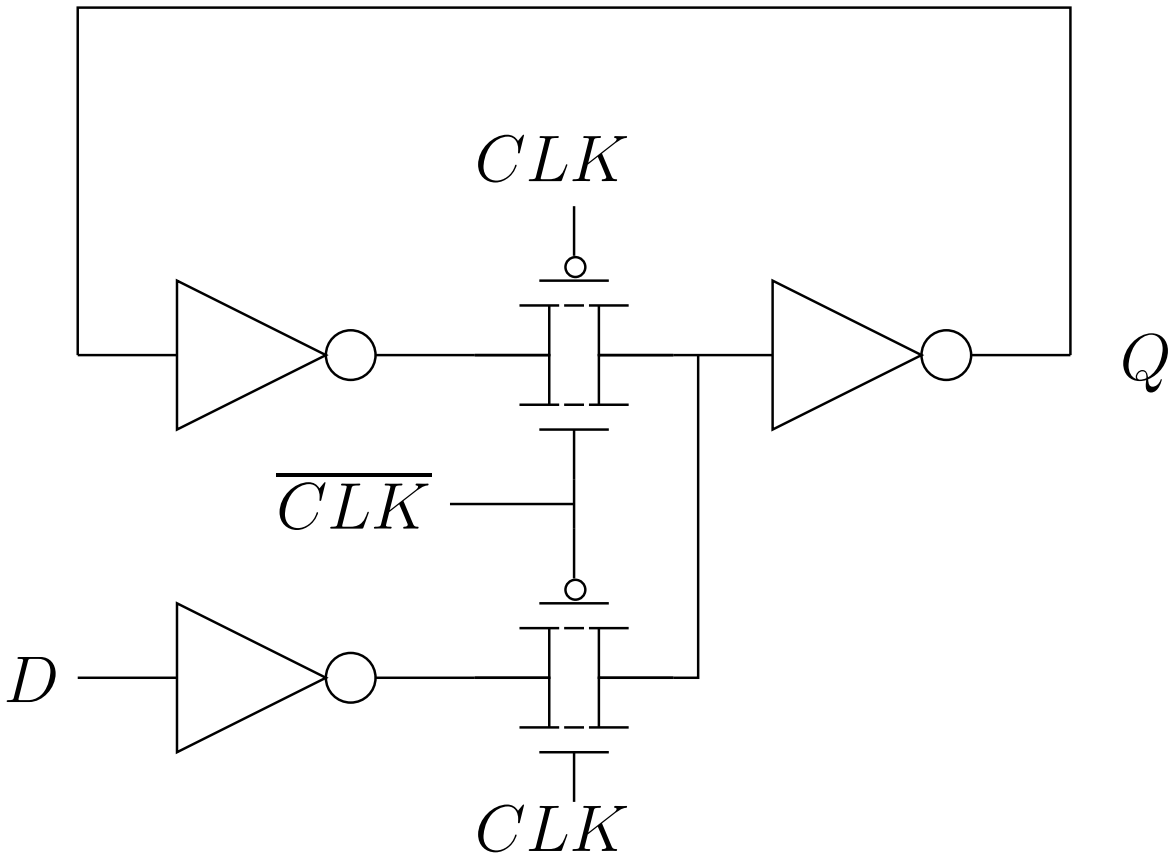


Multiplexer Based Latches



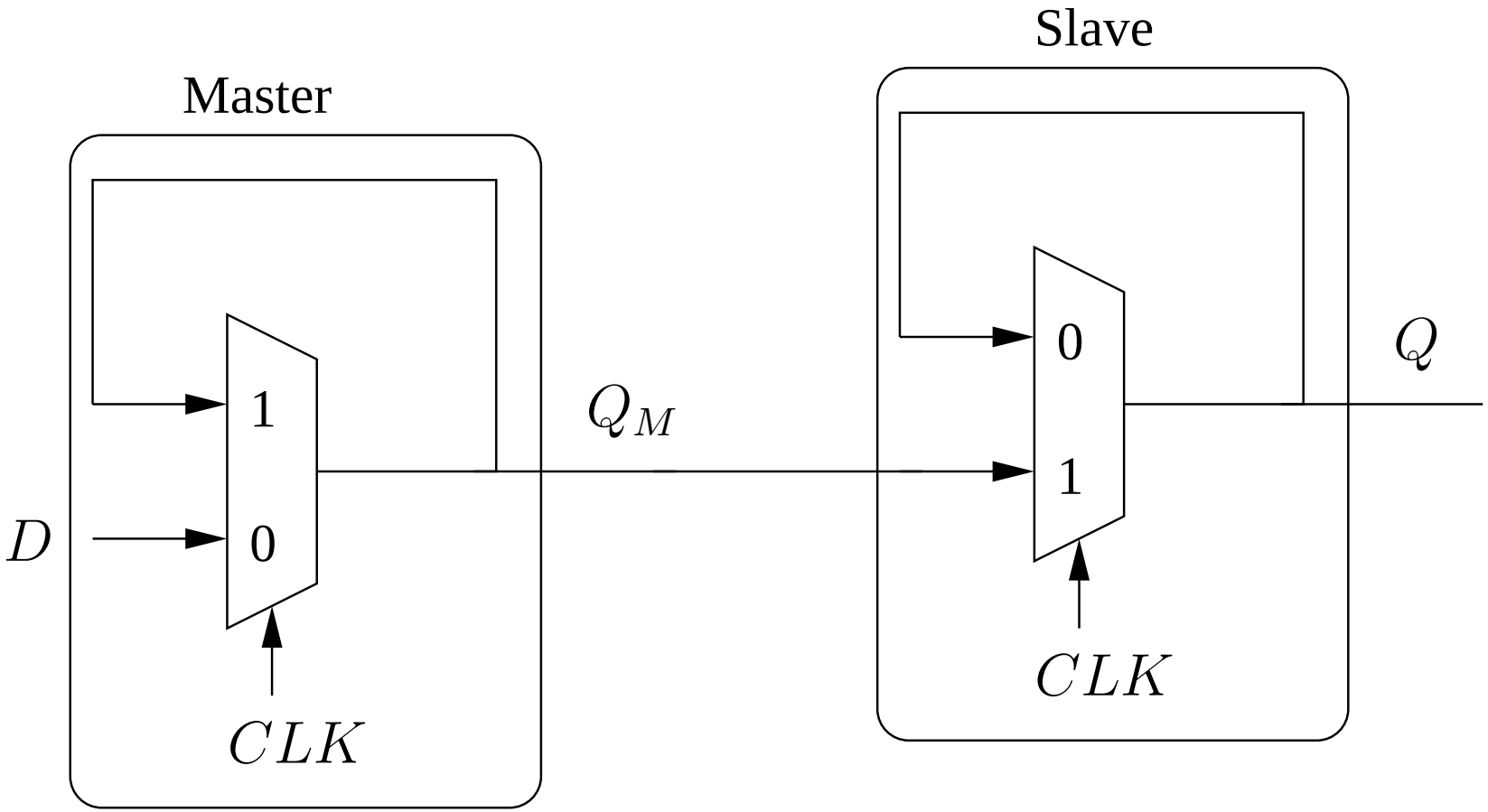


Multiplexer Based Latches



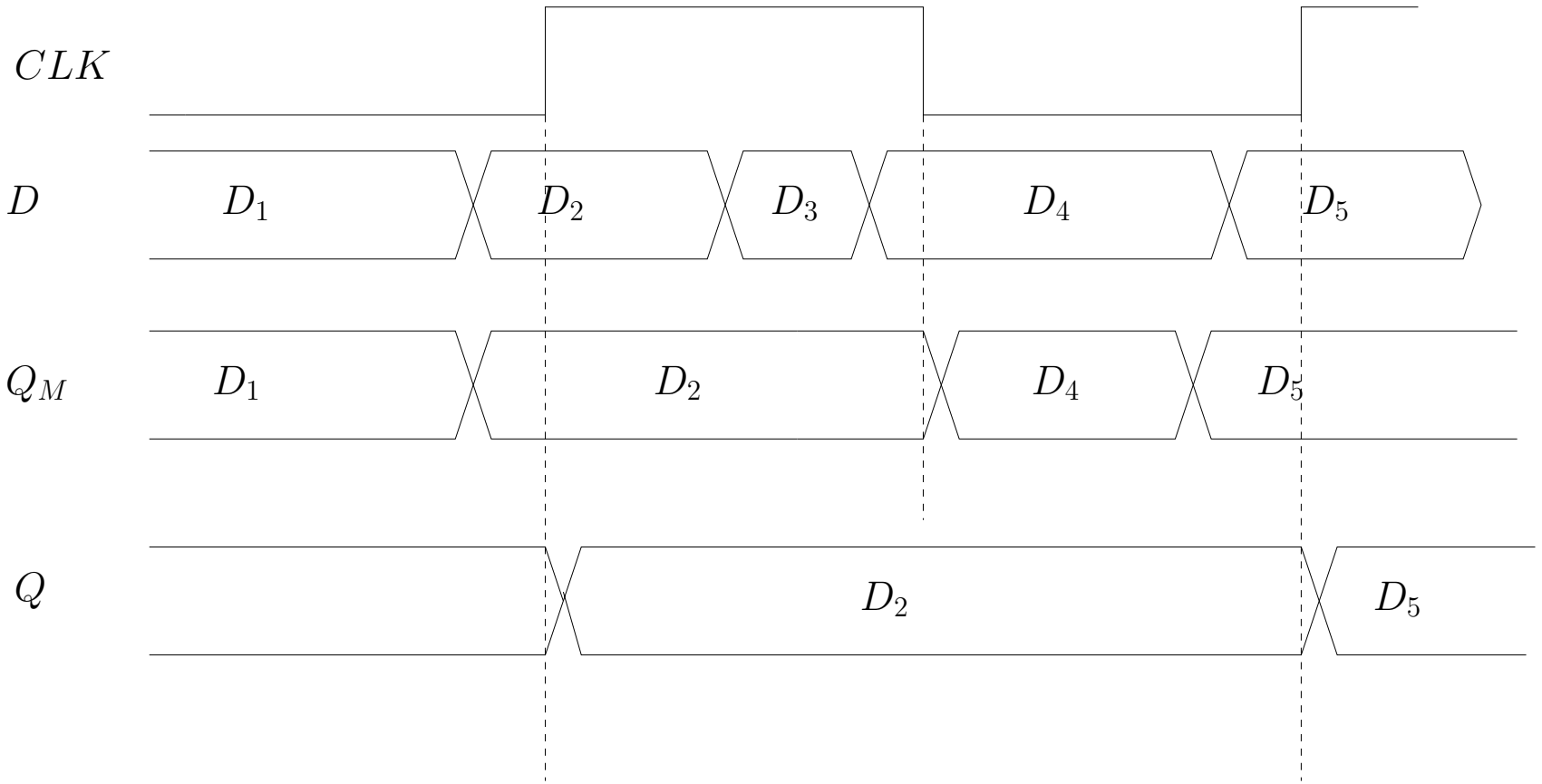
- Clock load is very high - FOUR transistors

Multiplexer Based Flip Flop



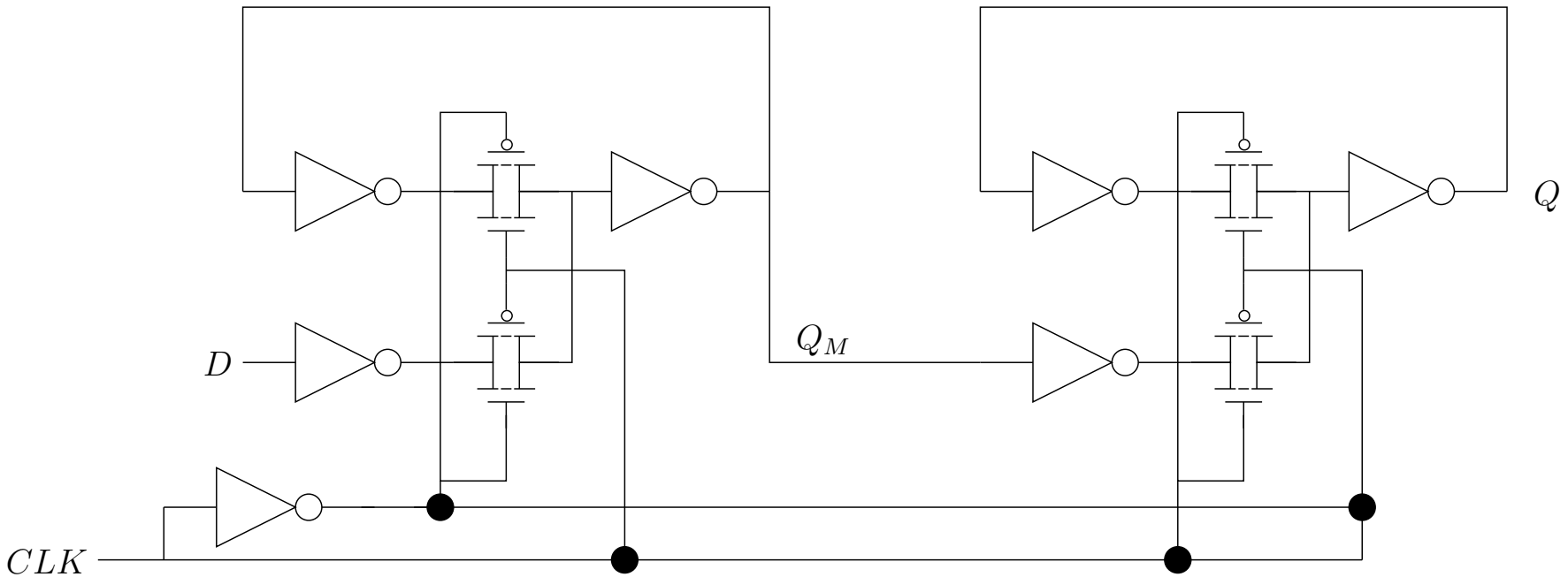
Master-Slave Positive edge triggered Flip Flop

Multiplexer Based Flip Flop Timing



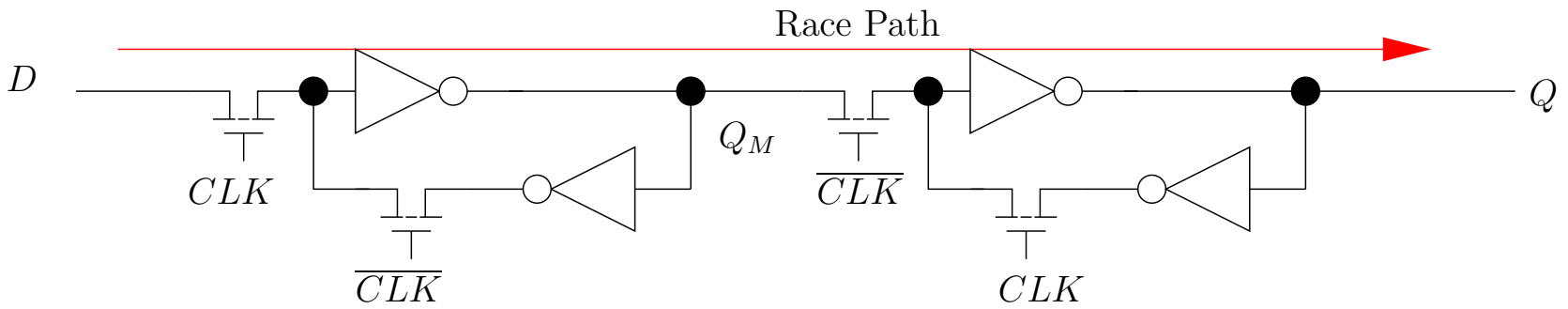
Master-Slave Positive edge triggered Flip Flop - Timing

Multiplexer Based Positive Edge Triggered Flop



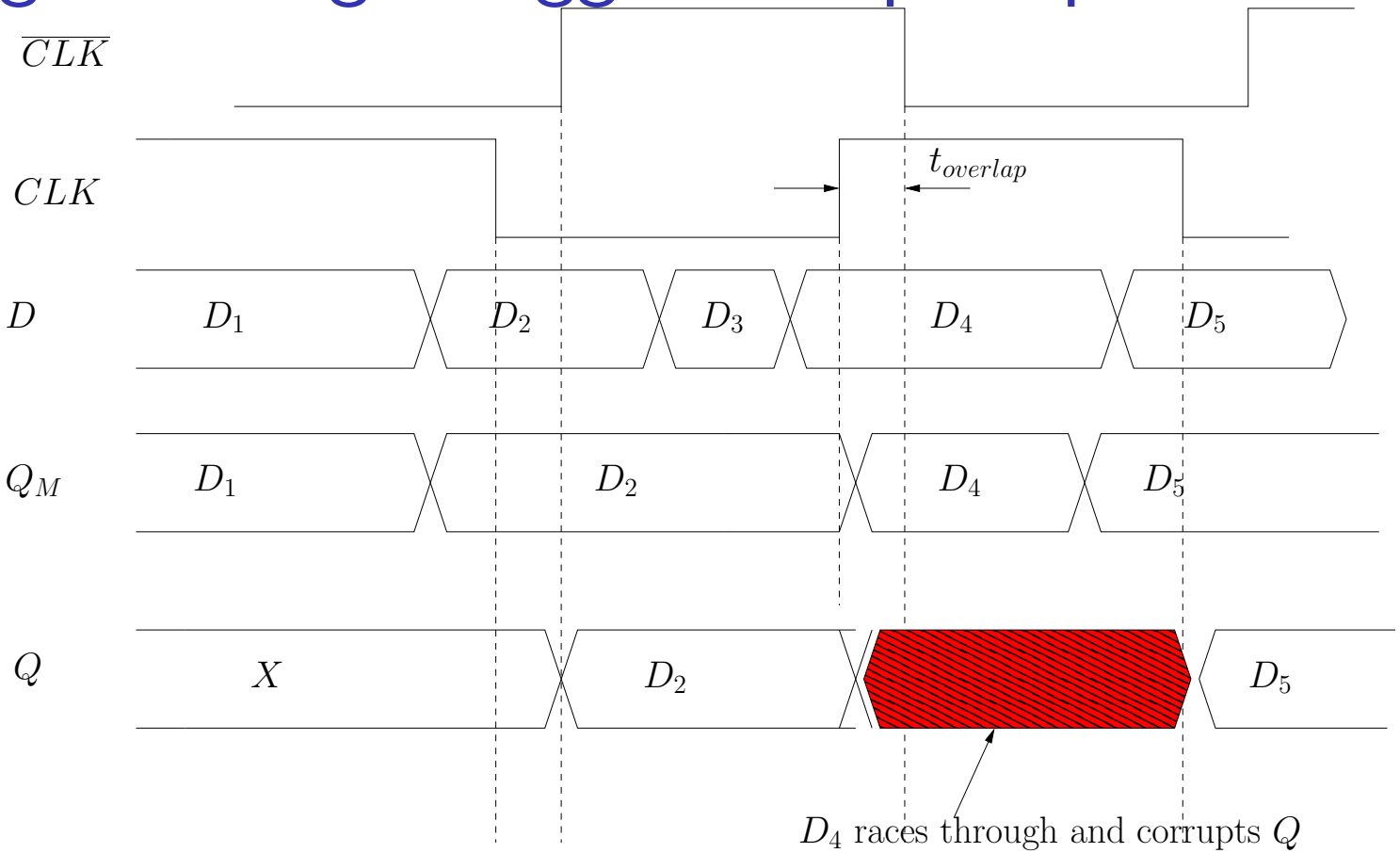
- Clock load is very high - FOUR transistors

Negative Edge Triggered Flop Race Conditon



- Negative Edge Flop - Race Condition ($CLK = \overline{CLK} = 1$)
- Both latches are transparent at the same time
- ($CLK = \overline{CLK} = 0$) is not a problem because all NMOS pass transistors are OFF
- This flop suffers from:
  - Passing a logic high fully
  - Slow charging time for a logic high (source potential increases)

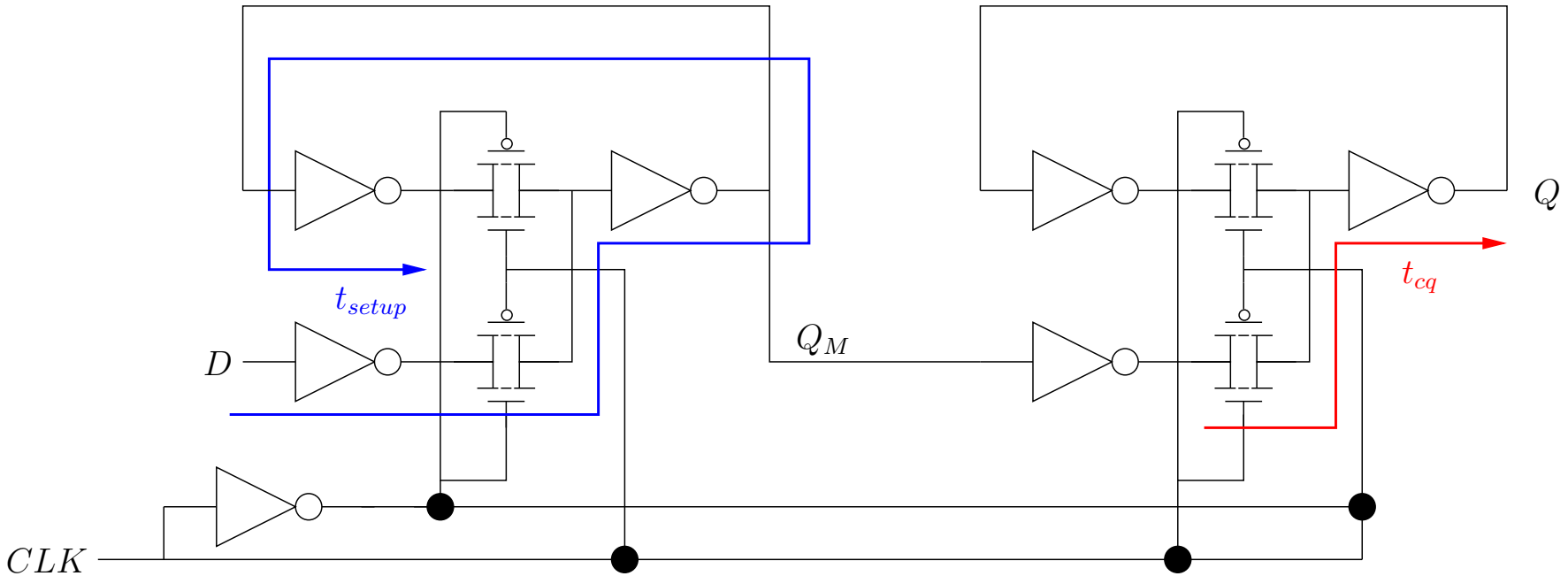
Negative Edge Triggered Flip Flop Race Conditon



Race condition:

- Race condition at sampling edge can be avoided by imposing a hold time constraint
- Beware of race condition on the non-sampling edge

Multiplexer Based Flop - Setup and Hold Times

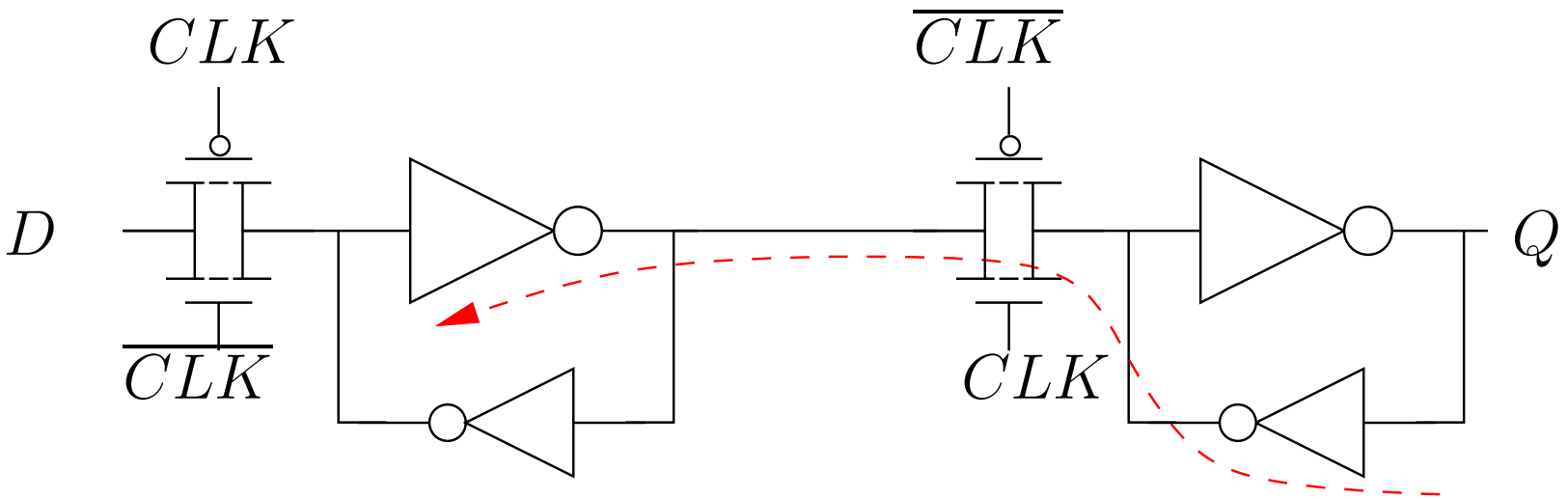


$$t_{setup} = 3t_{inv-pd} + t_{tx-pd}$$

$$t_{cq} = t_{pd-tx} + t_{pd-inv}$$

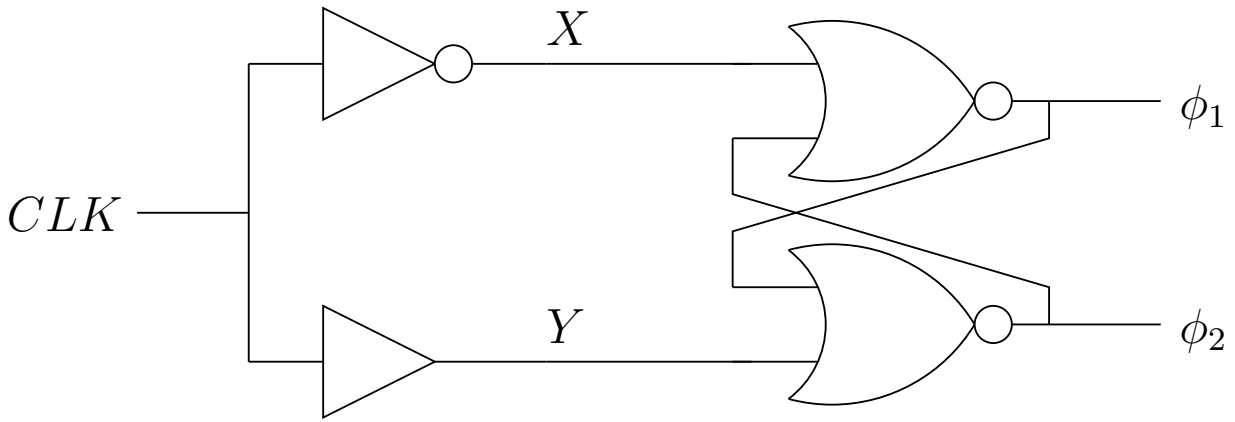
$$t_{hold} = 0$$

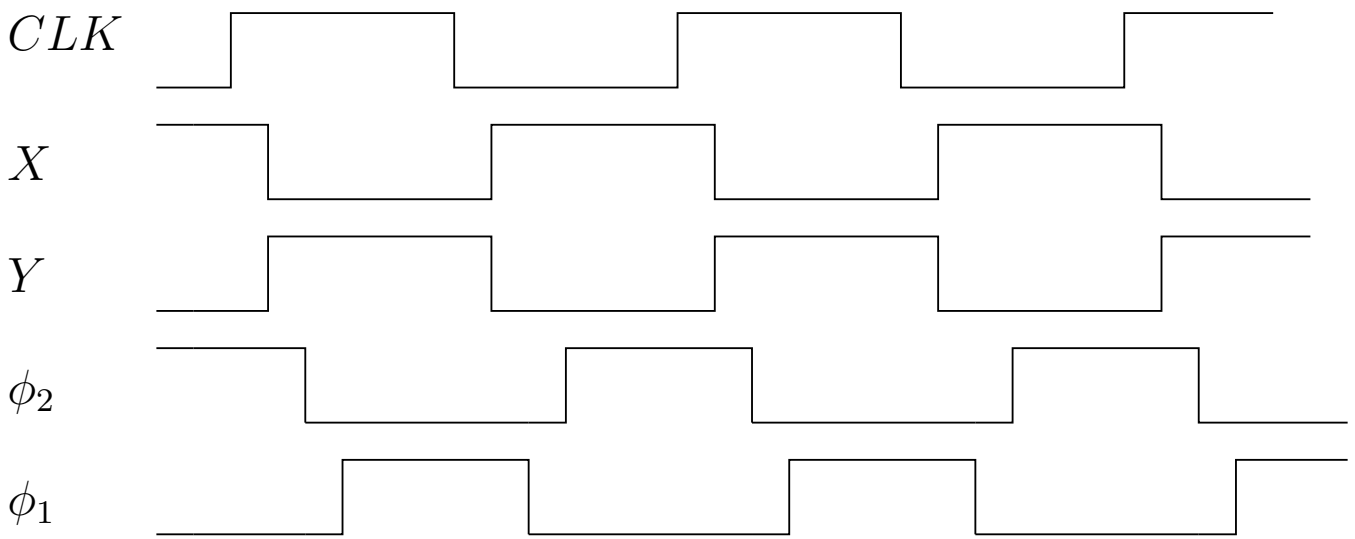
Flops with Overpowering Feedback Loops



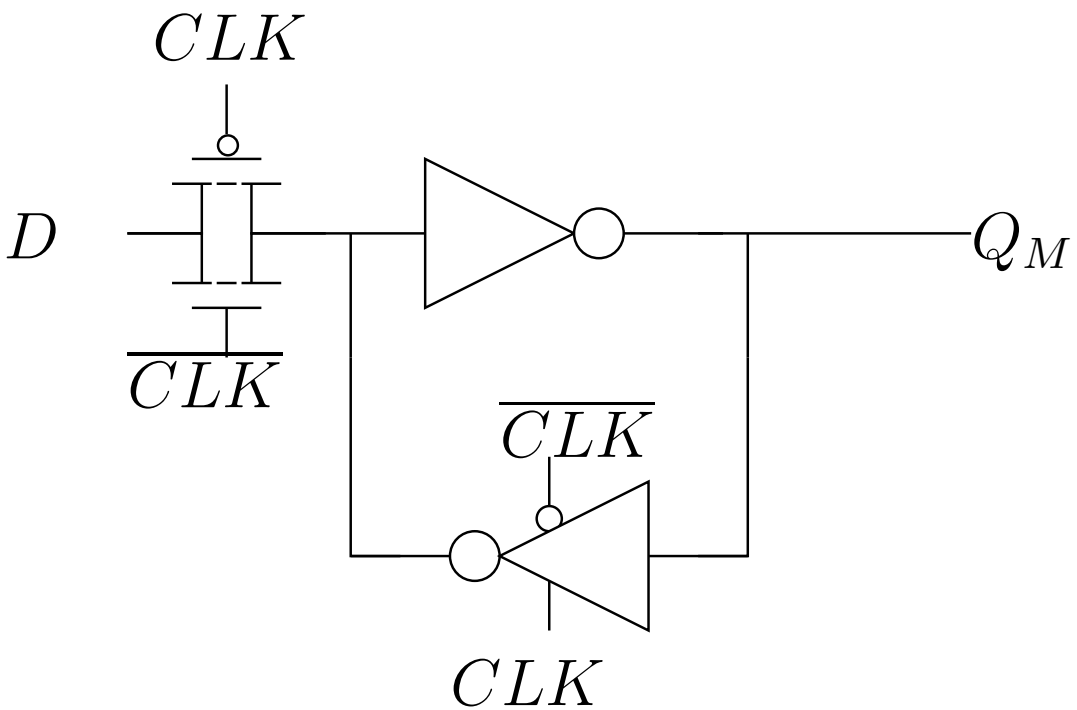
- Driver needs to overpower feedback loop in the master
- Reverse conduction possible
- Need non-overlapping clocks

Non-overlapping Clocks



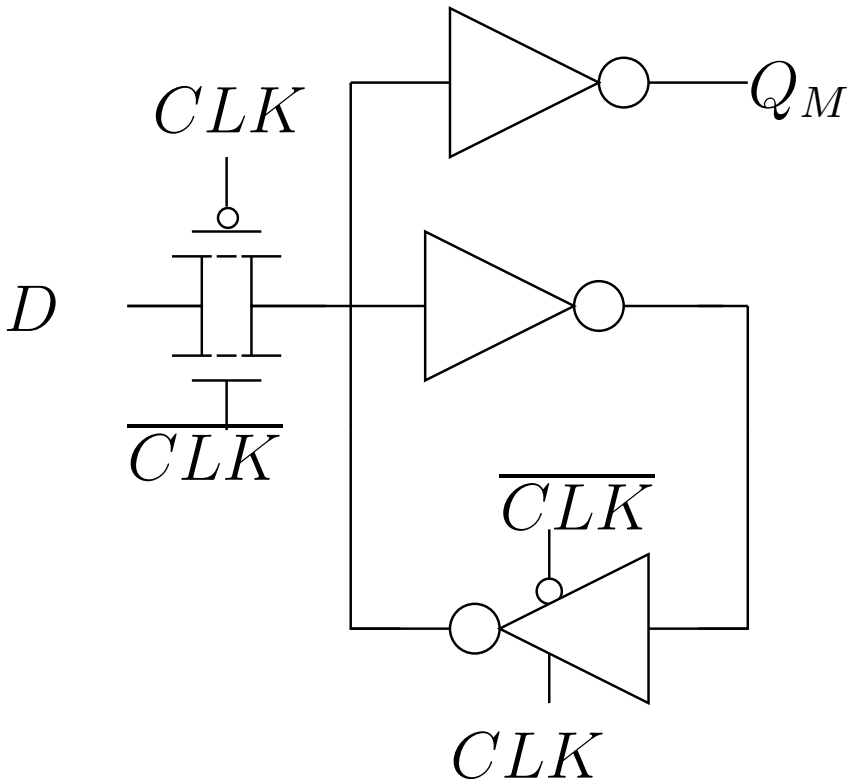


Latch with Tri State Inv in Feedback Loop



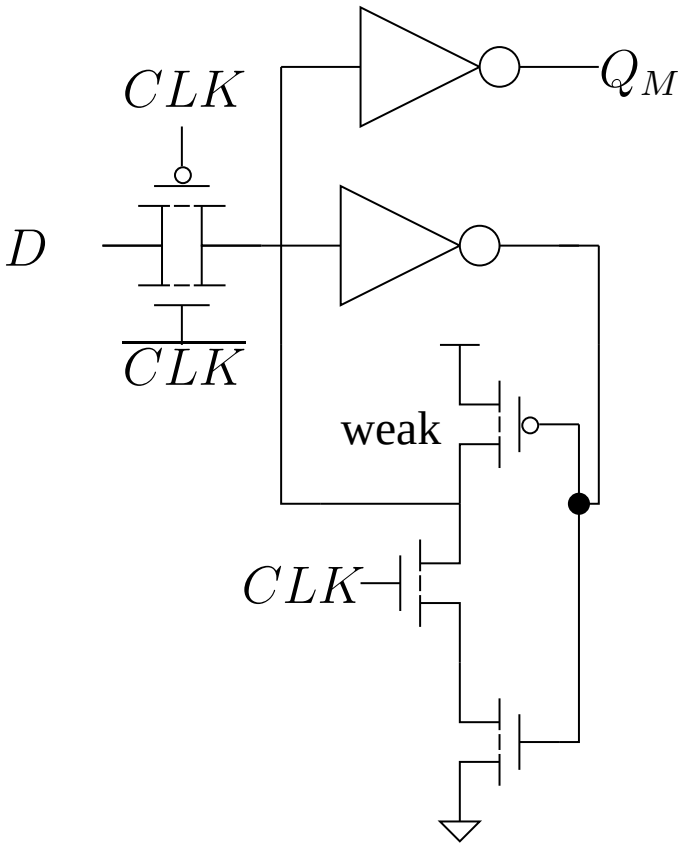
- Inverter + Pass gate in feedback loop = Tri state inverter

Latch with Output Isolation



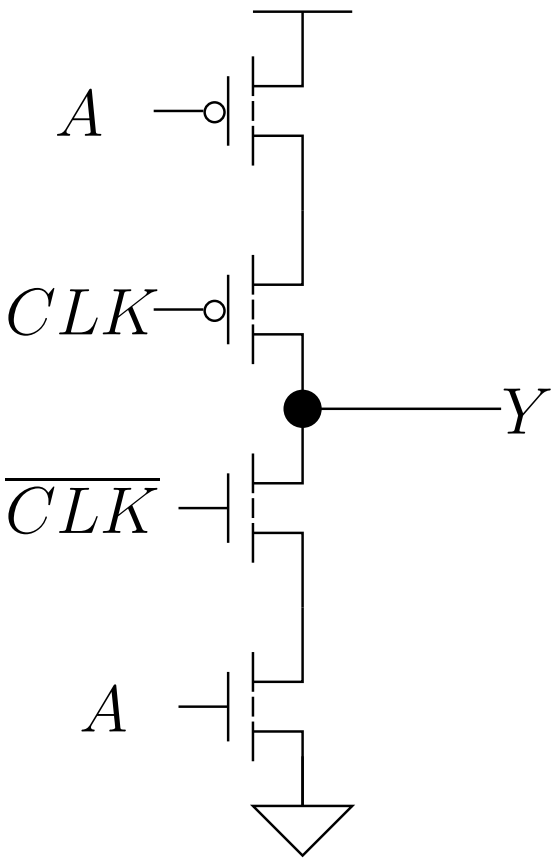
- Noise on the output cannot propagate and disturb the internal state

Itanium 2 Latch



- Break or Overpower Feedback? Break 0 and overpower 1.
- Lesser area needed to overpower weak PMOS with strong NMOS

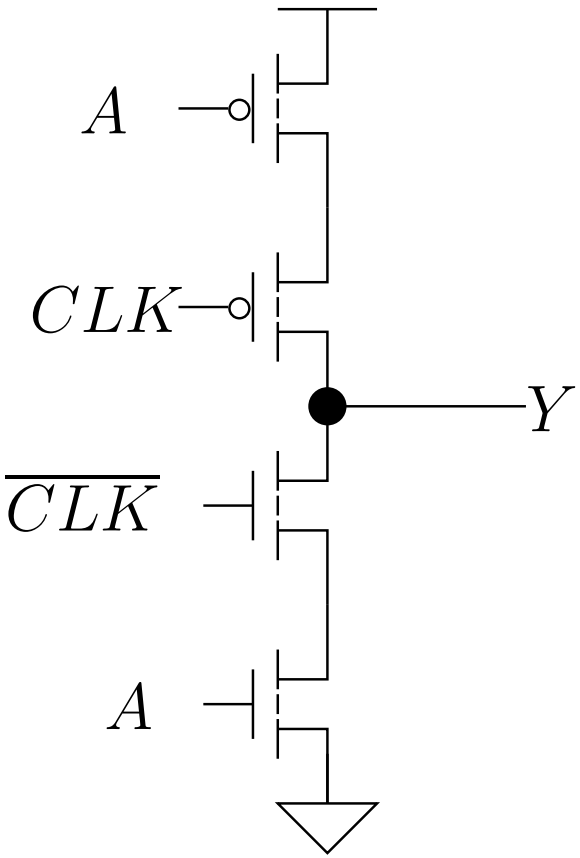
Tri State Inverter Dynamic Latch



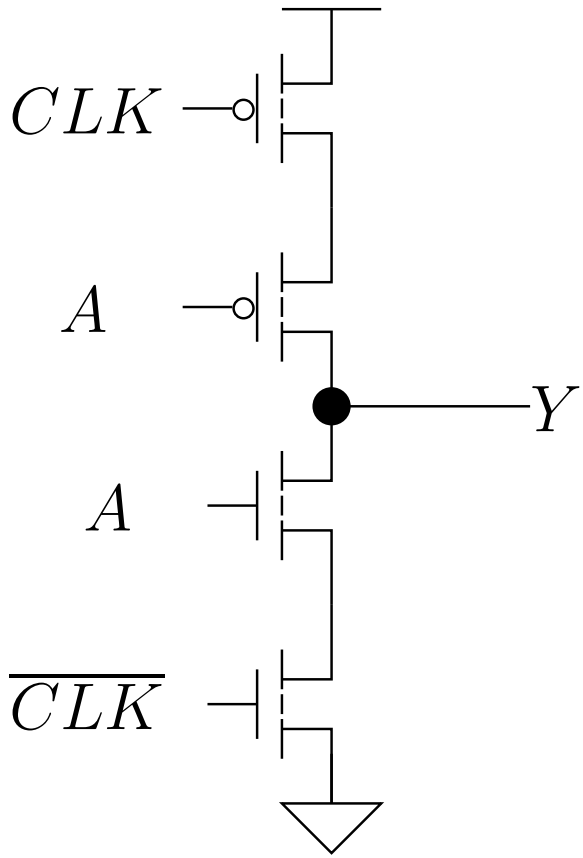
Tri−State Inverter

- Data stored dynamically on a capacitor

Tri State Inverter Dynamic Latch



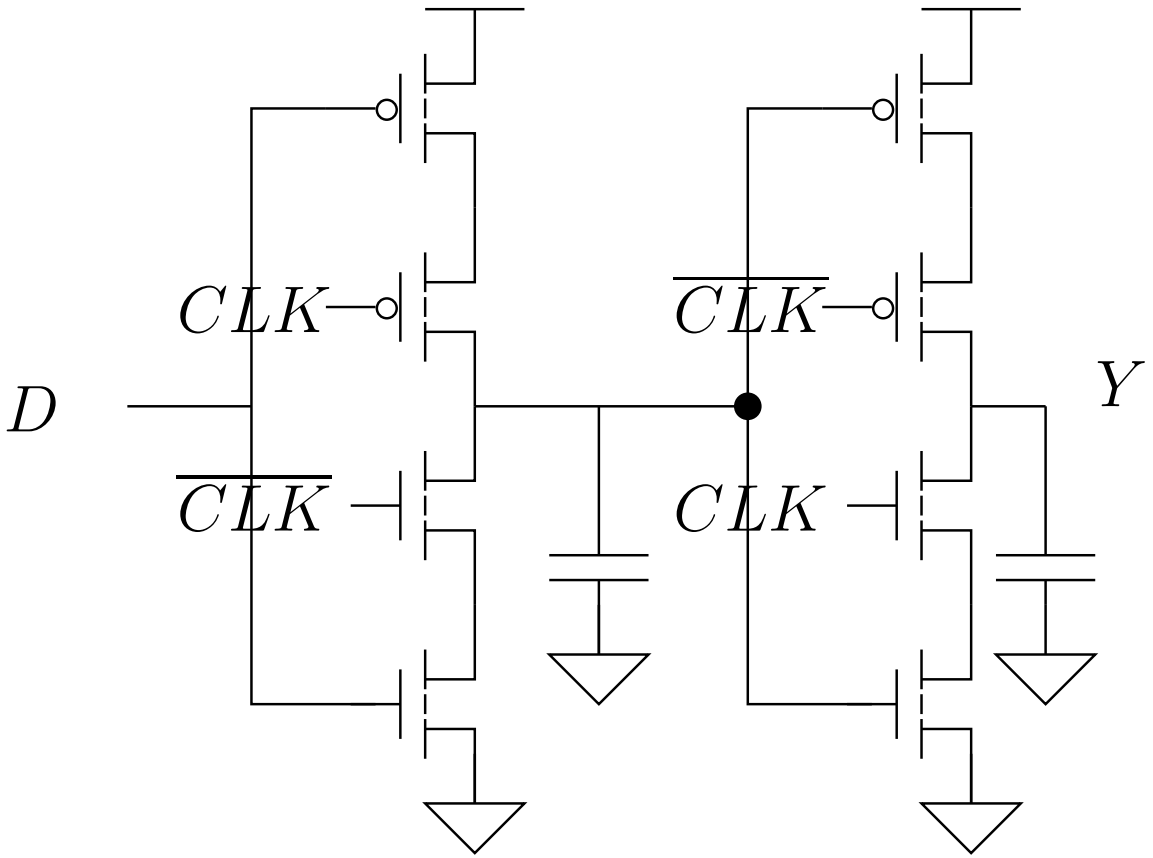
Tri−State Inverter



Bad Implementation

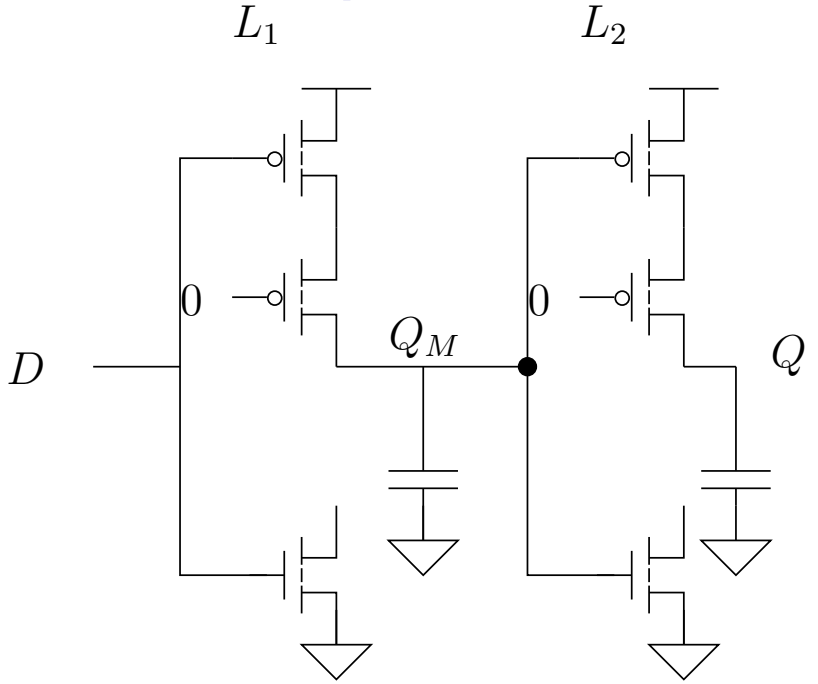
- Charge sharing is a serious problem in the bad implementation

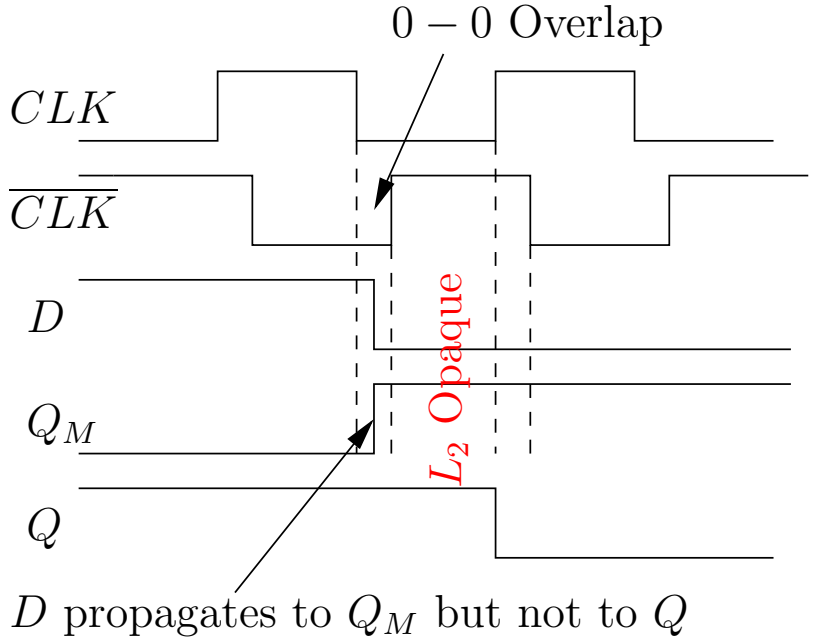
C2MOS Flop Positive Edge Triggered



- Insensitive to clock overlap

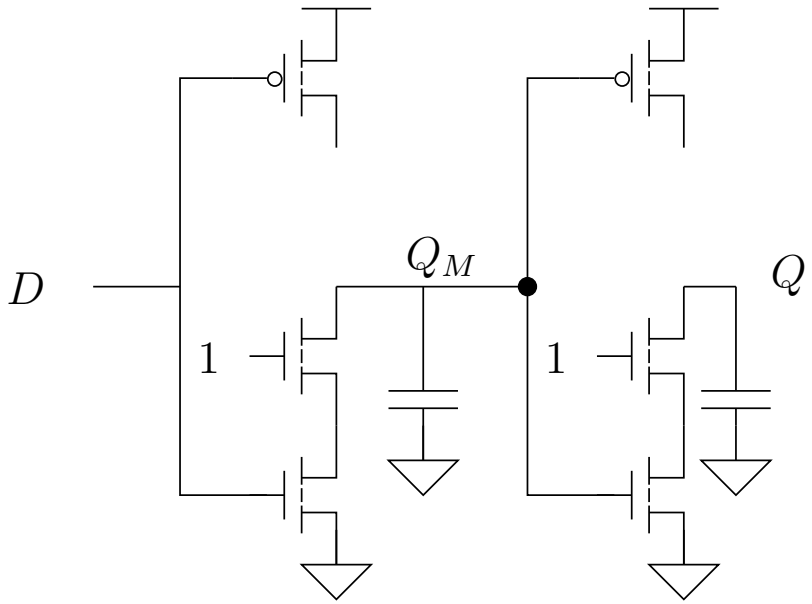
C2MOS Flop - 00 Overlap

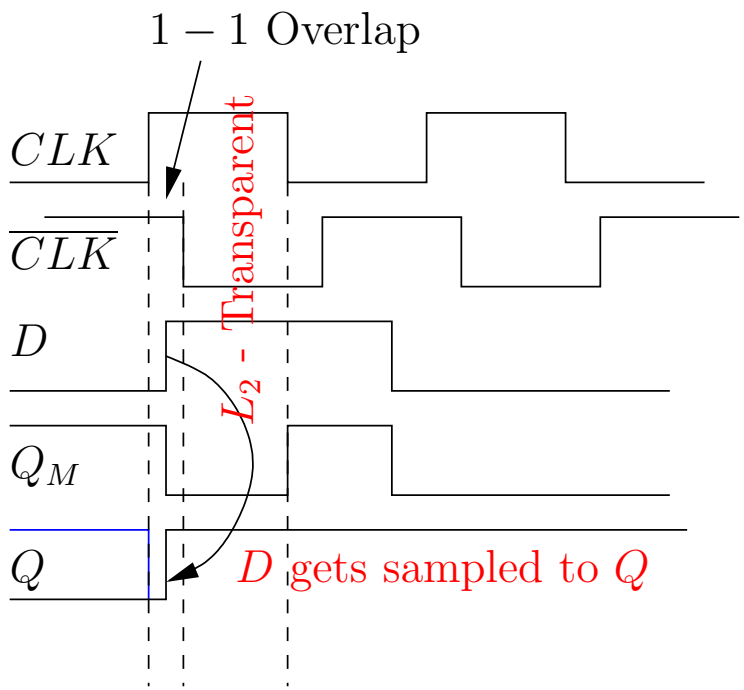




- Positive Edge Triggered Flop: $0-0$ overlap
- Post the overlap L_2 becomes opaque
- Data cannot go through from $D \rightarrow Q$
- Data inversion does the trick
- Race conditon requires PMOS in L_1 and NMOS L_2 to be ON - Not possible

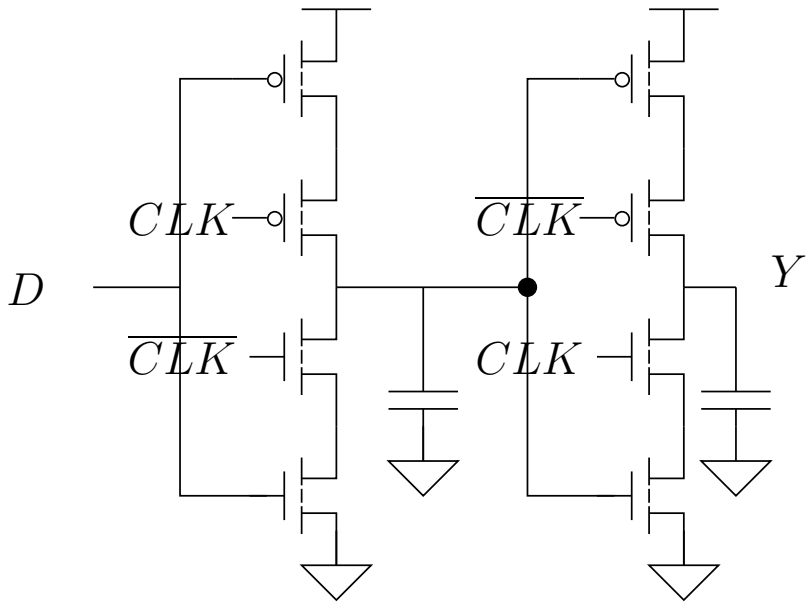
C2MOS Flop - 11 Overlap





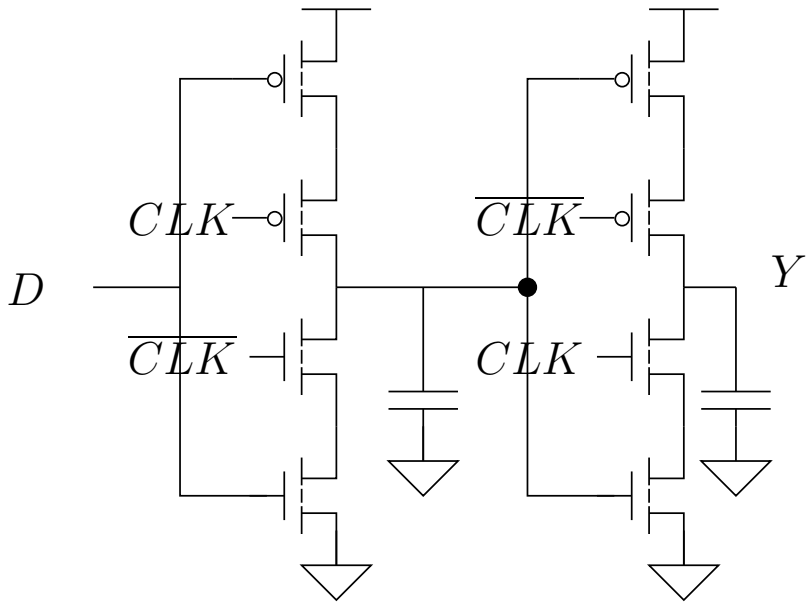
- Positive Edge Triggered Flop: $1-1$ overlap
- Data will go through from $D \rightarrow Q$
- Post the overlap L_2 becomes transparent - Turns on PMOS in $L2$
- Need to impose hold time constraint

C2MOS Flop - Timing Parameters



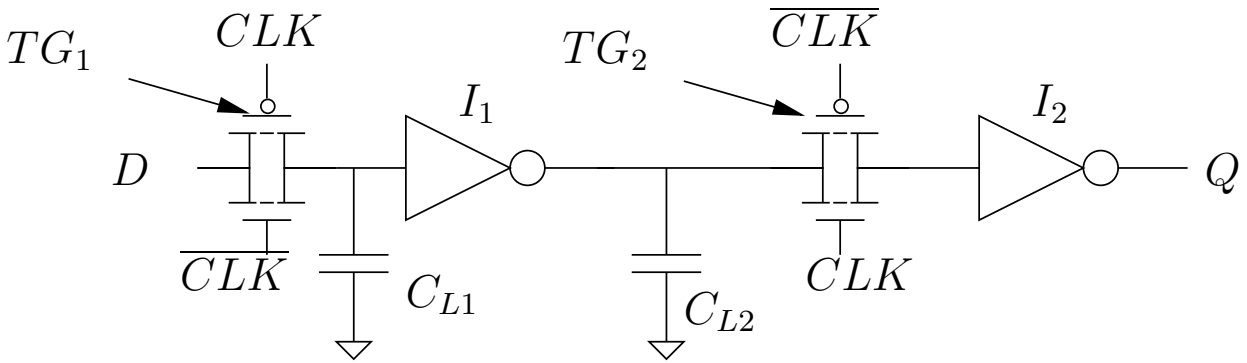
- Assumption: Clock edges are instantaneous and have no overlap
- $t_{setup} = ?$
- $t_{hold} = ?$
- $t_{cq} = ?$

C2MOS Flop - Timing Parameters



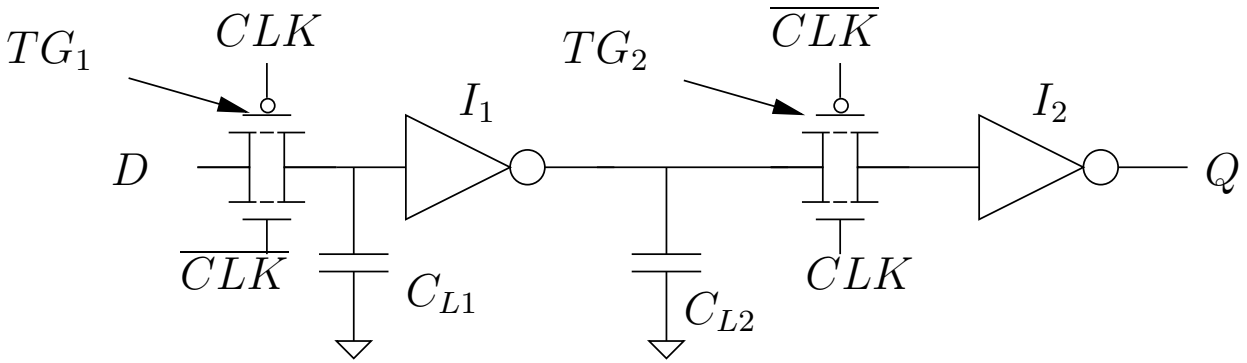
- Assumption: Clock edges are instantaneous and have no overlap
- $t_{setup} = L_1$ Tri state inverter delay
- $t_{hold} = 0$
- $t_{cq} = L_2$ Tri state inverter delay

Transmission Gate Based Flop



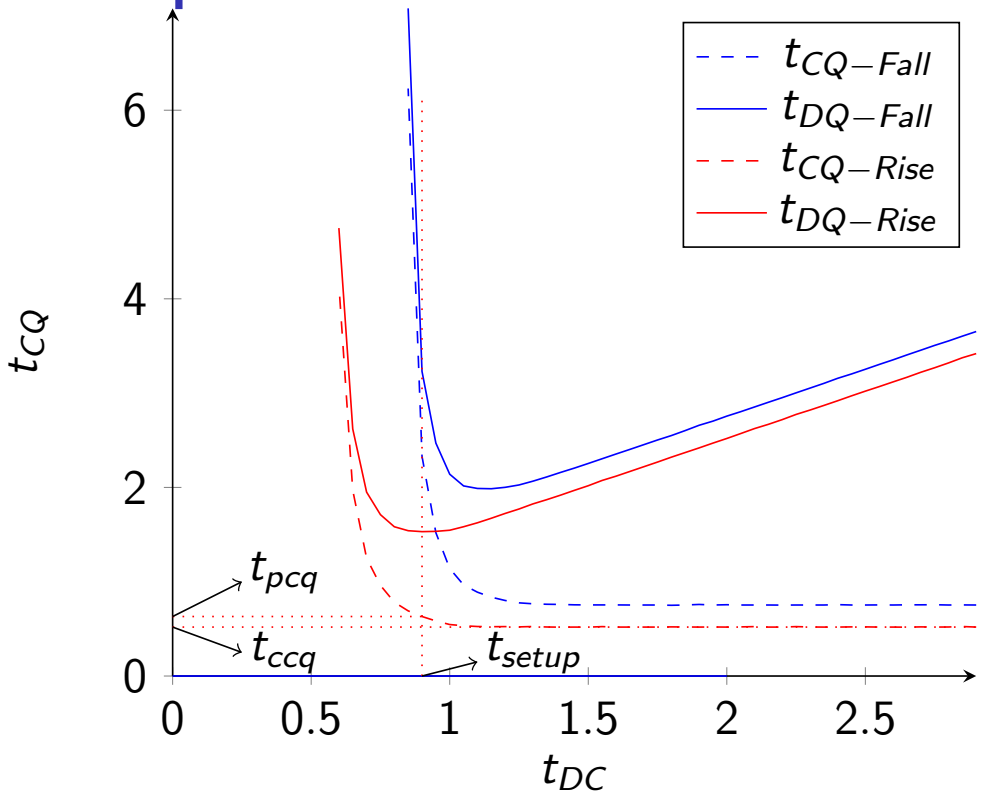
- Assumption: Clock edges are instantaneous and have no overlap
- $t_{setup} = ?$
- $t_{hold} = ?$
- $t_{cq} = ?$

Transmission Gate Based Flop



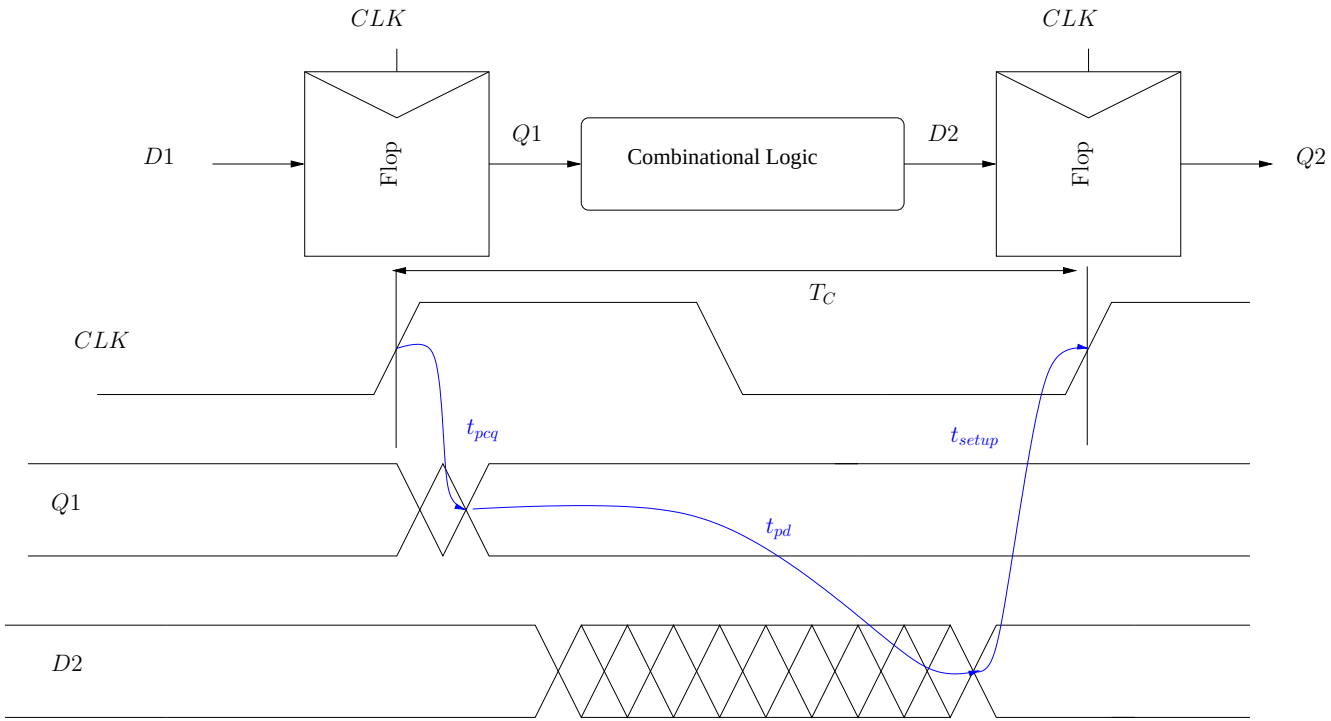
- Assumption: Clock edges are instantaneous and have no overlap
- $t_{setup} = t_{TG_1}$
- $t_{cq} = t_{I_1} + t_{TG_2} + t_{I_2}$
- $t_{hold} = 0$

Flip Flop Characterization



- As data to clock (t_{DC}) reduces, t_{CQ} increases
- $t_{DQ} = t_{DC} + t_{CQ}$ decreases and then increseas
- t_{setup} - t_{DC} at which t_{DQ} is minimum
- Corresponding t_{CQ} is t_{pcq}
- t_{ccq} - t_{CQ} for large t_{DC}

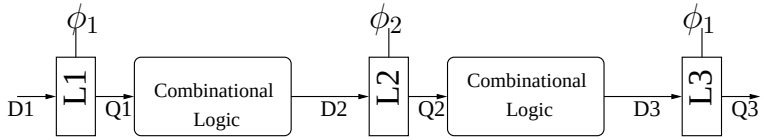
Max Delay Constraint - Flip Flop

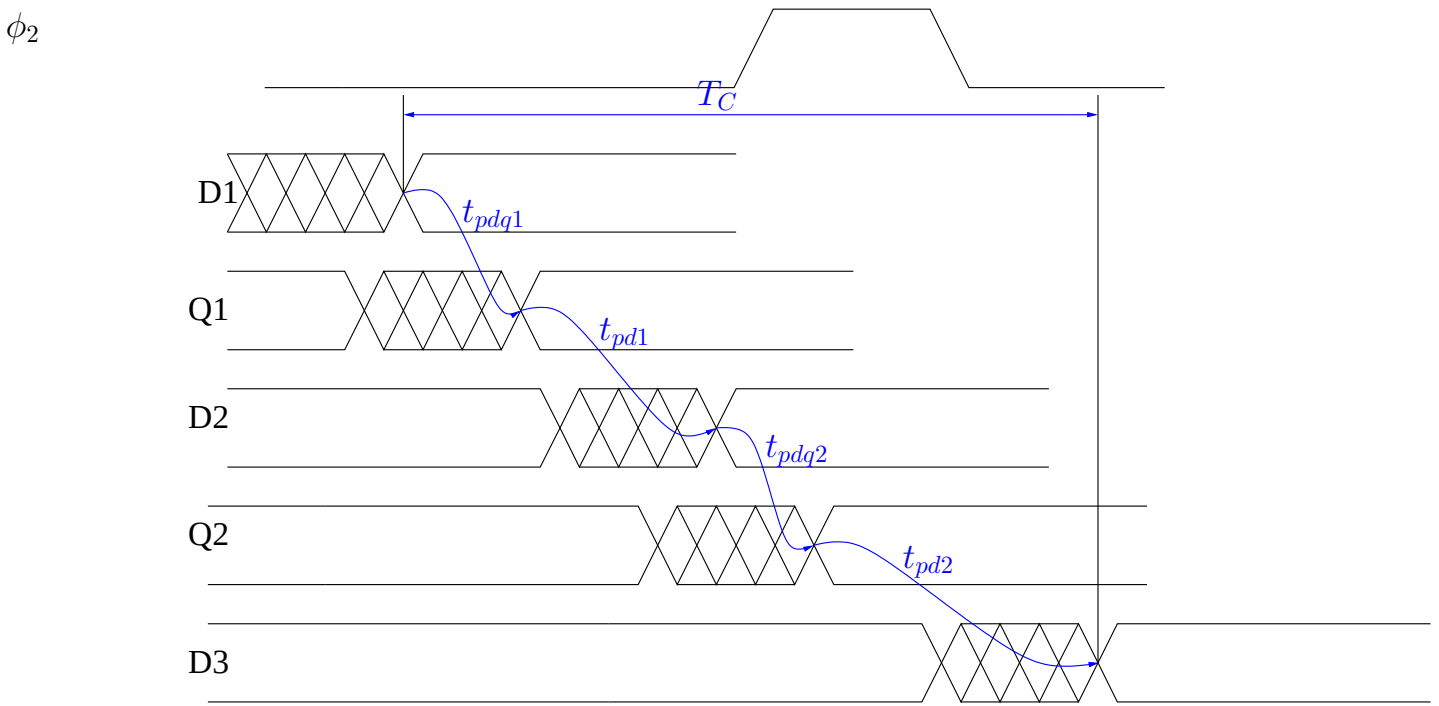


$$T_C \geq t_{pcq} + t_{pd} + t_{setup}$$

$$t_{pd} \leq T_C - (t_{pcq} + t_{setup})$$

Max Delay Constraint - Latch

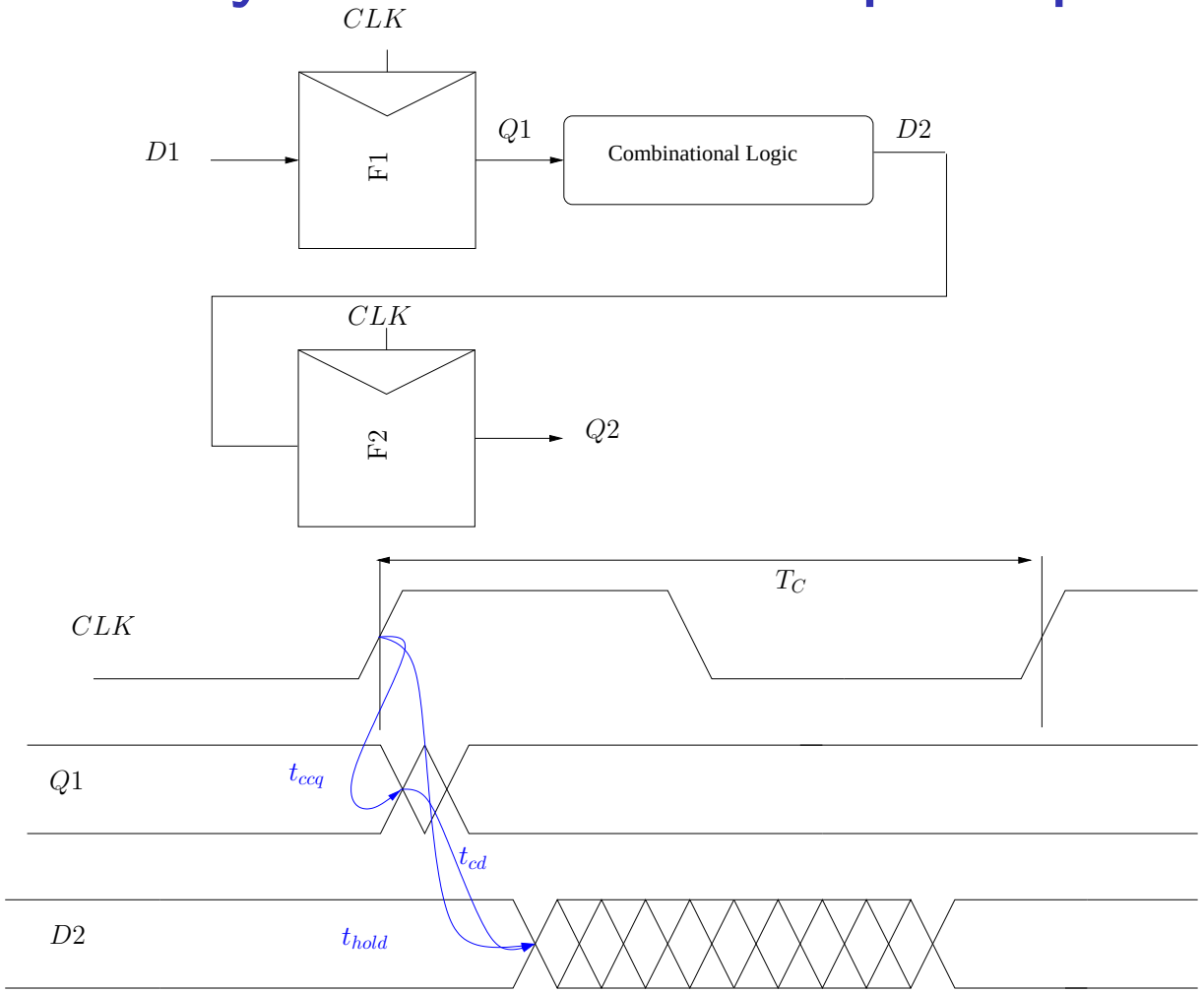




$$T_C \geq t_{pdq1} + t_{pd1} + t_{pdq2} + t_{pd2}$$

$$t_{pd} = t_{pd1} + t_{pd2} \leq T_C - (2t_{pdq})$$

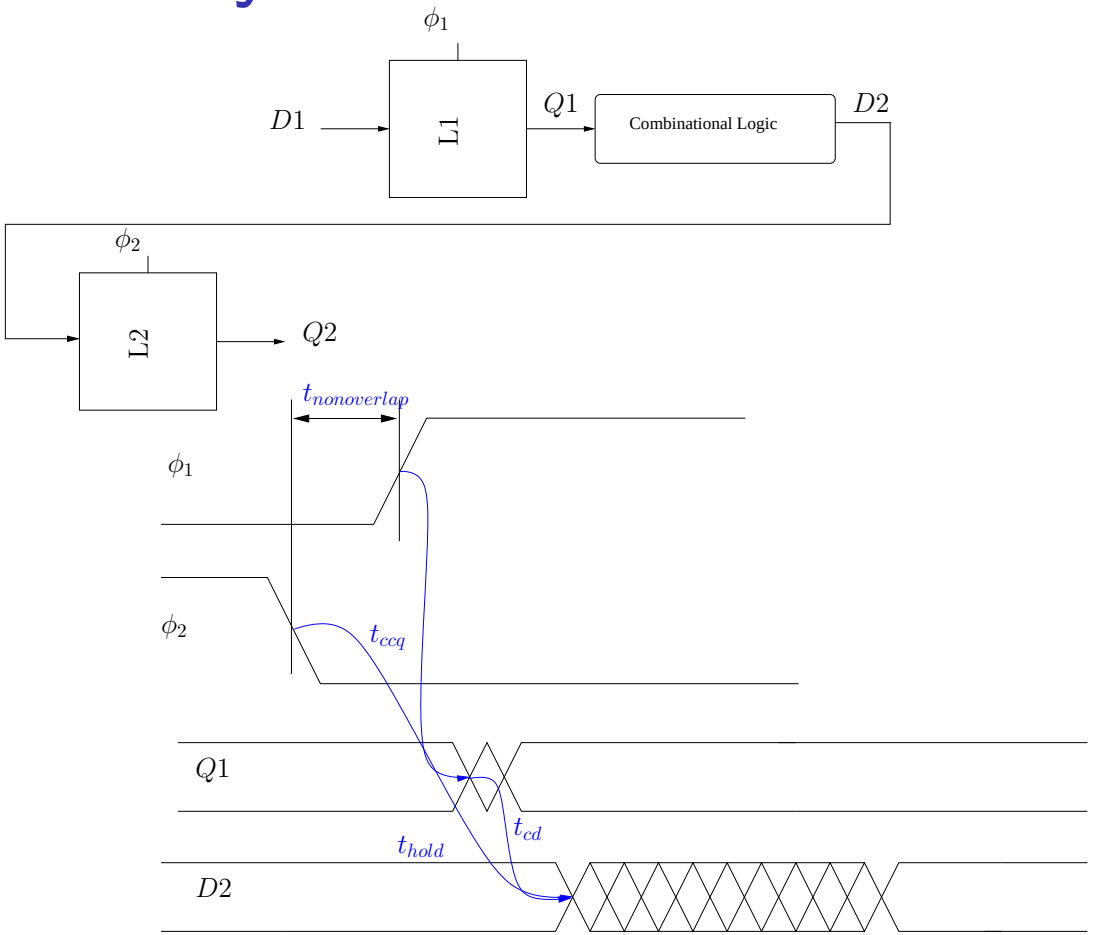
Min Delay Constraint - Flip Flop



$$t_{hold} \leq t_{cd} + t_{ccq}$$

$$t_{cd} \geq t_{hold} - t_{ccq}$$

Min Delay Constraint - Latch



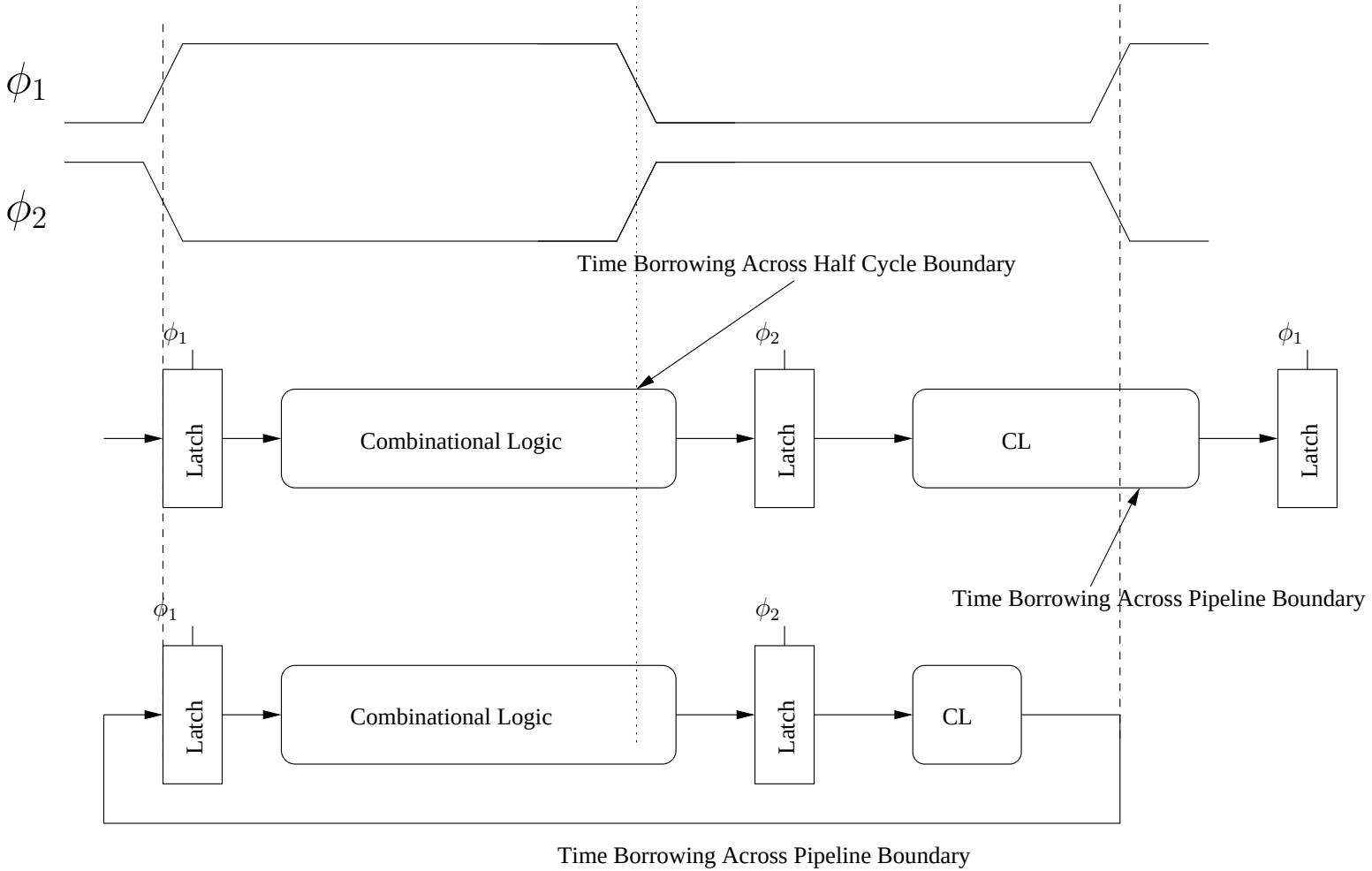
$$t_{hold} \leq t_{cd1}, t_{cd2} + t_{ccq} + t_{nonoverlap}$$

$$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap}$$

Time Borrowing

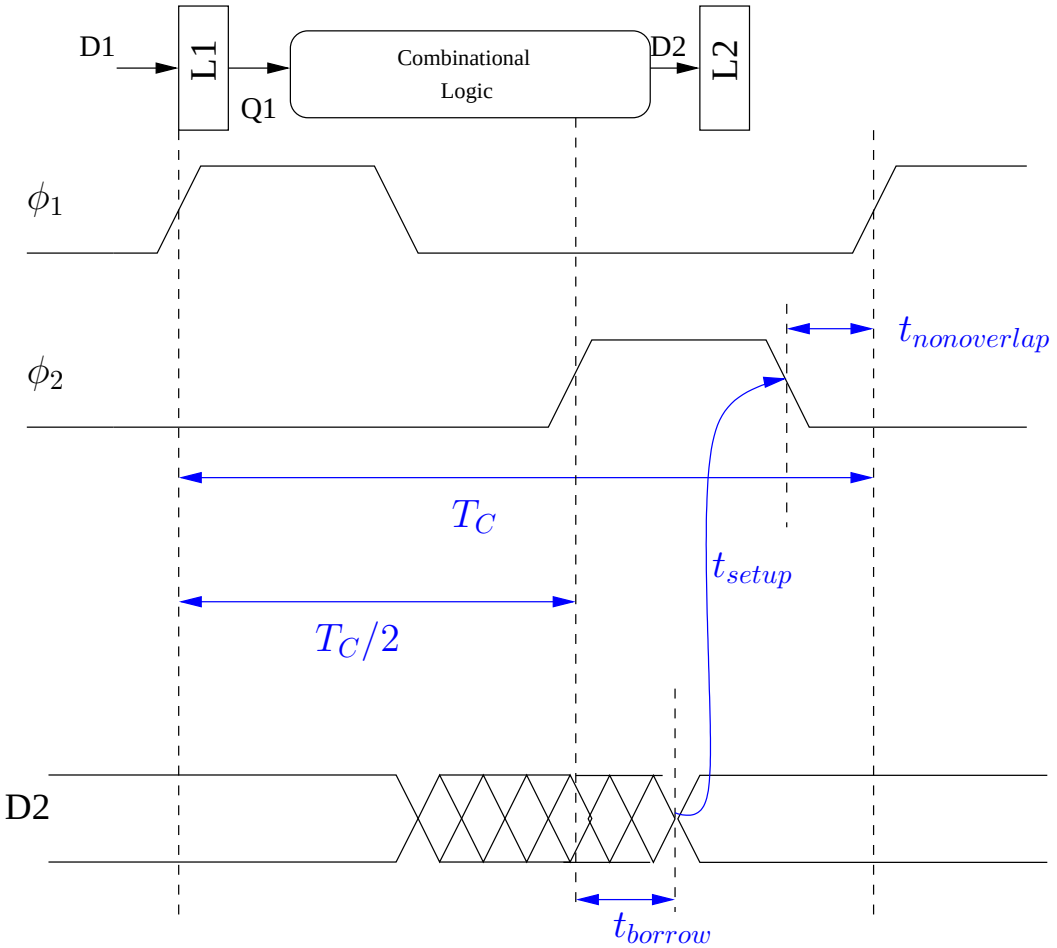
- Flops impose hard edges
- If data arrives late - Error
- If data arrives early - Data is blocked till next edge
- Blocking time is wasted
- Latches allow Time Borrowing
- Data doesn't have to set up until the falling edge

Time Borrowing



- Open loop pipelines can borrow across cycles
- Closed loop pipelines can only borrow across half cycles.

Maximum Time Borrowing

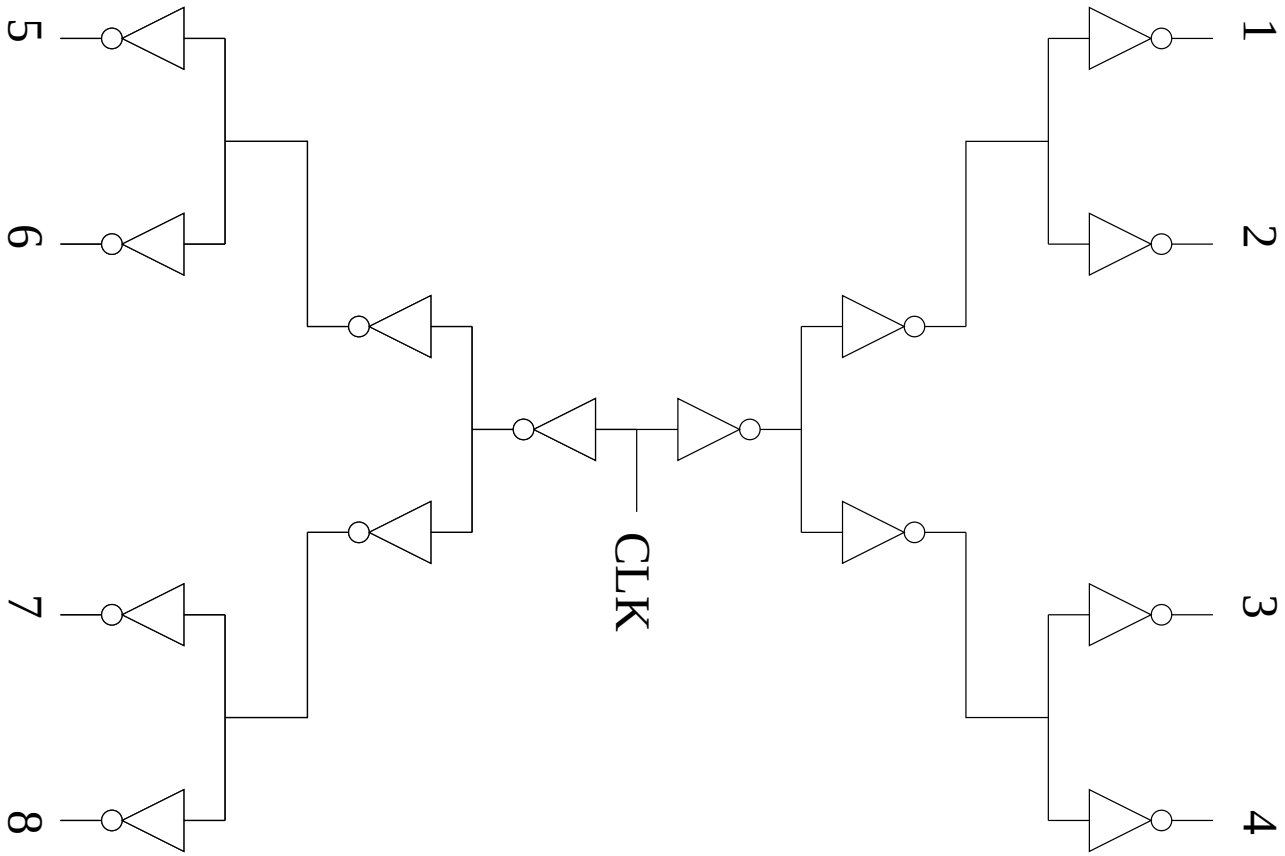


$$t_{borrow} \leq \frac{T_C}{2} - (t_{setup} + t_{nonoverlap})$$

Clock Skew

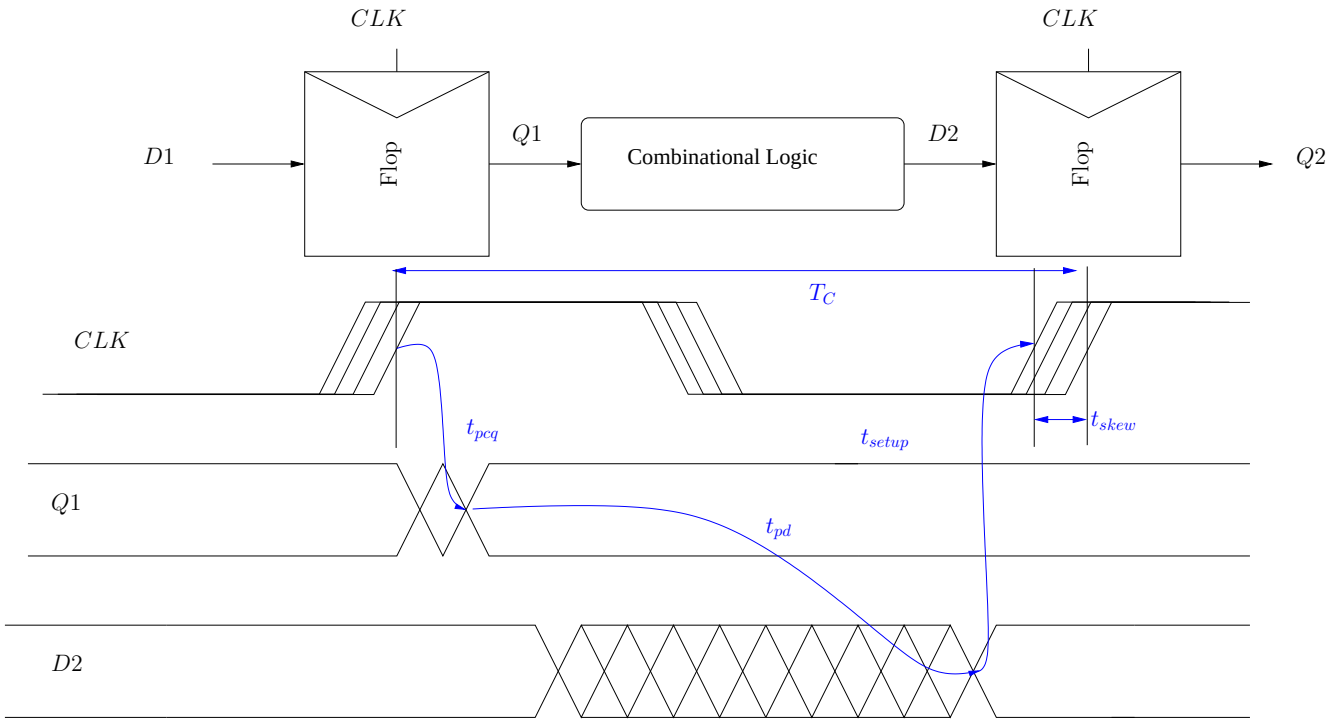
- Clock is routed all through the chip
- Clocks are distributed in a tree structure through buffers
- All clock edges need to arrive at the same time across the chip
- Some variation is inevitable!
- The grid will have some small delay
- Worst case delay is called t_{skew}

Clock Tree



Nodes 1-8 see the same amout of delay and ideally should have no skew

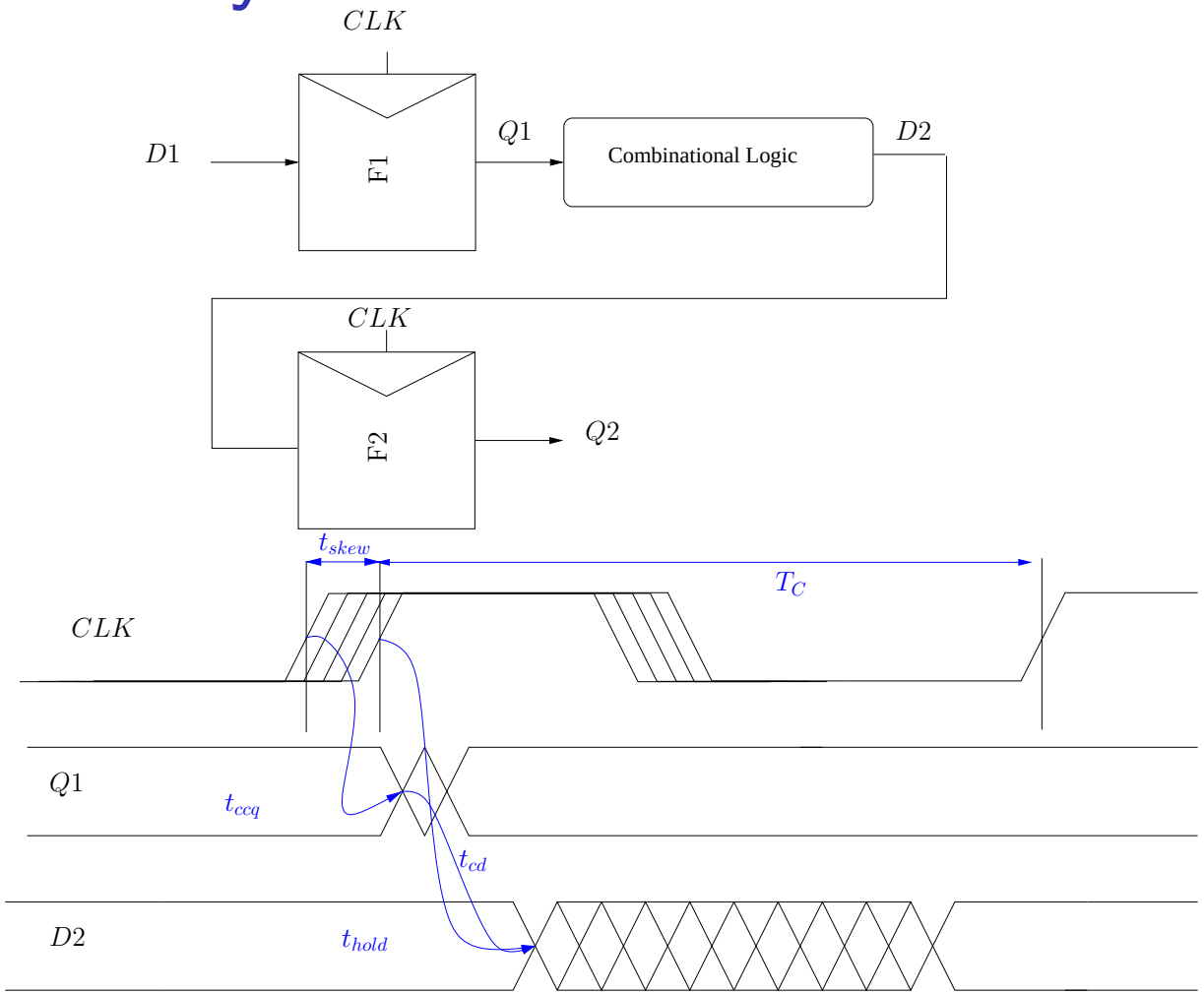
Max Delay Constraint with Skew- Flip Flop



$$T_C \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$t_{pd} \leq T_C - (t_{pcq} + t_{setup} + t_{skew})$$

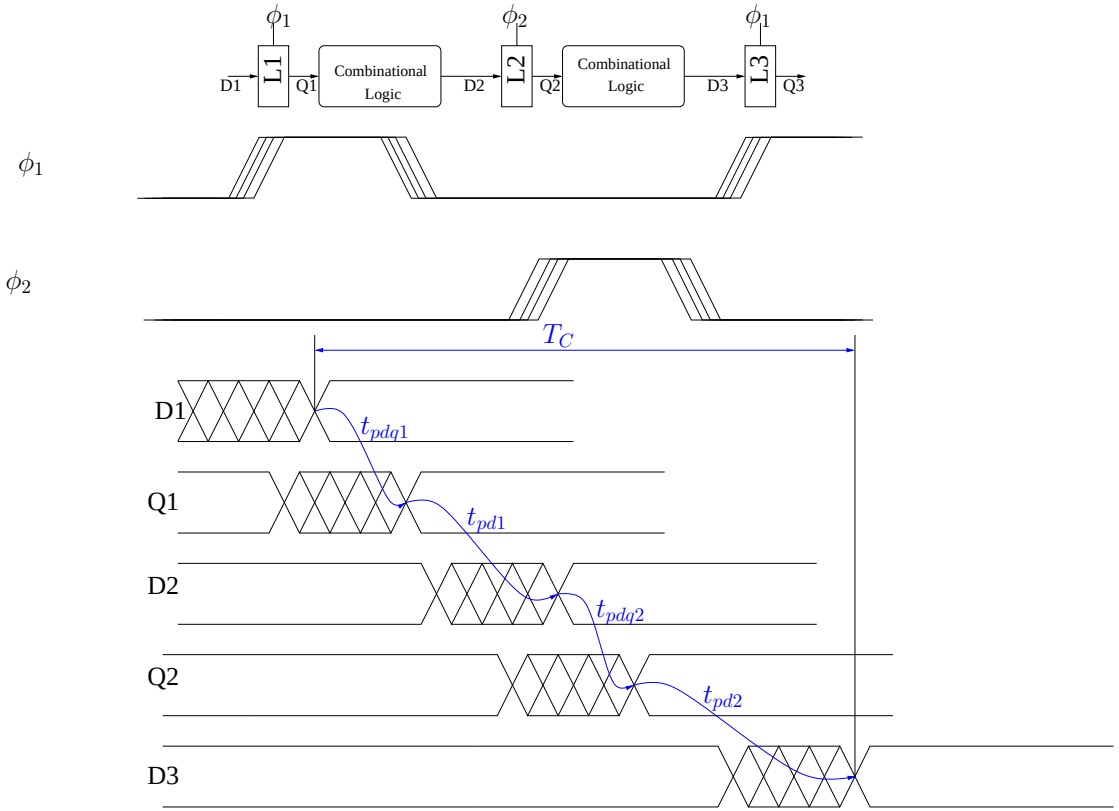
Min Delay Constraint with Skew - Flip Flop



$$t_{hold} \leq t_{cd} + t_{ccq} - t_{skew}$$

$$t_{cd} \geq t_{hold} - t_{ccq} + t_{skew}$$

Max Delay Constraint with Skew- Latch

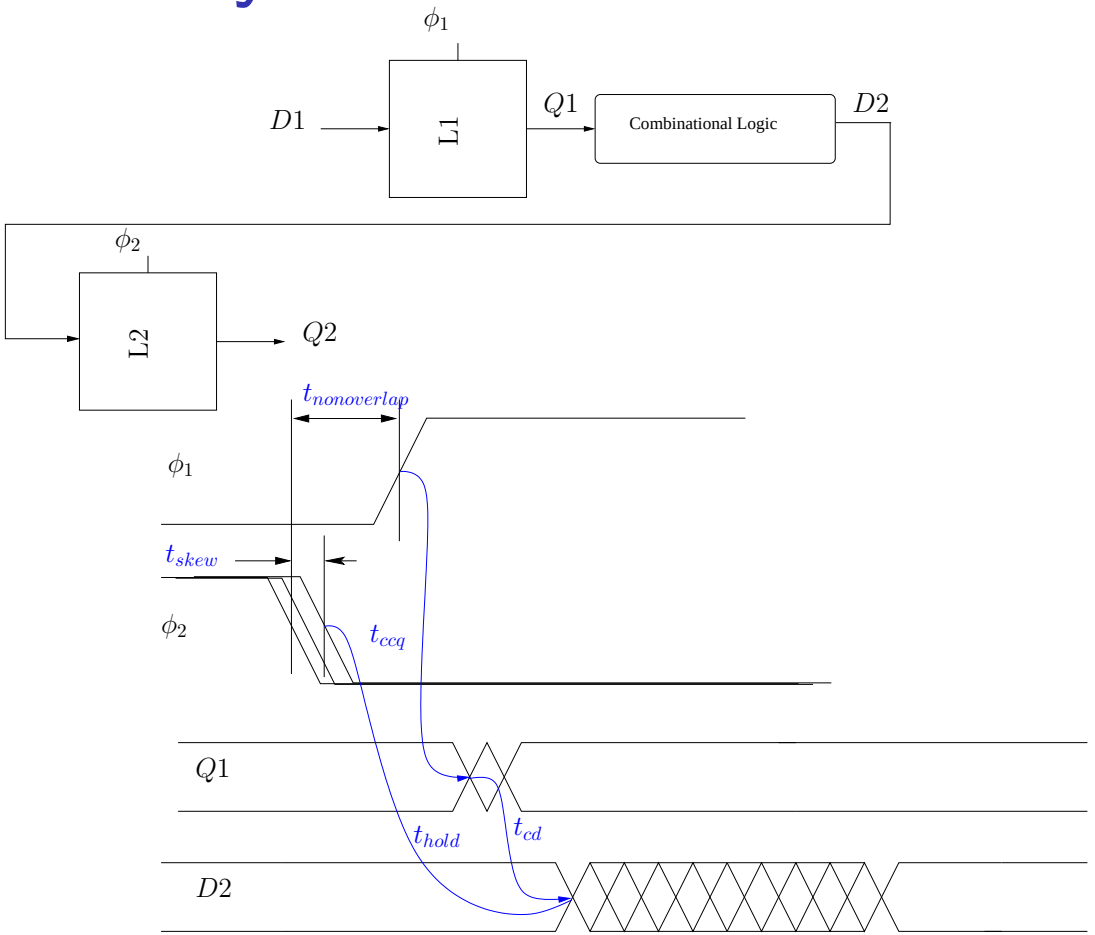


$$T_C \geq t_{pdq1} + t_{pd1} + t_{pdq2} + t_{pd2}$$

$$t_{pd} = t_{pd1} + t_{pd2} \leq T_C - (2t_{pdq})$$

Two phase latches are Skew Tolerant

Min Delay Constraint - Latch



$$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}$$

$$t_{borrow} \leq \frac{T_C}{2} - (t_{setup} + t_{nonoverlap} + t_{skew})$$

Sequence Element Timing Summary

Constraint	Flop	Two Phase Latch
Max	$t_{pd} \leq T_C - (t_{pcq} + t_{setup} + t_{skew})$	$t_{pd1} + t_{pd2} \leq T_C - (2t_{pdq})$ (Skew Tolerant)
Min	$t_{cd} \geq t_{hold} - t_{ccq} + t_{skew}$	$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap} + t_{skew}$
Borrow	N.A.	$t_{borrow} \leq \frac{T_C}{2} - (t_{setup} + t_{nonoverlap} + t_{skew})$

References

The material presented here is based on the following books/ lecture notes

1. Digital Integrated Circuits Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic 2nd Edition, Prentice Hall India
2. CMOS VLSI Design, Neil H.E. Weste, David Harris and Ayan Banerjee, 3rd Edition, Pearson Education