EE5311- Digital IC Design

Module 3 - The Inverter

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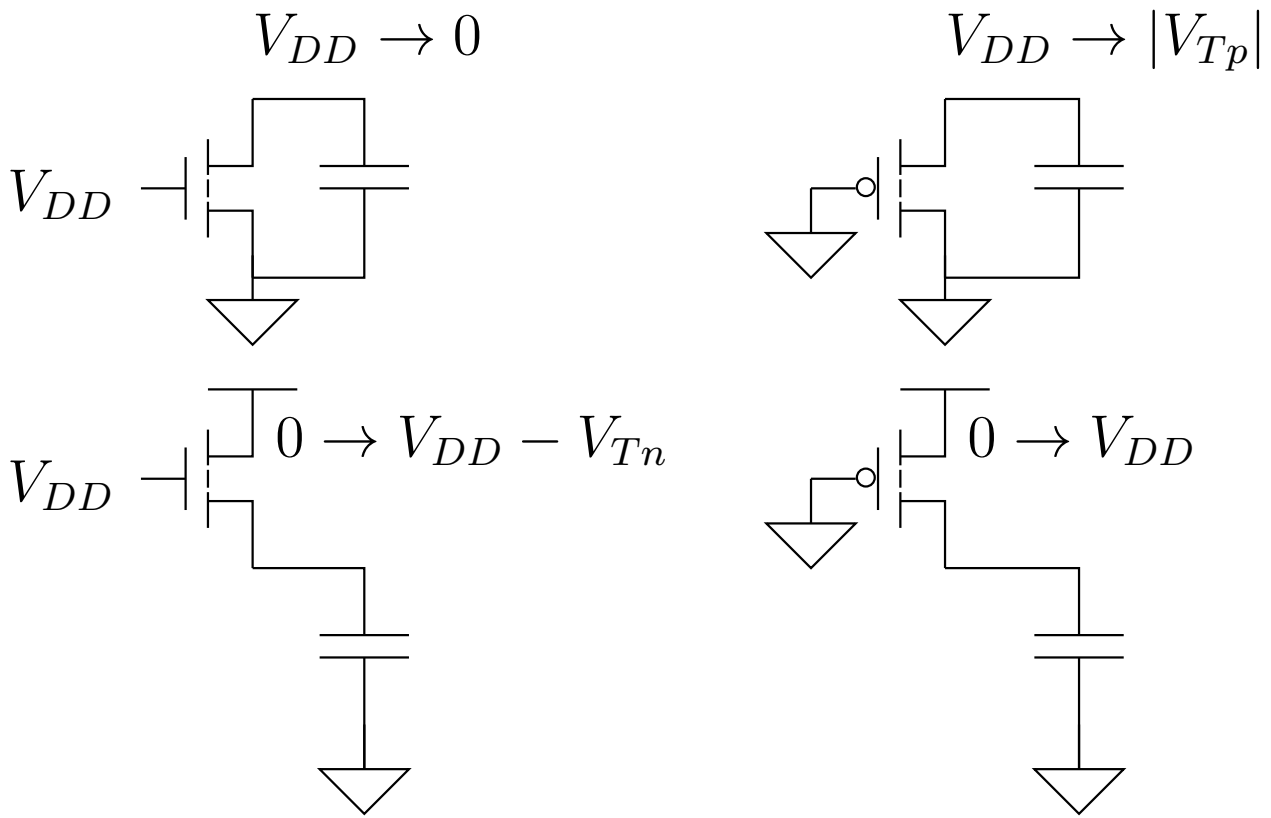
Learning Objectives

- Explain the functioning of a CMOS inverter
- Explain the Voltage Transfer Characteristics of an inverter
- Derive an expression for the trip point of an inverter
- Derive an expression for the delay of an inverter driving a load
- Derive expressions for Static, Dynamic and Short Circuit power of an inverter.

Outline

- Switch Model
- Transfer Characteristics
- Switching Threshold
- Noise Margin
- Supply Voltage Scaling
- Propagation Delay
- Power
  - Dynamic
  - Short circuit
  - Leakage

Inverters - Robust Configuration



- Pull down to *GND* with NMOS
- Pull up to V_{DD} with PMOS

Load Line

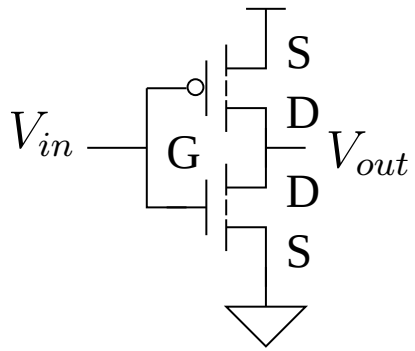


Figure: The CMOS Inverter

$$I_{DSp} = -I_{DSn}$$
$$V_{GSn} = V_{in}$$
$$V_{GSp} = V_{in} - V_{DD}$$
$$V_{DSn} = V_{out}$$
$$V_{DSp} = V_{out} - V_{DD}$$

Load Line

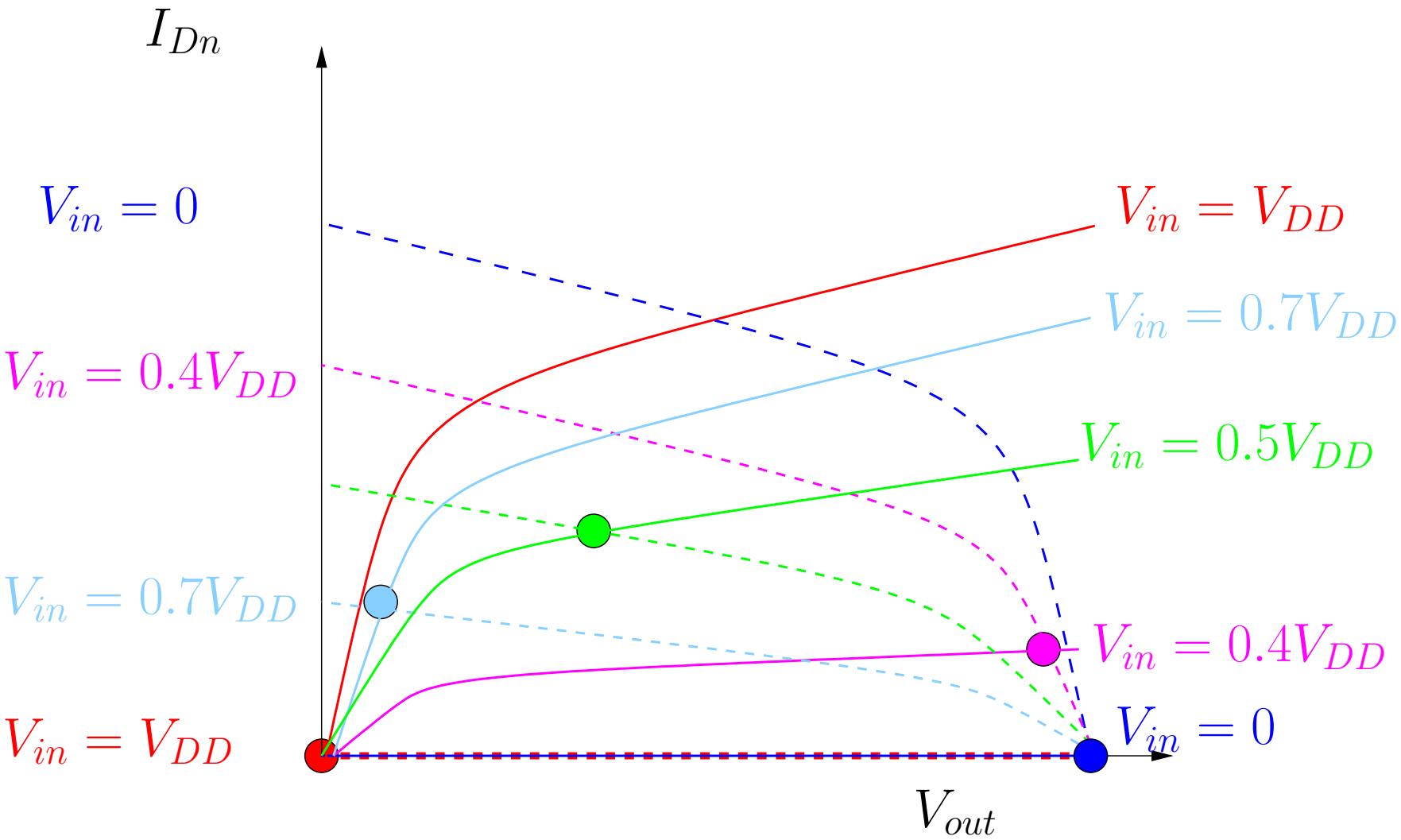


Figure: Solid lines- NMOS, Dashed lines - PMOS

Voltage Transfer Characterisitcs

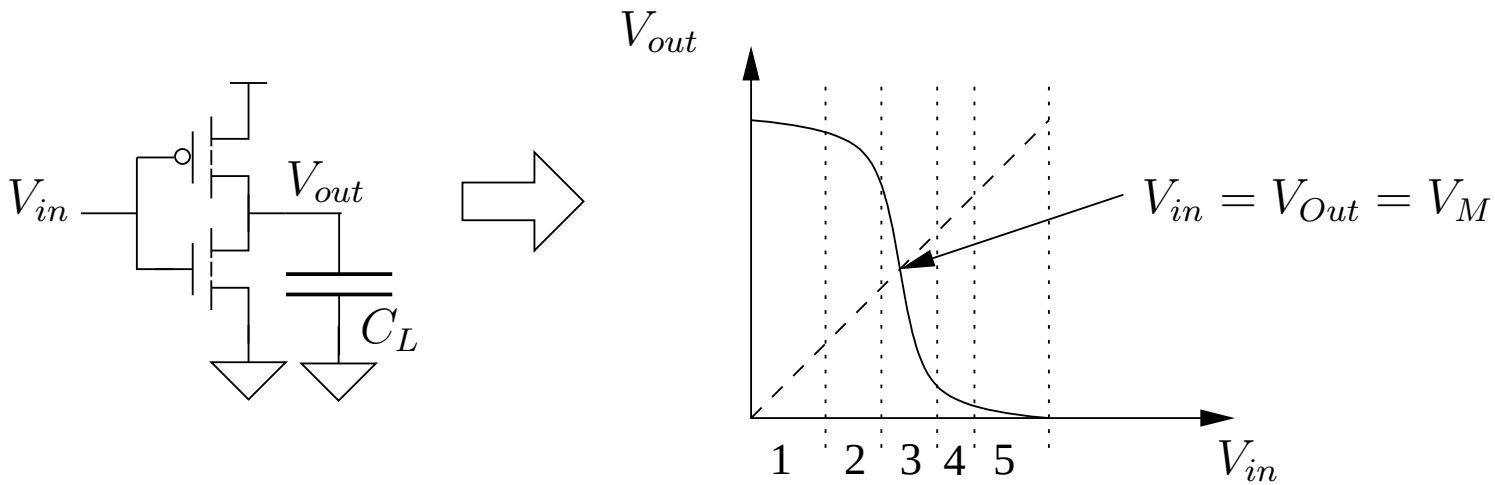


Figure: VTC of a CMOS Inverter

Region	NMOS	PMOS
1	Off	Lin
2	Sat	Lin
3	Sat	Sat
4	Lin	Sat
5	Lin	Off

Switching Threshold

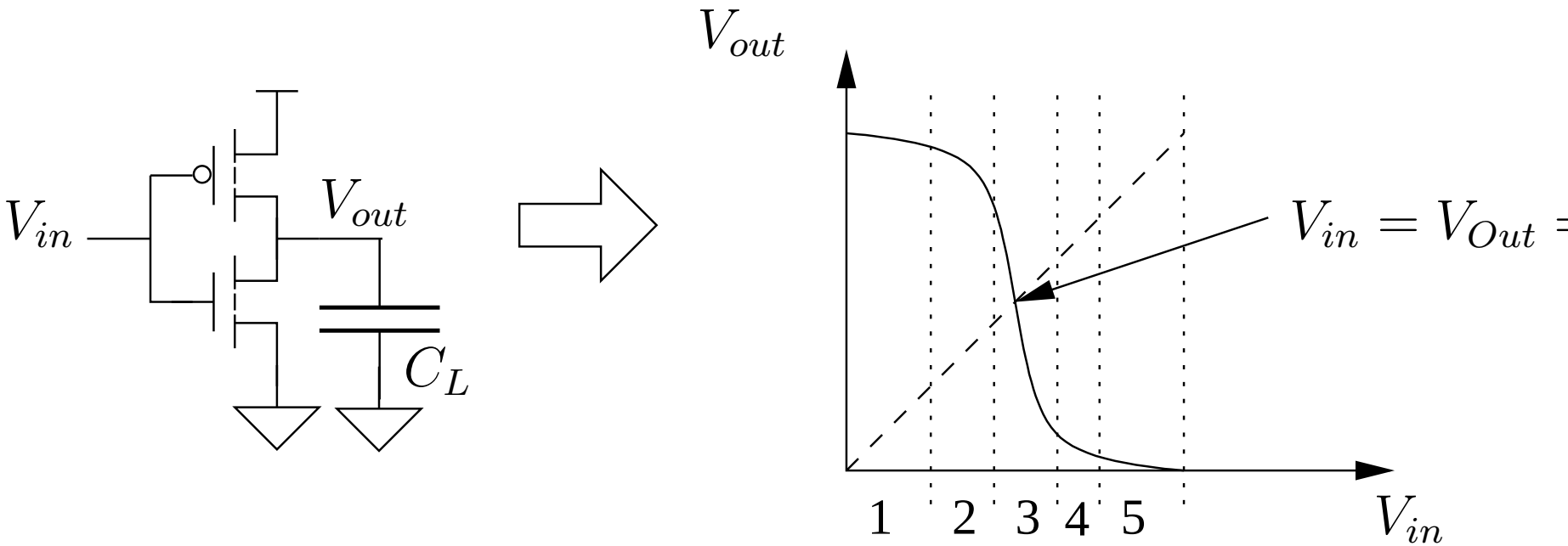


Figure: Switching Threshold

- Both NMOS and PMOS are in saturation
- Assume velocity saturation

Switching Threshold

$$I_{DSp} = -I_{DSn}$$
$$V_{GSn} = V_{in}$$
$$V_{GSp} = V_{in} - V_{DD}$$
$$V_{DSn} = V_{out}$$
$$V_{DSp} = V_{out} - V_{DD}$$
$$V_{in} = V_{out}$$

- Both NMOS and PMOS are in saturation
- Assume velocity saturation

Switching Threshold

Ignoring channel length modulation

$$I_{DSn} = k'_n \frac{W_n}{L}(V_M - V_{Tn} - \frac{V_{DSATn}}{2})V_{DSATn}$$

$$I_{DSp} = k'_p \frac{W_p}{L}(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2})V_{DSATp}$$

$$V_M = \frac{V_{Tn} + \frac{V_{DSATn}}{2} + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r}$$

$$r = \frac{k'_p(W_p/L)V_{DSATp}}{k'_n(W_n/L)V_{DSATn}} = \frac{W_p v_{satp}}{W_n v_{satn}}$$

$$V_M \approx \frac{r}{r+1} V_{DD}$$

Switing Threshold

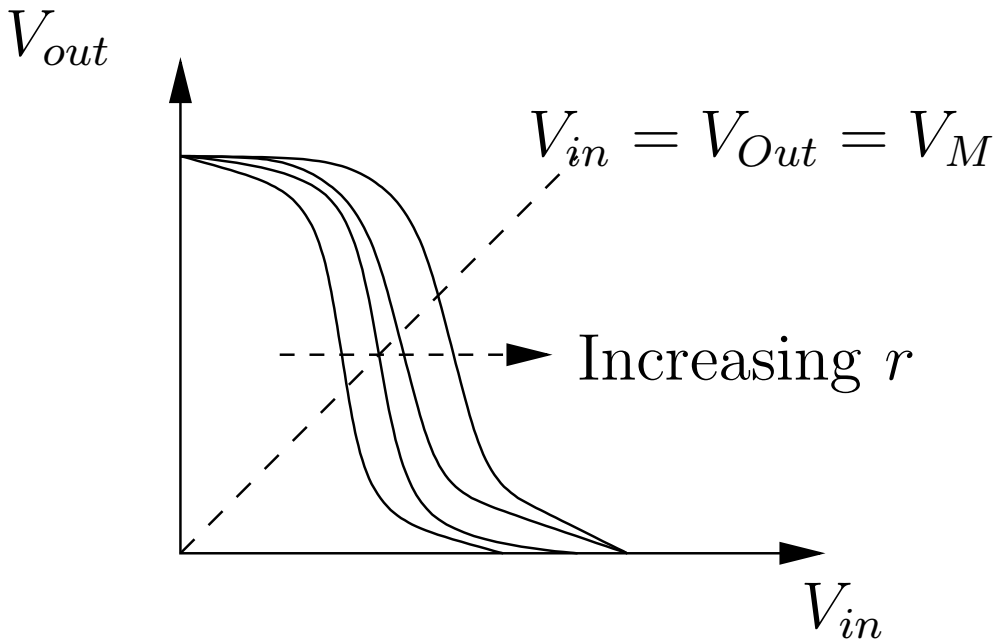


Figure: VTC Trip Point

Ratio of $\frac{W_p}{W_n}$ determines V_M

Switing Threshold Without Velocity Saturation

$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1 + r}$$

$$r = \sqrt{\frac{-k_p}{k_n}}$$

Left as an exercise

Noise Margin

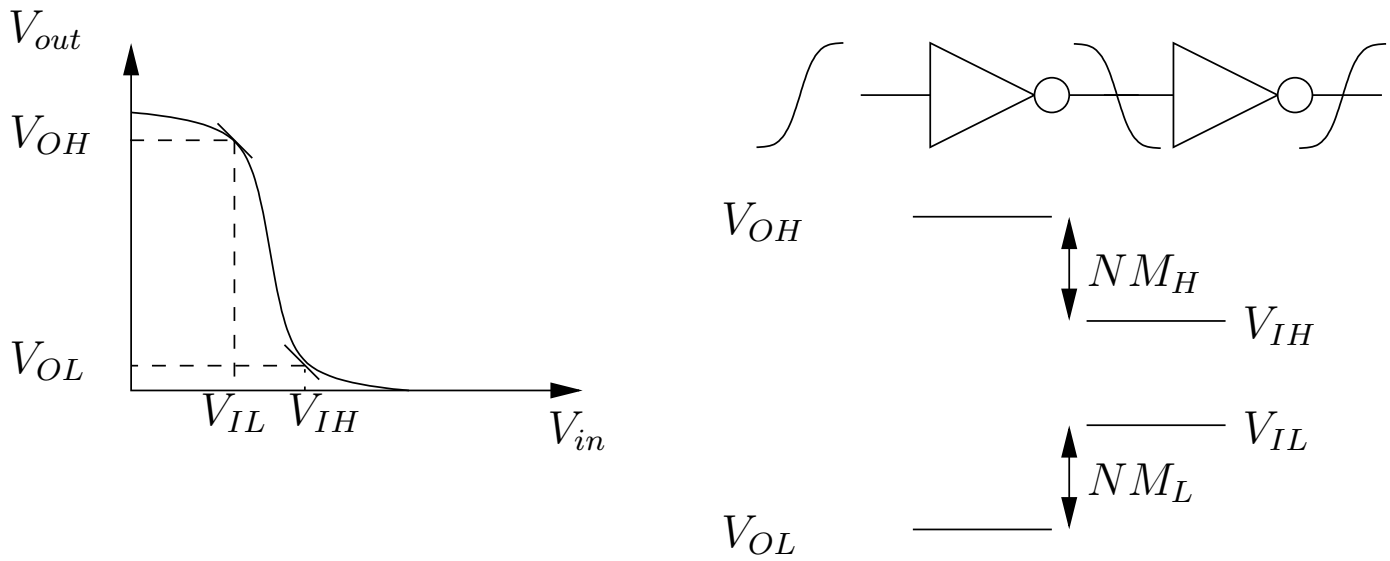


Figure: Noise Margin of a CMOS Inverter

- Logic levels from the driver should be recognized by the load
- Points of slope -1 provide the noise margin levels

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Noise Margin Approximation

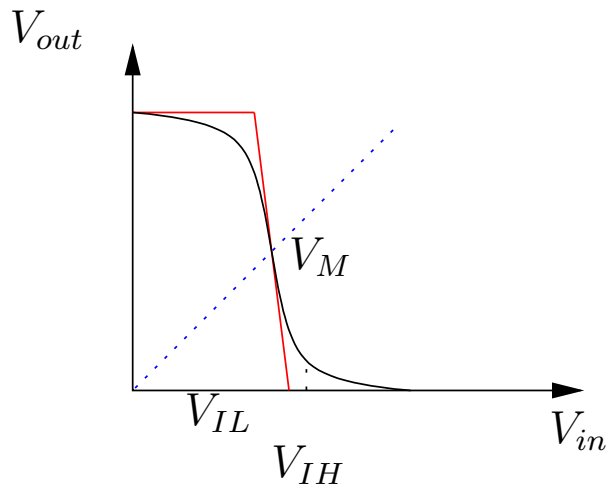


Figure: Noise Margin approximation of a CMOS Inverter

- Extend the tangent at V_M
- Slope is the gain (g) of the VTC

$$NM_H = V_{DD} - V_{IH} = V_{DD} - V_M + \frac{V_M}{g}$$

$$NM_L = V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

Noise Margin Calculations

- Need to consider channel length modulation
- Slope is the gain ($g = \frac{dV_{out}}{dV_{in}}$) of the VTC

$$I_{DSn} = I_{DSn}^{no-clm}(1 + \lambda_n V_{out})$$

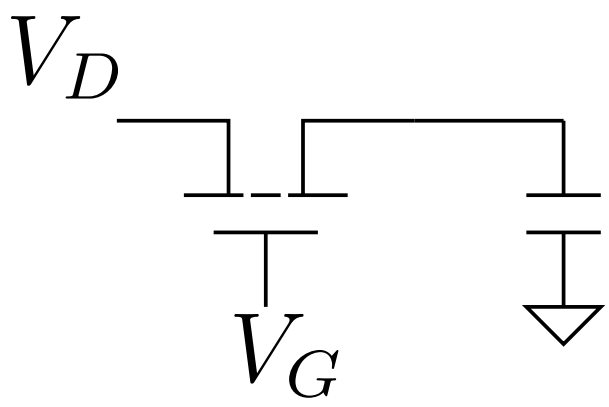
$$I_{DSp} = I_{DSp}^{no-clm}(1 + \lambda_p(V_{out} - V_{DD}))$$

$$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p}$$

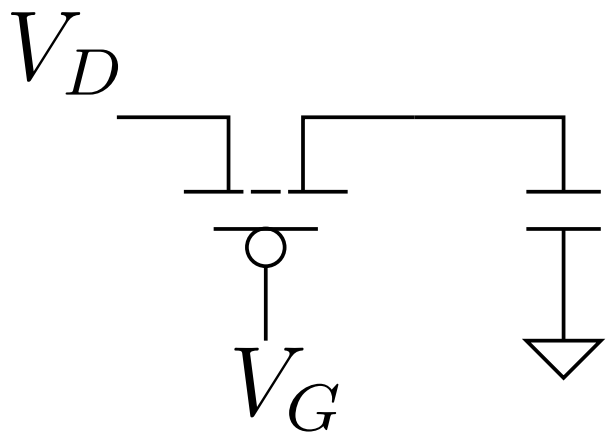
$$g \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

Pass Transistors



$$v_C(0^-) = 0$$



$$v_C(0^-) = V_{DD}$$

$$v_C(t) = min(V_G - V_{Tn}, V_D)$$
$$v_C(t) = max(V_G - V_{Tp}, V_D)$$

Switch Model

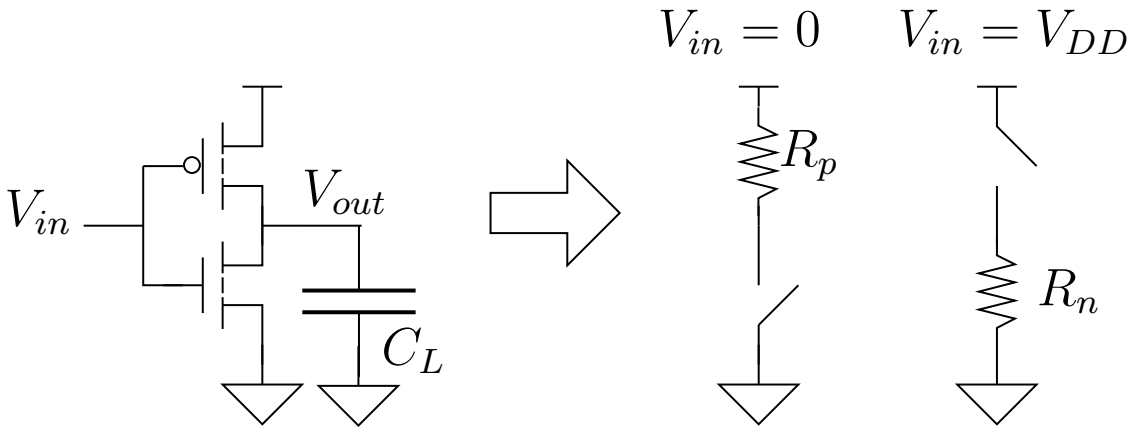


Figure: The CMOS Inverter

- The high and low logic levels are V_{DD} and $GND(0)$
- Logic levels are independent of sizes - Ratioless Logic
- Low output impedance ($k\Omega$) - Immune to noise
- Large input impedance - Infinite fanout
- No conduction path from supply to ground in steady state

Switch Model Dynamic Behaviour

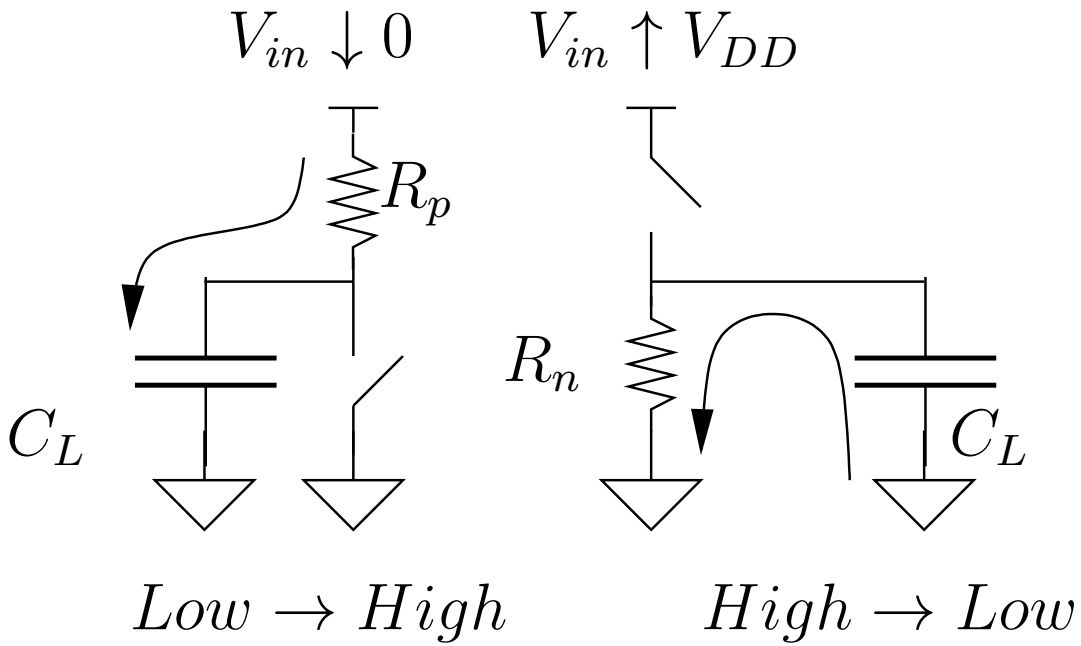


Figure: Dynamic Behaviour of CMOS Inverter

$$\tau_{rise} = R_p C_L$$
$$\tau_{fall} = R_n C_L$$

Delay

- Propagation Delay - 50% input to 50% output
  - Rise delay. Output goes from $L \uparrow H$ - t_{pLH}
  - Fall delay . Output goes from $H \downarrow L$ - t_{pHL}
  - Propagation delay is defined as $t_p = \frac{t_{pHL}+t_{pLH}}{2}$
- Slew
  - Rise time - Time taken for output to go from 10% to 90%
  - Fall time - TIme taken for output to go from 90% to 10%

Delay

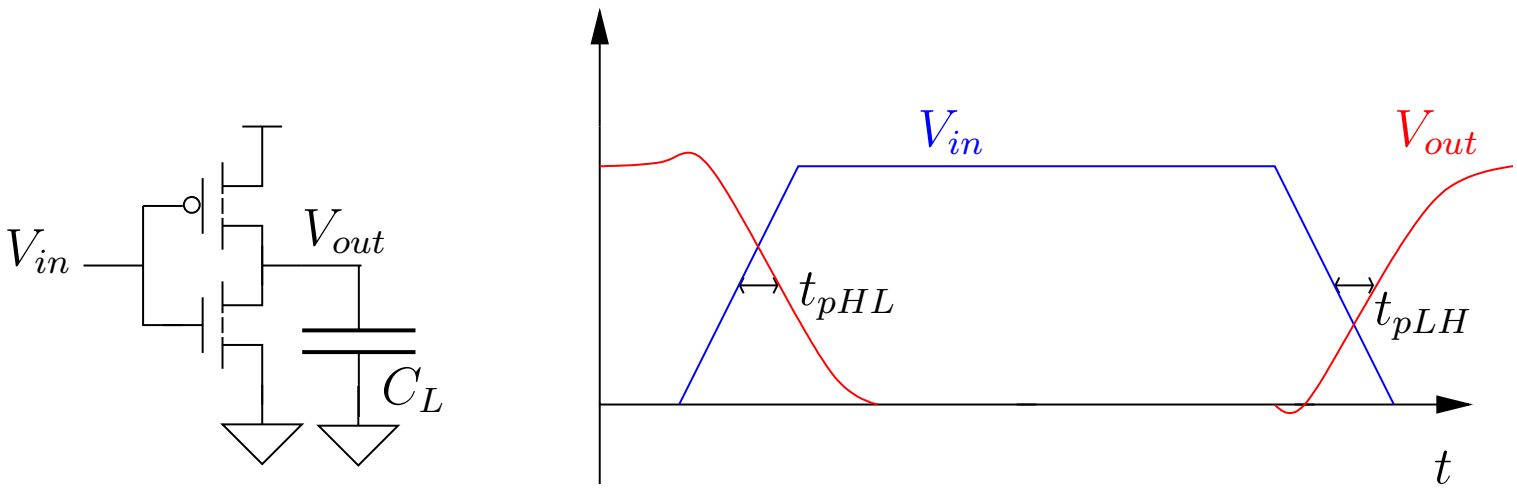


Figure: Delay

$$t_{pHL} = R_{eqn} C_L$$

$$t_{pLH} = R_{eqp} C_L$$

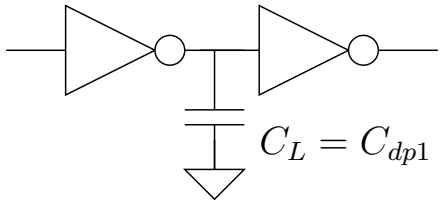
$$t_p = C_L \frac{R_{eqn} + R_{eqp}}{2}$$

Transistor Sizing - Symmetric delay

- Rising propagation delay should be identical to falling propagation delay.
- This also ensures a symmeteric VTC

$$t_{pHL} = t_{pLH}$$
$$R_{eqn} = R_{eqp}$$
$$\frac{C_L V_{DD}}{2 I_{DSATn}} = \frac{C_L V_{DD}}{2 I_{DSATp}}$$
$$W_n \mu_n = W_p \mu_p$$
$$W_p \approx 2 W_n$$

Transistor Sizing - Minimum delay



$$t_p = C_L \frac{R_{eqn} + R_{eqp}}{2}$$

$$t_p = (0.5)[(1+\beta)(C_{gn2} + C_{dn1}) + C_{wire}]R_{eqn}(1 + \frac{\alpha}{\beta})$$

$$\alpha = \frac{R_{eqp}}{R_{eqn}} @ W_p = W_n; \beta = \frac{W_p}{W_n}$$

$$\frac{\partial t_p}{\partial \beta} = 0$$

$$\beta_{opt} = \sqrt{\alpha \left(1 + \frac{C_{wire}}{C_{dn1} + C_{gn2}}\right)}$$

Power Dissipation

Energy lost as heat disspation in the devices

- Dynamic - Charge/ Discharging of cpacitance
- Short Circuit - Conductive path from $V_{DD} \rightarrow GND$
- Static - Leakage even when no activity happens

Dynamic Power

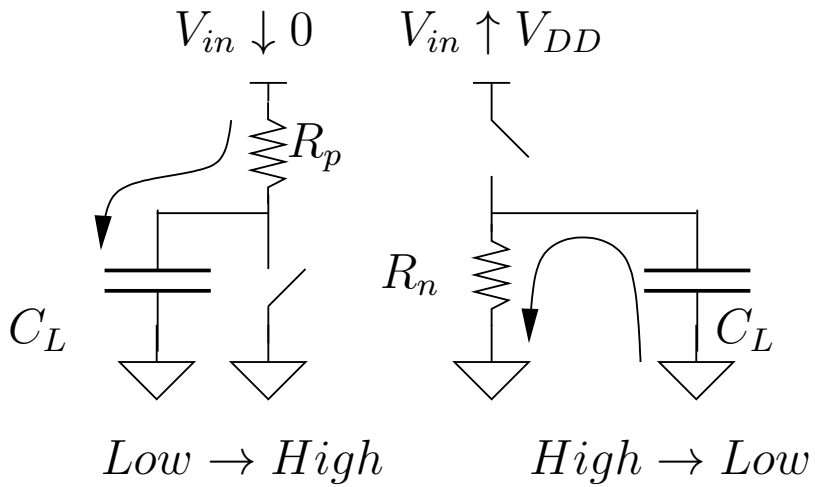


Figure: Capacitor charge and discharge

$$L \uparrow H$$

$$E_{VDD} = \int_0^\infty i_{VDD}(t) V_{DD} dt$$

$$E_C = \int_0^\infty i_{VDD}(t) V_{out} dt$$

Dynamic Power

$$L \uparrow H$$

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t) V_{DD} dt$$

$$E_{VDD} = \int_0^{\infty} C_L \frac{dv_{out}}{dt} V_{DD} dt$$

$$E_{VDD} = \int_0^{V_{DD}} C_L V_{DD} dv_{out}$$

$$E_{VDD} = C_L V_{DD}^2$$

$$E_C = \frac{C_L V_{DD}^2}{2}$$

Dynamic Power

- $L \uparrow H$ - Load capacitor charges and disspates $\frac{C_L V_{DD}^2}{2}$ in PMOS
- $H \downarrow L$ - Load capacitor discharges and disspates $\frac{C_L V_{DD}^2}{2}$ in NMOS
- Note that the energy dissipated is independent of size
- Depends on
  - Probability of switching ($P_{0\rightarrow 1}$) - Activity factor
  - Frequency of operation (f)

$$P_{dyn} = C_L V_{DD}^2 f_{0\rightarrow 1}$$
$$P_{dyn} = C_L V_{DD}^2 P_{0\rightarrow 1} f$$

Short Circuit Power

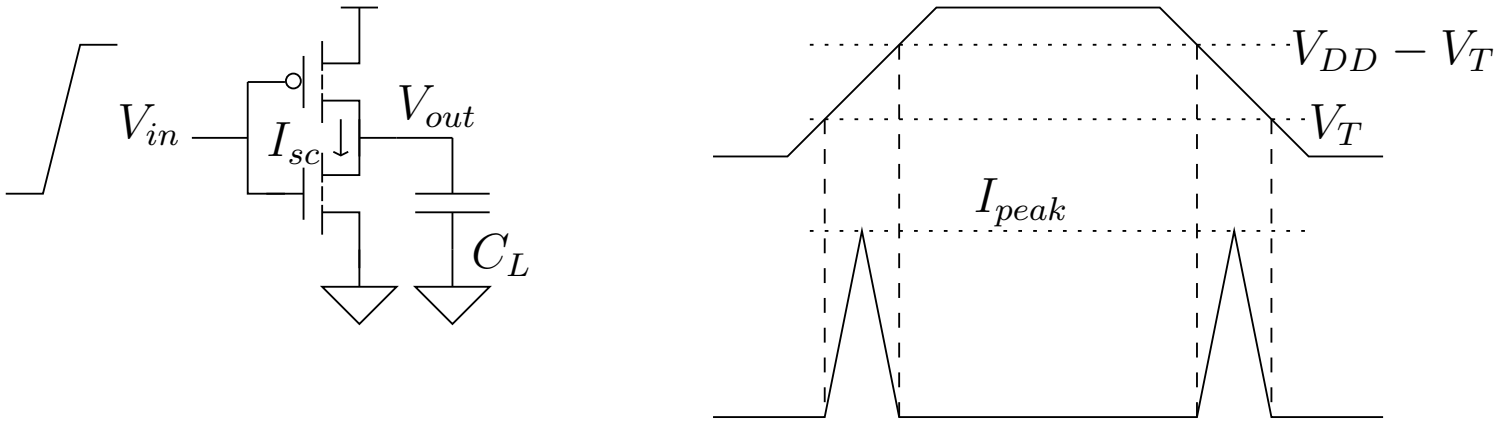


Figure: Both NMOS and PMOS conduct

$$E_{sc} = V_{DD}\frac{I_{peak}\,t_{sc}}{2} + V_{DD}\frac{I_{Peak}\,t_{sc}}{2}$$

$$P_{sc} = t_{sc}\,V_{DD}\,I_{peak}\,f$$

$$t_{sc} = \frac{V_{DD} + V_{Tp} - V_{Tn}}{V_{DD}}\,t_s$$

Static Power

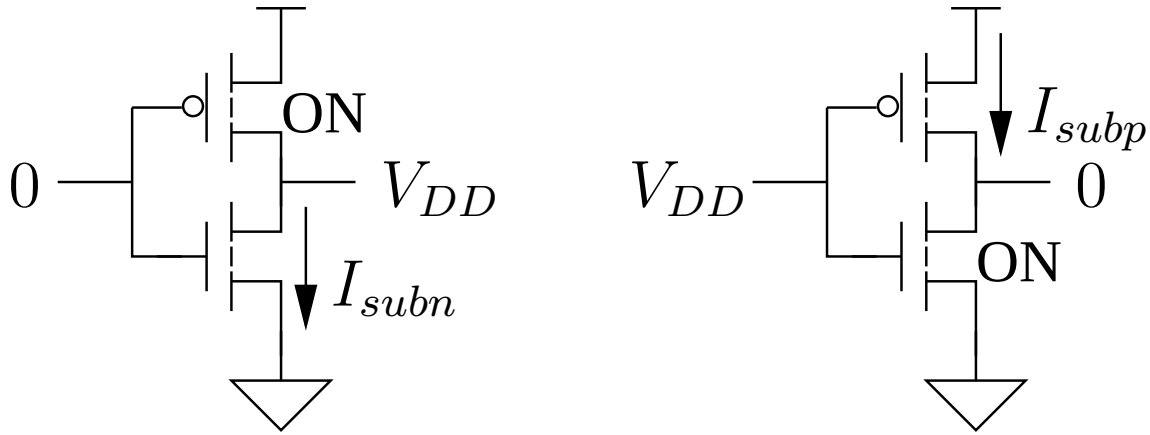


Figure: NMOS or PMOS leaks current

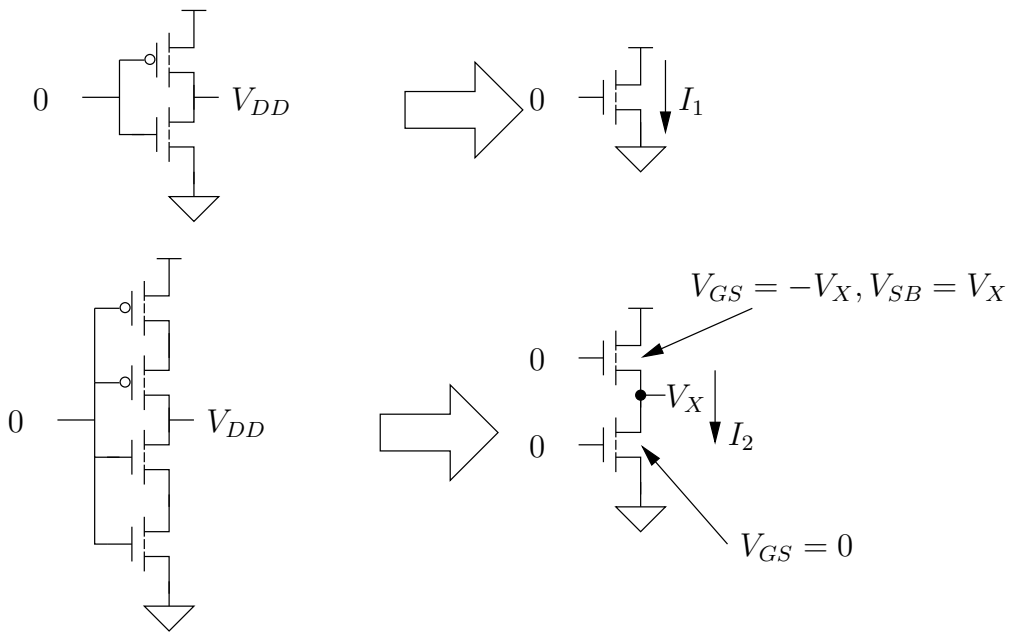
$$P_{stat} = I_{stat} V_{DD}$$

$$P_{tot} = P_{dyn} + P_{sc} + P_{stat}$$

$$P_{tot} = (C_L V_{DD}^2 + V_{DD} I_{peak} t_s) f_{0\to1} + V_{DD} I_{leak}$$

Stacking Effect

- The intermedaite node : $0 < V_X < V_{DD}$
- Exponentially reduces the leakage of the series stack ($I_2 << I_1$)
- Increase in V_{TH} of the top transistor due to body effect



$$I_{TOP} \propto e^{(-V_X - V_{Tn})/n\phi_t}$$

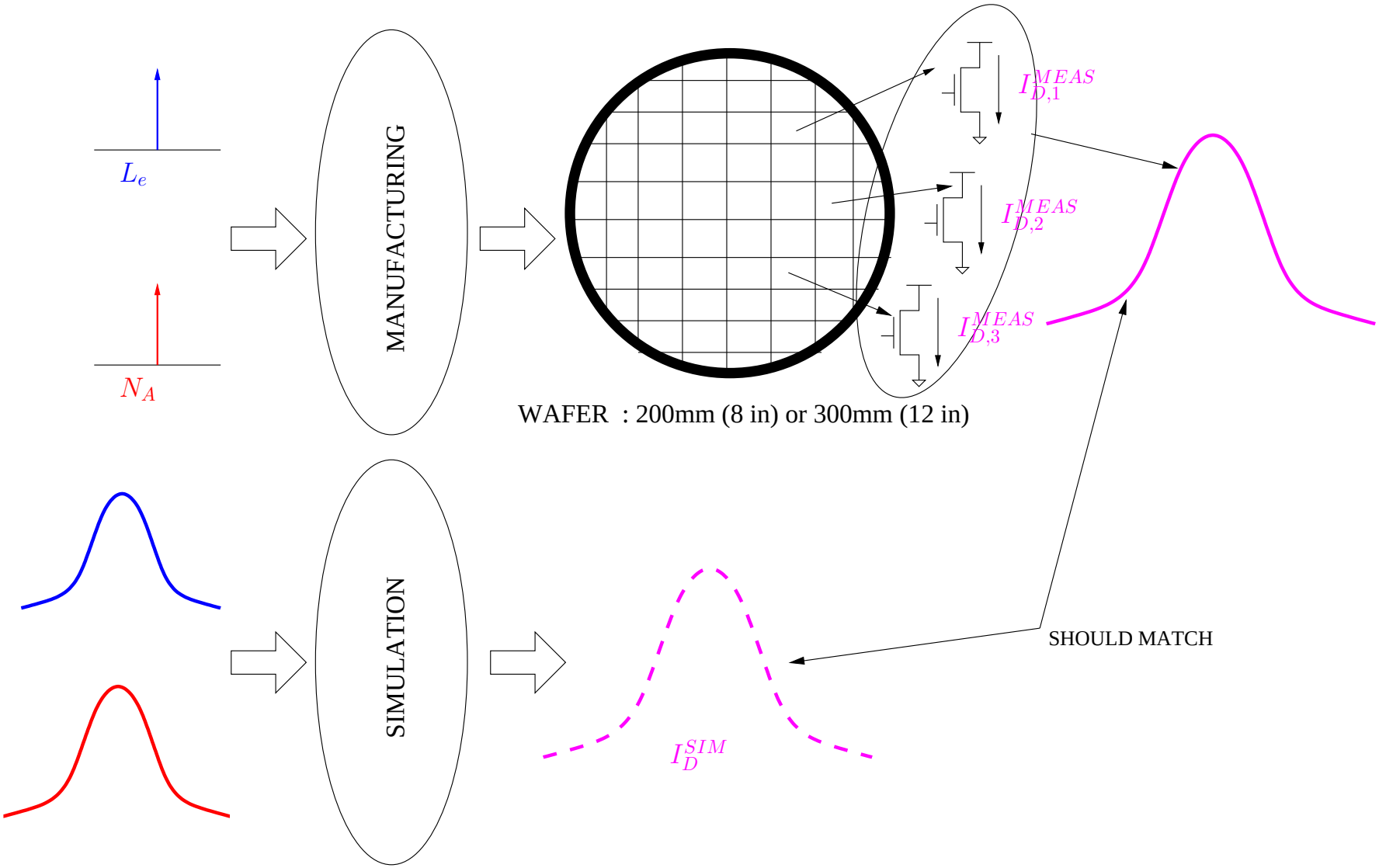
$$I_{BOT} \propto e^{(-V_{Tn})/n\phi_t}$$

$$I_{BOT} = I_{TOP}$$

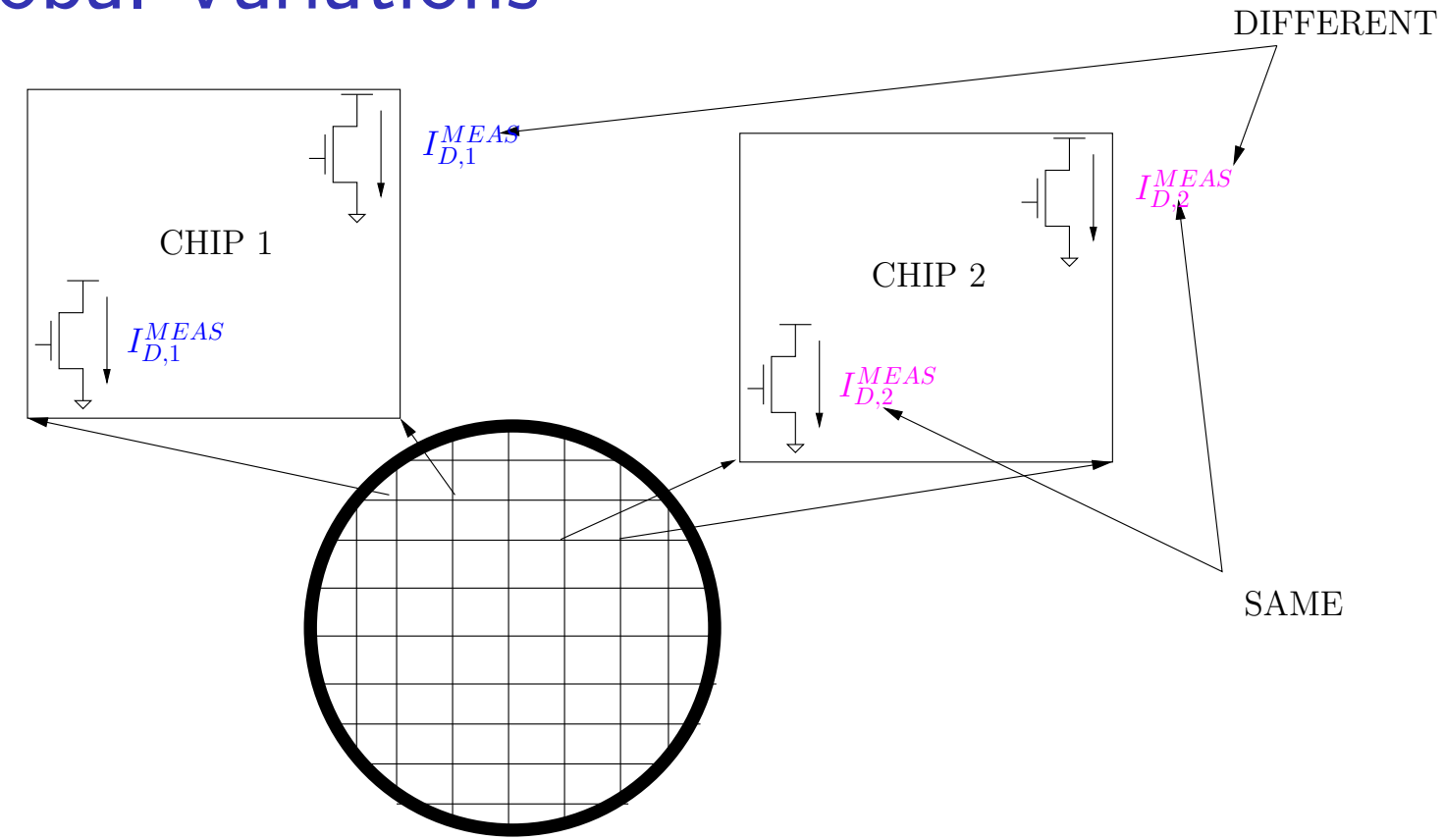
Process Variations

- Impossible to manufacture tiny dimensions accurately
- Variations are not avoidable
- Process Parameters : T_{OX}, N_A, L_e x_j, μ_n, μ_p see variations
- Performance Parameters: Currents and Voltages
- Process variation information (μ, σ) are provided to designers
- Performance parameter variation in simulation should match measured variations

Process Variations

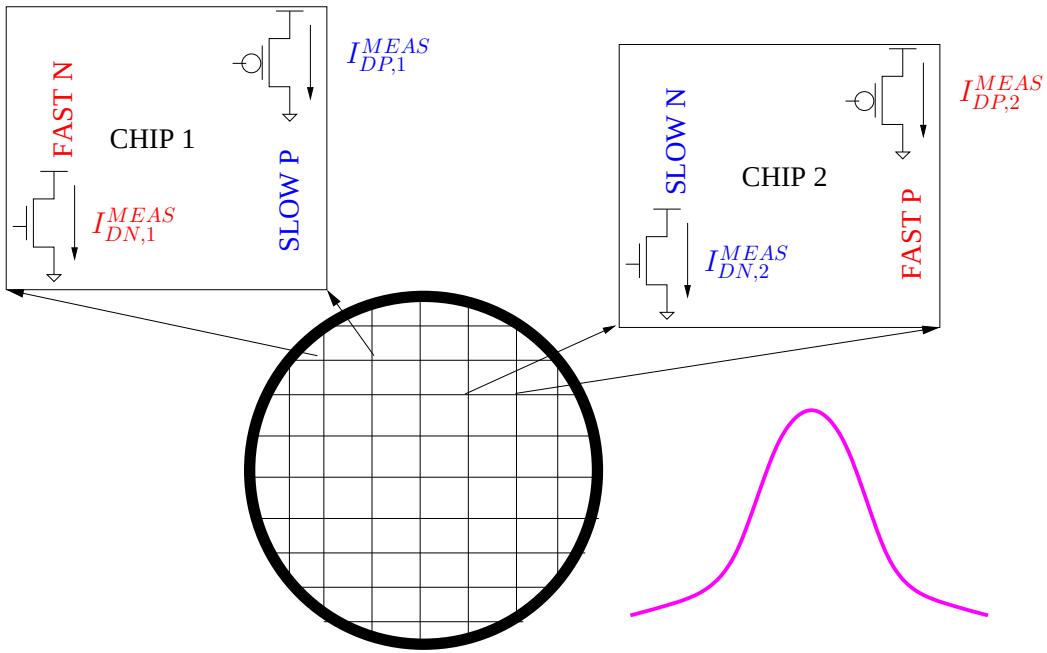


Global Variations



- All transistors within a chip affected in the same way
- Transistors in different chips across the wafer affected differently

Global Variations



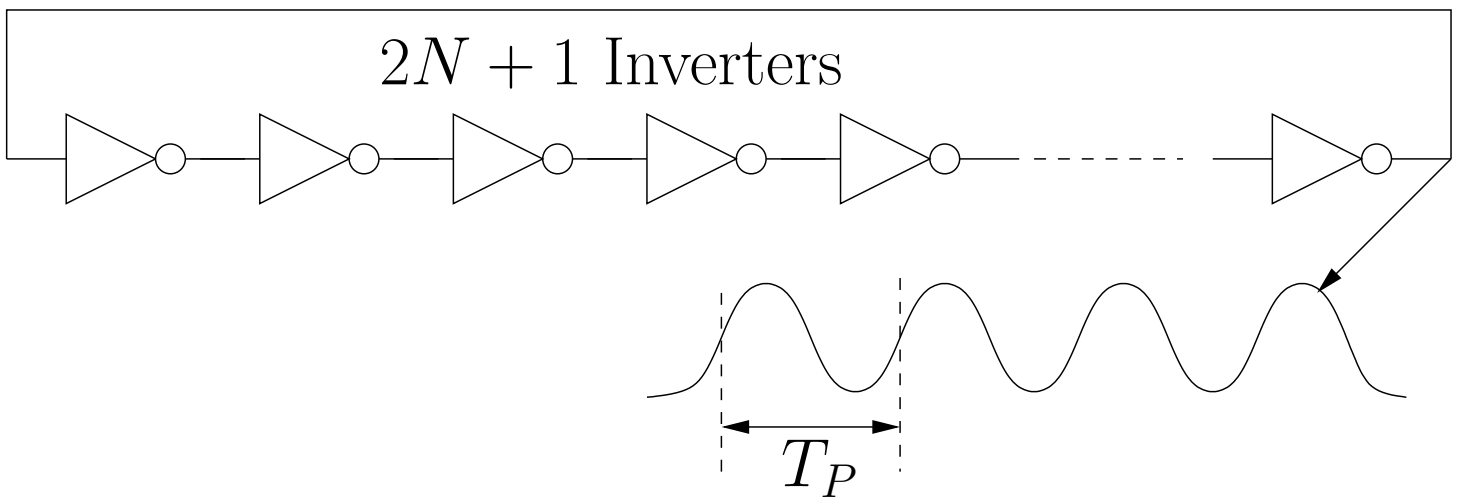
- Manufacturing process of (N and P)MOS are different
- Transistors end up being Fast (F), Slow (S) or Typical (T)
- All N can get biased in one direction
- All P can get biased in another
- Corner simulation (N,P) : (TT, FS, FF, SF, SS)

Local Variations

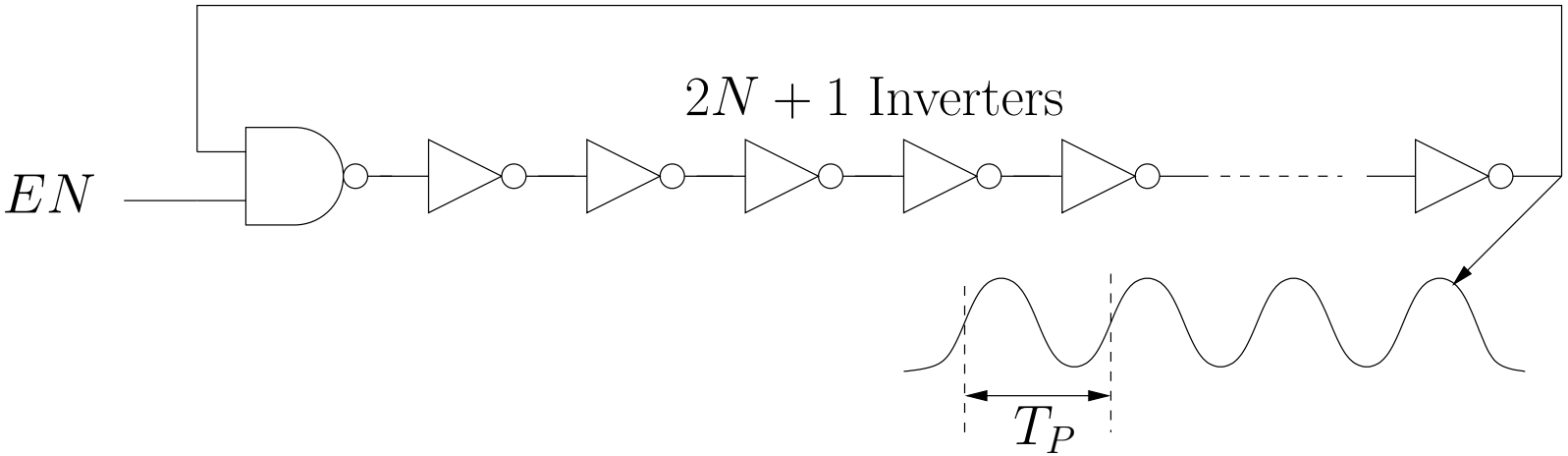
- Transistors sitting right next to each other will be different
- Happens mainly due to Random Dopant Fluctuation
- Large transistors are affect lesser than small ones ($\sigma_{Local} \propto \frac{1}{\sqrt{LW}}$)
- Requires large number of statistical simulations to ensure correct functionality

Ring Oscillators

- Excellent process monitors
- Good representative of all digital circuits
- Can be added by the FAB in Kerf regions or by designers in their chip
- Measure the frequency of oscilations to determine the global process corner
- Can be added in multiple corners of a large chip to measure any across chip variation



Ring Oscillators



$$T_P \approx 2x(2N+1)\tau_{inv}$$

- $EN = 0$ prevents any oscillations - Saves dynamic power
- Usually a couple of 100 INV long
- Very high frequency of oscillations
- Divided several times before being brought out of the chip

References

The material presented here is based on the following books/ lecture notes

1. Digital Integrated Circuits Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic 2nd Edition, Prentice Hall India