EE5311- Digital IC Design

Module 2 - Interconnects

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Learning Objectives

- Estiamte the wire parasitics given the sheet resistance and the capacitance per unit length
- Derive the Elmore delay for a given RC tree
- Estimate the wire RC delay by applying the Elmore delay model to a distributed RC network

Outline

- Capacitance
- Resistance
  - Sheet Resistance
  - Skin depth
- Resistance Models
- Lumped model (C and RC)
- Propagating delay and rise time
- Elmore delay model
- Example - Time constant of a rc-wire model

Capacitance

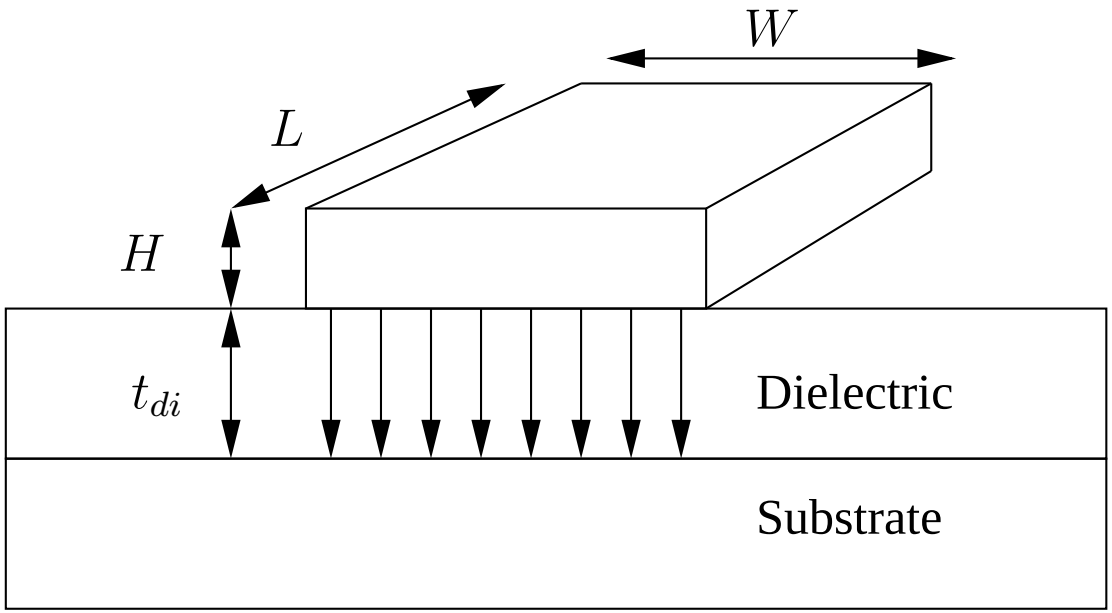


Figure: Wire capacitance

$$C_{int} = \frac{\epsilon_{di}}{t_{di}} WL$$

Capacitance

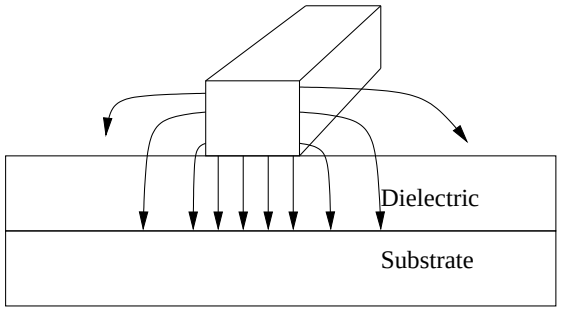


Figure: Thin wire capacitance

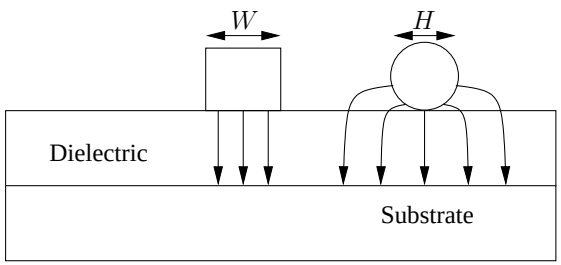


Figure: Thin wire capacitance model

$$c_{wire} = \frac{\epsilon_{di}}{t_{di}} W + \frac{2\pi\epsilon_{di}}{log(t_{di}/H)}$$

Resistance

$$R = \frac{\rho L}{HW}$$
$$R = R_{\square}\frac{L}{W}$$
$$R_{\square} = \frac{\rho}{H}$$

- $R_{\square}$ - Sheet resistance ($\Omega/\square$) - Technology Parameter
- To obtain resistance of a wire just multiply with L/W

Skin Effect

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

- At high frequencies current tends to flow only in the outer surface confined to a depth of δ
- Area of current flow is $\approx 2(H + W)\delta$

$$r(f) = \frac{\sqrt{\pi \rho f \mu}}{2(H + W)}$$

Lumped Model

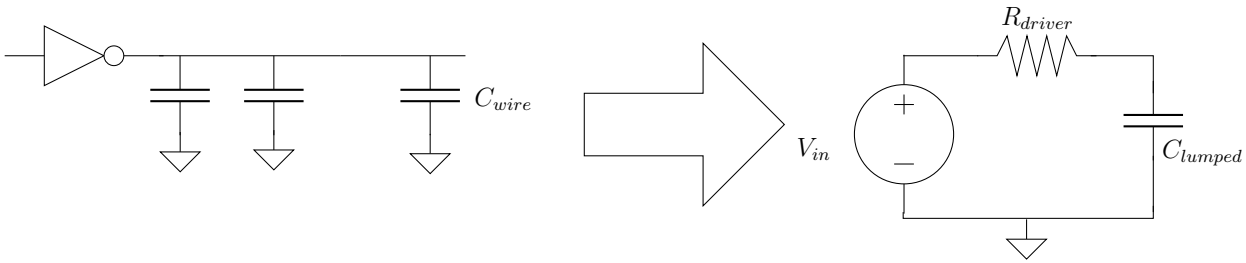


Figure: Lumped Capacitance model

$$C_{lumped} = L \times c_{wire}$$

Lumped RC Model

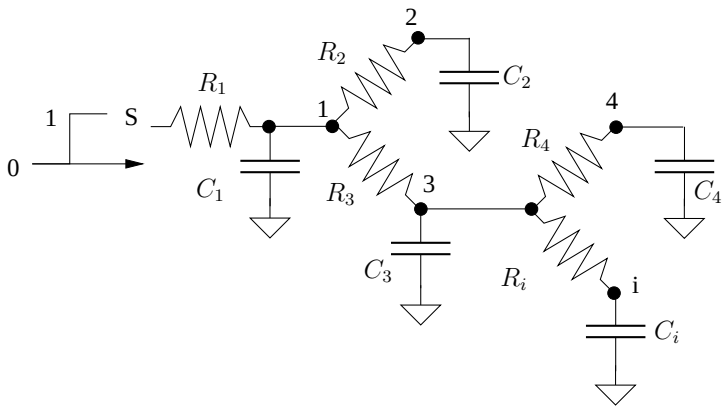


Figure: Lumped RC model

Assumptions:

- The network has a single input node
- All capacitors are between the node and ground
- The network does not contain any resistive loops (tree)

Lumped RC Model

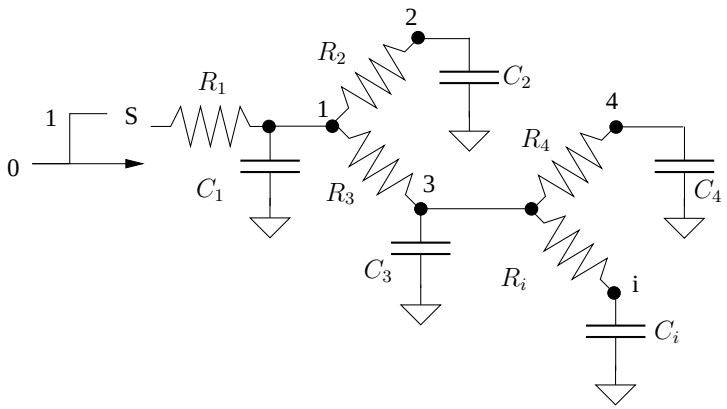


Figure: Lumped RC model

- Path resistance (R_{ii}) is the net resistance from the source node to node i ($R_{44} = R_1 + R_2 + R_4$)
- Shared path resistance: Sum of resistance shared between two paths
  $R_{ik} = \sum R_j : [R_j \in (path(s \rightarrow i) \cap path(s \rightarrow k))]$

Elmore Delay Model

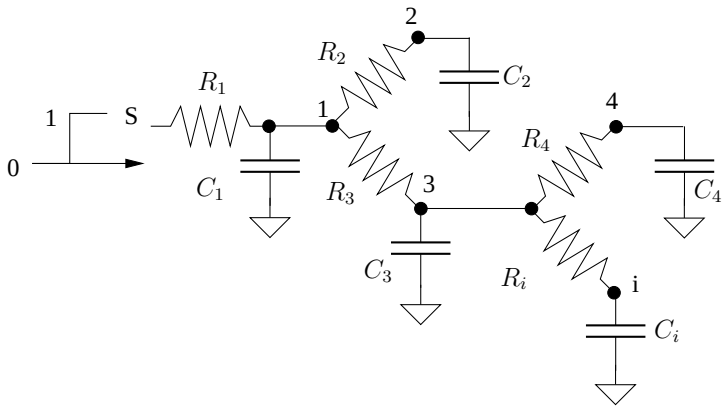


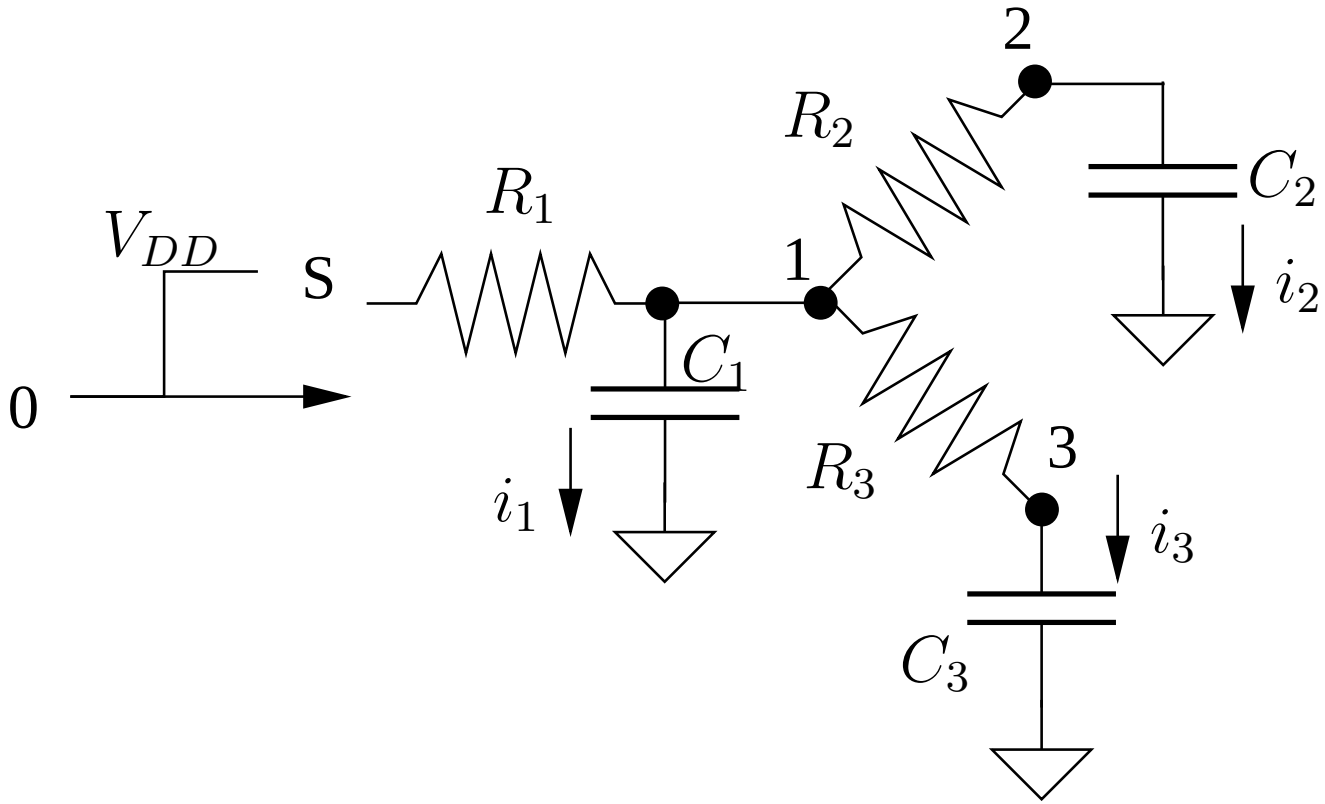
Figure: Elmore delay

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Delay is affected by:

- All capacitances ($C_k : k \in 1, 2 \ldots N$) - Loading
- Path resistances

Elmore Delay Model Example



Assumption

- Input is an ideal step function.
- All capacitances charge up to V_{DD} as $V_k \approx V_{DD}(1 - e^{-t/\tau_k})$ - Second order effects are negligible

Elmore Delay Model Example

$$V_{in} - V_3 = (i_1 + i_2 + i_3)R_1 + i_3 R_3$$

$$i_k = C_k \frac{dV_k}{dt}$$

$$\int_0^{\infty} (V_{in} - V_3)dt = \int_0^{V_{DD}} R_1(C_1 dV_1 + C_2 dV_2 + C_3 dV_3) + R_3 C_3 dV_3$$

Substituting $V_3 \approx V_{DD}(1 - e^{-t/\tau_3})$ and integrating we get

$$\tau_3 = C_1 R_1 + C_2 R_1 + C_3(R_1 + R_3)$$

Clearly shows that off path resistances don't affect delay (to a first order) but all capacitances do

Elmore Delay Model

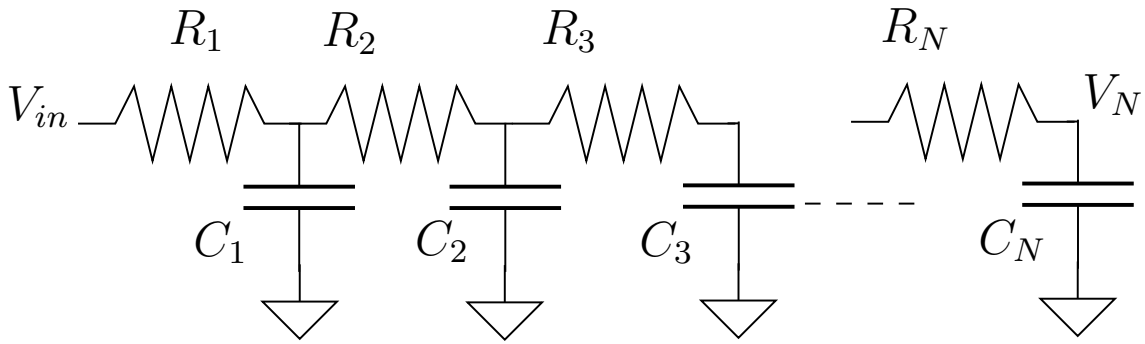


Figure: RC Ladder

Delay is the **first order** time constant of the transfer function

$$\frac{V_N(s)}{V_{in}(s)} = \frac{H(s)}{G(s)}$$

General expression for the delay of an RC-ladder is

$$\tau_{DN} = \sum_{k=1}^{N} C_k \sum_{i=1}^{k} R_i$$

Delay of RC wire model

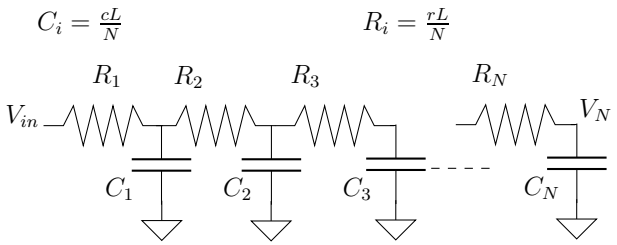


Figure: RC wire delay model.

Delay of an RC-wire model is

$$\tau_{DN} = (\frac{L}{N})^2(rc+2rc+\ldots+Nrc) = (rcL)^2\frac{N+1}{2N} \approx \frac{rcL^2}{2} = \frac{RC}{2}$$

- r = resistance per unit length (Ω/m)
- c = capacitance per unit length (F/m)
- Delay of a wire is a quadratic function of its length
- The delay of the distributed rc line is half that of the lumped RC model

Design Thumb Rules

rc delay should be considered only when

- wire delay is larger or comparable to the gate delays ($L_{crit} = \sqrt{\frac{2t_{pgate}}{rc}}$)
- rise/ fall delay at the source is smaller than rise/ fall time of the line ($t_{rise} < rcL^2$)

When the wire delay is comparable to the total delay, consider RC models. Else lumped C model will do

Example

Material	$R_{\square}(\Omega/\square)$	$c(aF/\mu m)$
Poly	150	196
Al	0.075	110

Calculate the propagation delay of 10cm long, $1\mu m$ wide Al wire. Comapre the delay with that of a Polysilicon wire.

References

The material presented here is based on the following books/ lecture notes

1. Digital Integrated Circuits Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic 2nd Edition, Prentice Hall India