EE5311- Digital IC Design

Module 1 - The Transistor

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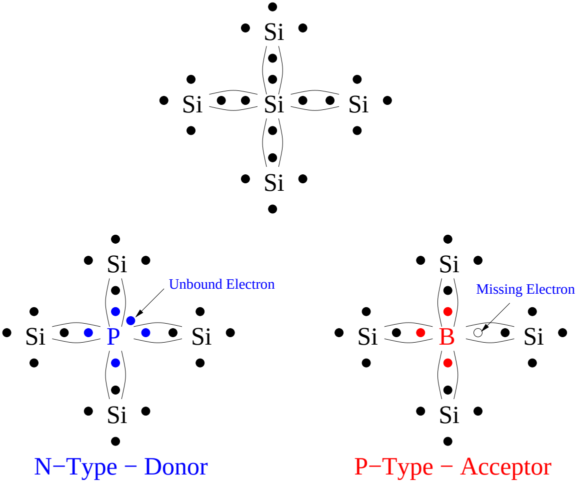
Learning Objectives

- Explain short channel effects(SCE) like Drain Induced Barrier Lowering, Gate Induced Drain Leakage, Sub-threshold leakage, Channel length modulation
- Derive the equation for ON current of a CMOS transistor with first order SC
- Estimate various capacitance values for a transistor
- Estimate the equivalent ON resistance of a transistor

Outline

- Silicon and Doping
- P-N Junction
- CMOS Transistor
  - Threshold Voltage
  - ON Current (I_{ON})
  - Channel length modulation
  - Velocity saturation
  - Sub-threshold leakage
  - Drain Induced Barrier Leakage
  - Gate Induced Drain leakage
  - (Reverse) Short Channel Effect
  - Other leakage mechanisms
  - Capacitance
  - Resistance

Silicon and Doping



- n_i - Intrinsic electron/ hole concentration

Device Physics Abstraction

1. Law of Mass Action - Product of concentrations remains constant

$$np = n_i^2$$

   Where

   - n/p = Electron/ hole concentration after doping
   - n_i = Intrinsic electron/ hole concentration

2. Maxwell Boltzmann Equation -

$$\frac{n_1}{n_2} = e^{\frac{\Psi_{12}}{kT/q}}$$

   Where

   - kT/q - Thermal voltage = 26mV @ 300K
   - n_1, n_2 - Charge concentration across a potential ψ_{12}

PN Junction

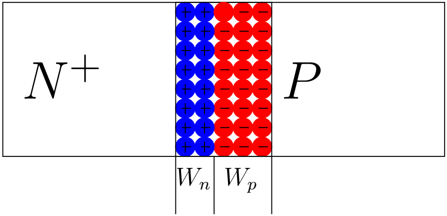


Figure: PN Junction Diode

$$W_n N_D = W_p N_A$$

- Conservation of charge
- Note: $N_D \gg N_A \implies W_p \gg W_n$
- Current is due to diffusion of minority carriers

NMOS Transistor

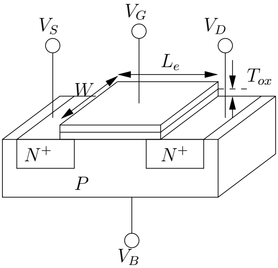


Figure: NMOS transistor

- $V_{GS} < 0$ - Accumulation (Surface becomes more P type than bulk)
- $0 \leq V_{GS} < V_{TH}$ - Depletion (Surface is less P type than bulk)
- $V_{GS} \geq V_{TH}$ - Inversion (Surface is more N than the bulk is P)

Threshold Voltage

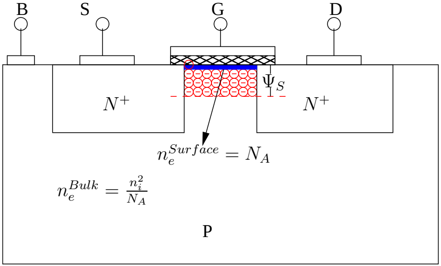


Figure: Inversion

@$V_G = V_{TH}$ - Channel is as N-type as the body is P-type

$$\Psi_S = 2\frac{kT}{q} ln(\frac{N_A}{n_i})$$

$$V_{GB} = \psi_{OX} + \psi_S$$

Threshold Voltage

W_D = Depletion width and Q_D = Depletion charge per unit area

$$W_D = \sqrt{\frac{2\epsilon_{si}|\psi_s|}{qN_A}}$$

$$Q_D = -qN_A W_D = -\sqrt{2qN_A|\psi_s|}$$

$$\psi_{OX} = \frac{-(Q_D + Q_I)}{C_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$V_{TH} = \psi_S - \frac{Q_D}{C_{ox}}$$

Threshold Voltage

- $V_B \neq 0$
- Body effect alters depletion region charge

$$Q_D = \sqrt{2qN_A\epsilon_{Si}|\Psi_S + V_{SB}|}$$

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|\Psi_S + V_{SB}|} - \sqrt{|(\Psi_S)|})$$

Technolopgy parameters

- V_{TH0} - Threshold voltage without body effect
- γ - Body effect coefficient
- Ψ_S - Positive (Negative) for NMOS (PMOS) transistors

NMOS Transistor

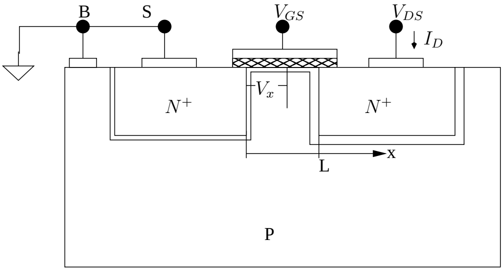


Figure: NMOS Transistor

- $V_{GS} \leq 0$ - OFF
- $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$ - Linear
- $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$ - Saturation

NMOS - ON Current - Linear Region

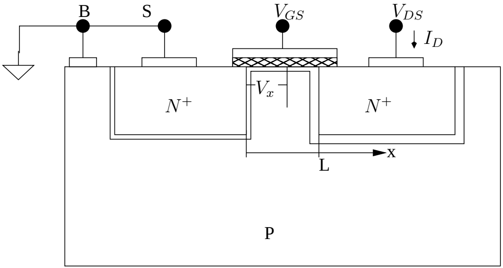


Figure: NMOS Transistor

$$Q_i(x) = -C_{OX}[V_{GS} - V_x - V_{TH}]$$

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$$

$$I_D = -v_n Q_i(x) W$$

NMOS - ON Current - Linear Region

$$v_n = -\mu_n E(x)$$
$$v_n = \mu_n \frac{dV_x}{dx}$$

Substituting we get

$$I_D = C_{OX}[V_{GS} - V_x - V_{TH}]W\mu_n \frac{dV_x}{dx}$$
$$\int_0^L I_D dx = \int_0^{V_{DS}} C_{OX}[V_{GS} - V_x - V_{TH}]W\mu_n dV_x$$
$$I_D = k_n^{'} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$$

NMOS - ON Current - Saturation

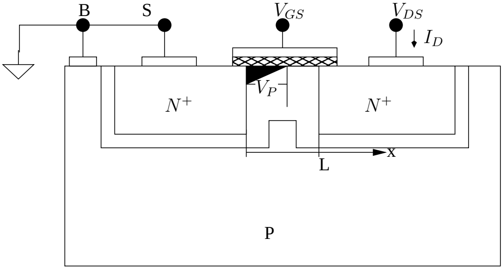


Figure: NMOS Transistor under pinch off voltage (V_P) condition

$$I_D = \frac{k_n{'}}{2}\frac{W}{L}[(V_{GS} - V_{TH})^2]$$

Short Channel Effects

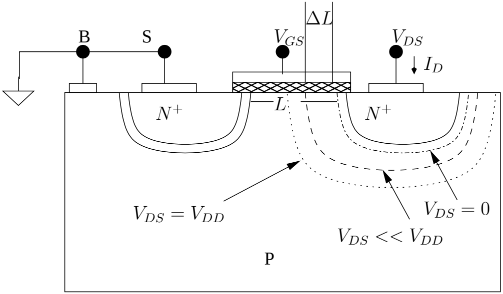


Figure: NMOS Transistor with Short Channel Effects

- Drain is very close to the source (L is very small)
- The depletion regions in the drain and source are comparable to the channel length

Channel Length Modulation

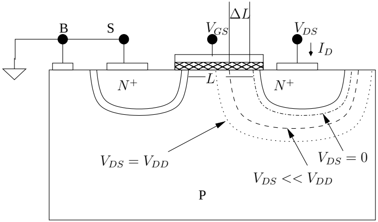


Figure: NMOS Transistor with Short Channel Effects

$$I_D = \frac{k_n{}'}{2} \frac{W}{L - \Delta L}[(V_{GS} - V_{TH})^2]$$

$$I_D = \frac{k_n{}'}{2} \frac{W}{L}[(V_{GS} - V_{TH})^2](1 + \frac{\Delta L}{L})$$

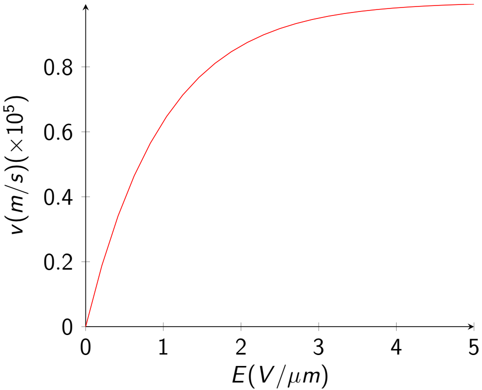
$$I_D = \frac{k_n{}'}{2} \frac{W}{L}[(V_{GS} - V_{TH})^2](1 + \lambda V_{DS})$$

Velocity Saturation

$$v_n = \mu_n E_{Lat}$$

- Not entirely correct - Velocity does not linearly increase with lateral field for ever
- It saturates beyond a critical field E_{Crit}
- Electrons encounter more collisions and hence don't pick up speed
- Maximum velocity of electrons/ holes $= 10^5 m/s$

Velocity Saturation



$$v = \begin{cases} \frac{\mu E}{1+\frac{E}{E_C}} & \text{if } E \leq E_C \\ v_{sat} & \text{if } E > E_C \end{cases}$$

Velocity Saturation- Simplified

Velocity:

$$v = \begin{cases} \mu E & \text{if } E \leq E_C \\ v_{sat} = \mu E_C & \text{if } E > E_C \end{cases}$$

VDS Saturation :

$$V_{DS-SAT} = L * E_C = \frac{L v_{SAT}}{\mu}$$

Velocity Saturated Drain Current:

$$I_{DS-SAT} = I_{DS}(V_{DS} = V_{DS-SAT})$$

$$I_{DS-SAT} = \mu_n C_{OX} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS-SAT} - \frac{V_{DS-SAT}^2}{2} \right)$$

Unified Current Model

- Useful to combine all effects into one equation
- Voltage values determine the governing equations

$$I_{DS} = \begin{cases} 0 & |V_{GS}| < |V_{TH}| \\ k' \frac{W}{L} \left((V_{GS} - V_{TH}) V_{min} - \frac{V_{min}^2}{2})(1 + \lambda V_{DS} \right) & |V_{GS}| > |V_{TH}| \end{cases}$$

Where

$$V_{min} = min(V_{DS}, (V_{GS} - V_{TH}), V_{DS-SAT}) \ldots NMOS$$
$$V_{min} = max(V_{DS}, (V_{GS} - V_{TH}), V_{DS-SAT}) \ldots PMOS$$
$$V_{TH} = V_{TH0} + \gamma(\sqrt{|V_{SB} + \Psi_S|} - \sqrt{\Psi_S})$$

$(V_{TH0}, k', V_{DSAT}, \gamma, \lambda)$ - Technology parameters

Sub-threshold Leakage

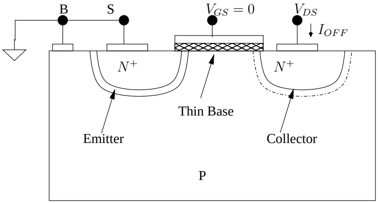
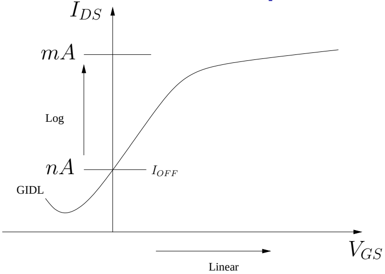


Figure: NMOS Transistor Sub-Threshold Leakage

- In a short channel transistor, the thin channel acts like a thin base of a BJT.
- Diffusion current flows even when $V_{GS} = 0$.
- Exponential dependence on V_{GS}

$$I_{OFF} = I_S e^{\frac{V_{GS} - V_{TH}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) (1 + \lambda V_{DS})$$

Sub-threshold Slope



$$S = \frac{1}{\frac{d(log_{10}(I_{OFF}))}{dV_{GS}}}$$

$$S = n\frac{kT}{q}ln(10)$$

- Ideal transistor $n = 1$, $S_{min} = 60mV/decade$
- Actual transistors $n \approx 1.5$ and hence $S = 90mV/decade$

Gate Induced Drain Leakage (GIDL)

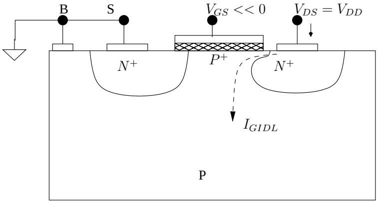


Figure: NMOS Transistor with Halo Implant

- Negative V_{GS} exponentially reduces sub-threshold leakage
- But beyond a point GIDL kicks in
- Surface is in deep accumulation causing a deeper depletion in the diffusion
- Tunneling current from drain to substrate

Drain Induced Barrier Lowering (DIBL)

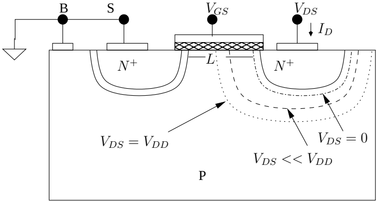


Figure: NMOS Transistor DIBL

- Drain controls amount of depletion in the channel
- Easier for the gate to invert with higher V_{DS}
- Gate effectively has lesser control

Drain Induced Barrier Lowering (DIBL)

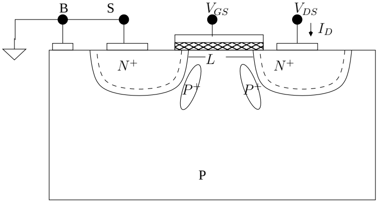
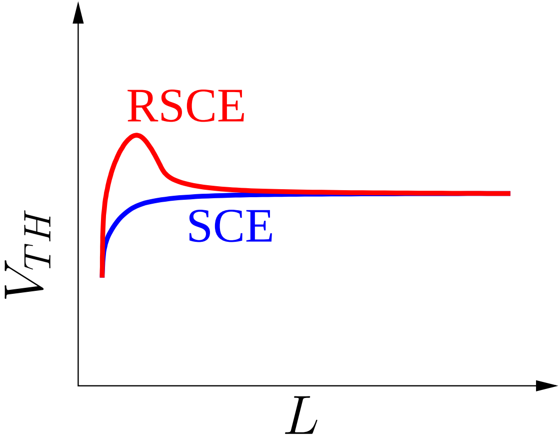


Figure: NMOS Transistor with Halo Implant

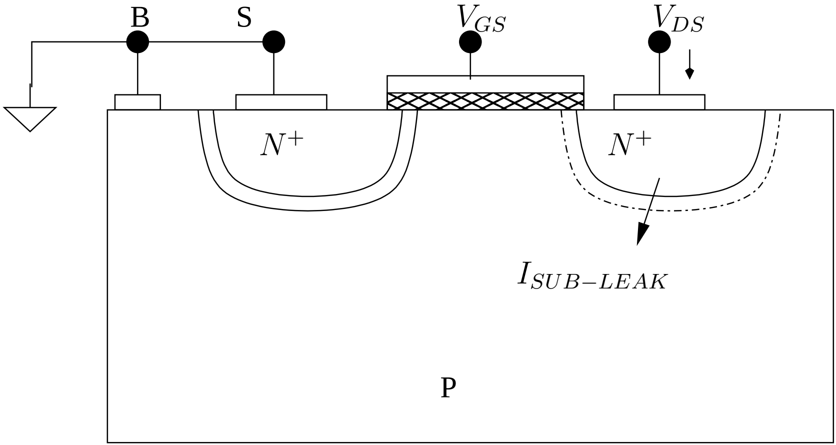
- P^+ halo added near diffusion
- Depletion layer now goes deeper into the diffusion rather than channel
- Gate has better control now
- $DIBL = \frac{V_{TH}(V_{DS}=V_{DD}^{H}) - V_{TH}(V_{DS}=V_{DD}^{L})}{V_{DD}^{H} - V_{DD}^{L}}$

Reverse Short Channel Effect



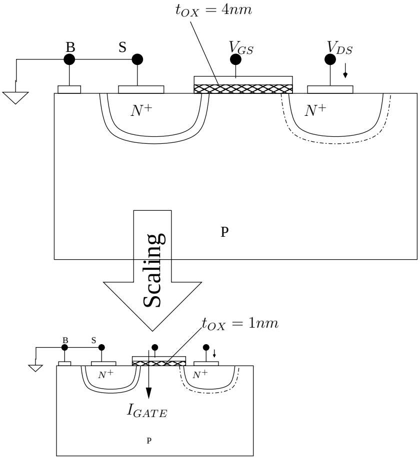
Halo implant makes it harder to invert the channel

Substrate Leakage



Reverse biased $P - N^+$ junction leakage

Gate Leakage



- Quantum mechanical tunneling across the gate oxide
- Use of HfO_2 - HiK dielectric since 45nm technology

Capacitance

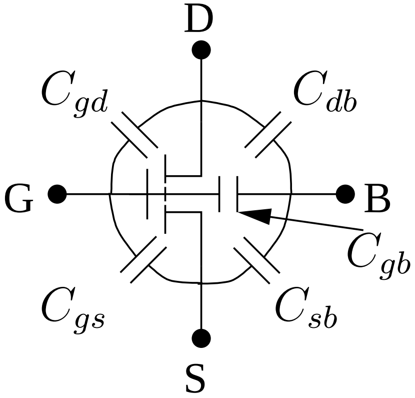


Figure: Capacitance Model

Gate Capacitance

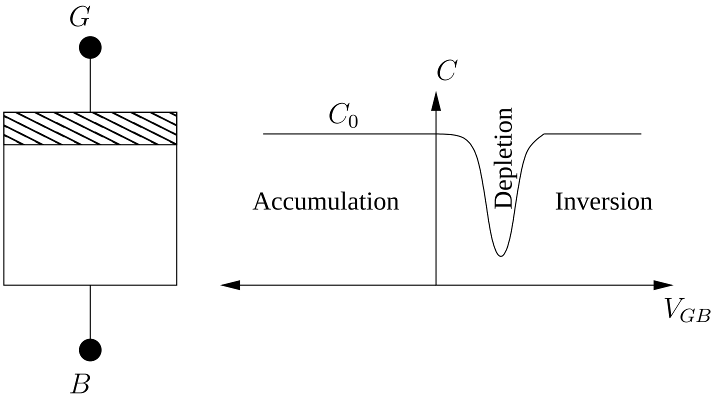


Figure: Capacitance Model

$$C_0 = \frac{\epsilon WL}{t_{ox}}$$

Gate Capacitance

Parameter	Cutoff	Linear	Saturation
C_{gb}	C_0	0	0
C_{gs}	0	$C_0/2$	$(2/3)C_0$
C_{gd}	0	$C_0/2$	0
$C_g = C_{gb} + C_{gs} + C_{gd}$	C_0	C_0	$(2/3)C_0$

$$C_0 = \frac{\epsilon_{ox} WL}{t_{ox}}$$

For all practical purposes $C_g \approx C_0$

Overlap Capacitance

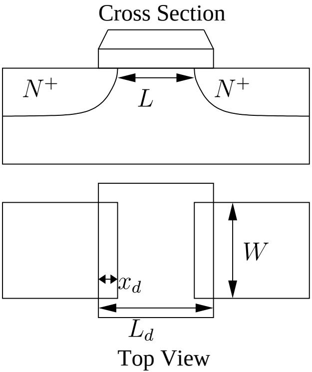


Figure: Overlap Capacitance

$$C_{overlap} = \frac{\epsilon_{ox} W x_d}{t_{ox}} = C_{ov} W$$
$$C_G = C_{OX} WL + 2 C_{ov} W$$

Diffusion Capacitance

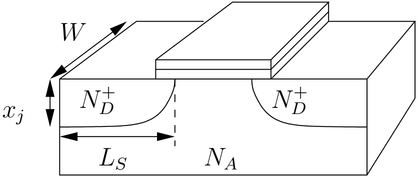


Figure: Diffusion Capacitance

- Bottom plate capacitance
- Sidewall capacitance

Diffusion Capacitance

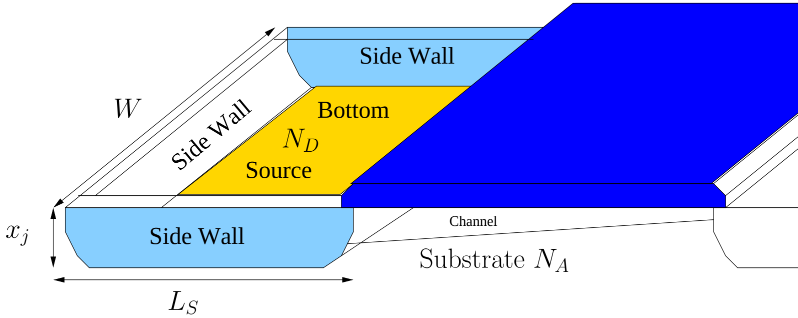
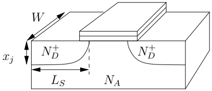


Figure: Diffusion Capacitance

Bottom Plate Diffusion Capacitance



$$C_{Bottom} = C_j W L_S$$

$$C_j = \frac{C_{j0}}{(1 + V_{SB}/\phi_0)^m}$$

$$C_{j0} = \sqrt{(\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}) \phi_0^{-1}}$$

$$\phi_0 = \frac{kT}{q} ln(\frac{N_A N_D}{n_i^2})$$

$$m \approx 0.5$$

C_j is charge per unit area. Similar expressions hold for the drain side ($V_{SB} \rightarrow V_{DB}$) as well.

Side wall Diffusion Capacitance

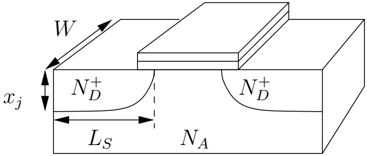


Figure: Diffusion Capacitance

$$C_{Side-wall} = C'_{jsw} x_j (W + 2L_S)$$

$$C_{jsw} = C'_{jsw} x_j$$

$$C_{diff} = C_{bottom} + C_{sw} = C_j L_S W + C_{jsw}(W + 2L_S)$$

C_{jsw} is capacitance per unit length.

Capacitance Summary

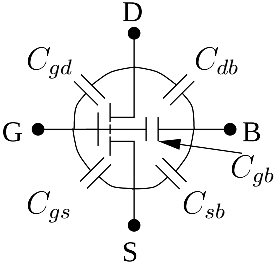


Figure: NMOS Capacitance

$$C_G = C_{GS} + C_{GD} + C_{GB} + 2C_{overlap} = C_{OX}WL + 2C_{ov}W$$
$$C_{DB} = C_j L_S W + C_{jsw}(W + 2L_S)$$
$$C_{SB} = C_j L_S W + C_{jsw}(W + 2L_S)$$

Resistance

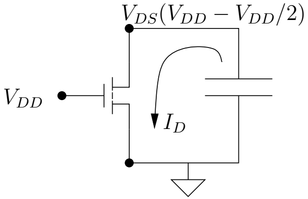


Figure: NMOS Equivalent Resistance

$$R_{eq} = \frac{1}{V_{DD}/2 - V_{DD}} \int_{V_{DD}}^{V_{DD}/2} R(V)dV$$

$$R_{eq} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1 + \lambda V)} dV$$

$$R_{eq} \approx \frac{3V_{DD}}{4I_{DSAT}} \left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

Resistance

$$R_{eq} \approx \frac{3V_{DD}}{4I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

$$I_{DSAT} = k'\frac{W}{L}((V_{DD} - V_{TH})V_{DSAT} - \frac{V_{DSAT}^2}{2})$$

- Resistance $R_{eq} \propto \frac{1}{W/L}$ - Doubling $W \implies R_{eq}$ halves
- If $V_{DD} >> V_{TH} + V_{DSAT}/2$, R_{eq} is independent of V_{DD}. Minor dependence due to CLM (λ)
- As $V_{DD} \rightarrow V_{TH}$, resistance goes up significantly

BSIM SPICE Level 1 Model

	V_{TH0}	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(\mu A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115	0.06
PMOS	-0.4	-0.4	-1	-30	-0.1

Table: Parameters of a $0.25\mu m$ CMOS process for a *minimum* length device

- Calculate the drain current of a PMOS transistor in $0.25\mu m$ technology whose $W/L = 0.5\mu/0.25\mu$ when biased at $V_{GS} = -0.6V$, $V_{DS} = -0.3V$ and $V_{SB} = 0V$
- Repeat the above calculation this time with $V_{DS} = -1.1V$ and $V_{GS} = -2V$
- Calculate the threshold voltage of a NMOS device when the body is biased at $V_{SB} = 0.11V$. Assume that $\psi_S = 0.25V$

Capacitance Model

	C_{OX} $(fF/\mu m^2)$	C_{ov} $(fF/\mu m)$	C_j $(fF/\mu m^2)$	m_j	ϕ_b $(V$	C_{jsw} $fF/\mu m)$	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Table: Capacitance parameters of a $0.25\mu m$ CMOS process

- Calculate variaous capacitances of an NMOS transistor with $W/L = 0.36\mu m/0.24\mu m$ in a $0.25\mu m$ technology where $L_D = L_S = 0.625\mu m$ under zero-bias condition
- Calculate the equivalent resistance of an NMOS transistor with a $W/L = 1$ when connected to a $V_{DD} = 1.5V$

Summary

- A transistor operates in 4 regions - cut-off, linear, velocity saturation and saturation.
- Identify the region using the unified current model
- Level-1 SPICE model parameters - $(k', \lambda, V_{DSAT}, V_{TH0}, \gamma)$
  - All positive for NMOS and all negative for PMOS
- Sub-threshold leakage is proportional to $e^{\frac{V_{GS}-V_{TH}}{n(kT/q)}}$
- Beware of forward biasing any junction
- All capacitance components change linearly with W
- Diffusion and overlap capacitances of a transistor don't depend on L
- Equivalent resistance of a transistor is proportional to $\frac{1}{W}$

References

The material presented here is based on the following books/ lecture notes

1. Digital Integrated Circuits Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic 2nd Edition, Prentice Hall India