EE5311- Digital IC Design

Introduction

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August 1, 2022

Outline

- Class Timings
- Grading
- Assignments
- Motivation
- Chip complexity
- Design Flow
- Learning Objectives
- Course Structure

Class Timings

G Slot

- M(12:00-12:50 PM) - Theory
- W(4:50 - 5:40 PM) - Layout discussion
- Th(10:00-11:00 AM) - Theory
- F(9:00-10:00 AM) - Theory

Grading

- Assignments - 10%
- Weekly Quiz - 20%
- End sem - 40%
- Project - 30%

Assignments

- Simulation with SPICE simulators
- Access to personal Laptops?

Motivation

Number system

$$x = \sum_{k=0}^{N-1} a_k b^k$$

$$x_{10} = \sum_{k=0}^{M-1} a_k 10^k$$

$$x_2 = \sum_{k=0}^{N-1} b_k 2^k$$

- Binary representation allows operation with two levels - 0 and 1 or Low and High
- Computation is key to efficient data processing
- What kind of computations?

Motivation - Computations

Kind of computations

- Arithmetic
- Logical
- Special purpose computations - Convolution in DSPs

Computational efficiency?

- How fast?
- How much energy?

Focus of the Course

Quantifying computational efficiency

- How fast?
- How much energy?

Improving computational efficiency

- Can be made faster?
- Can be done expending lesser energy?

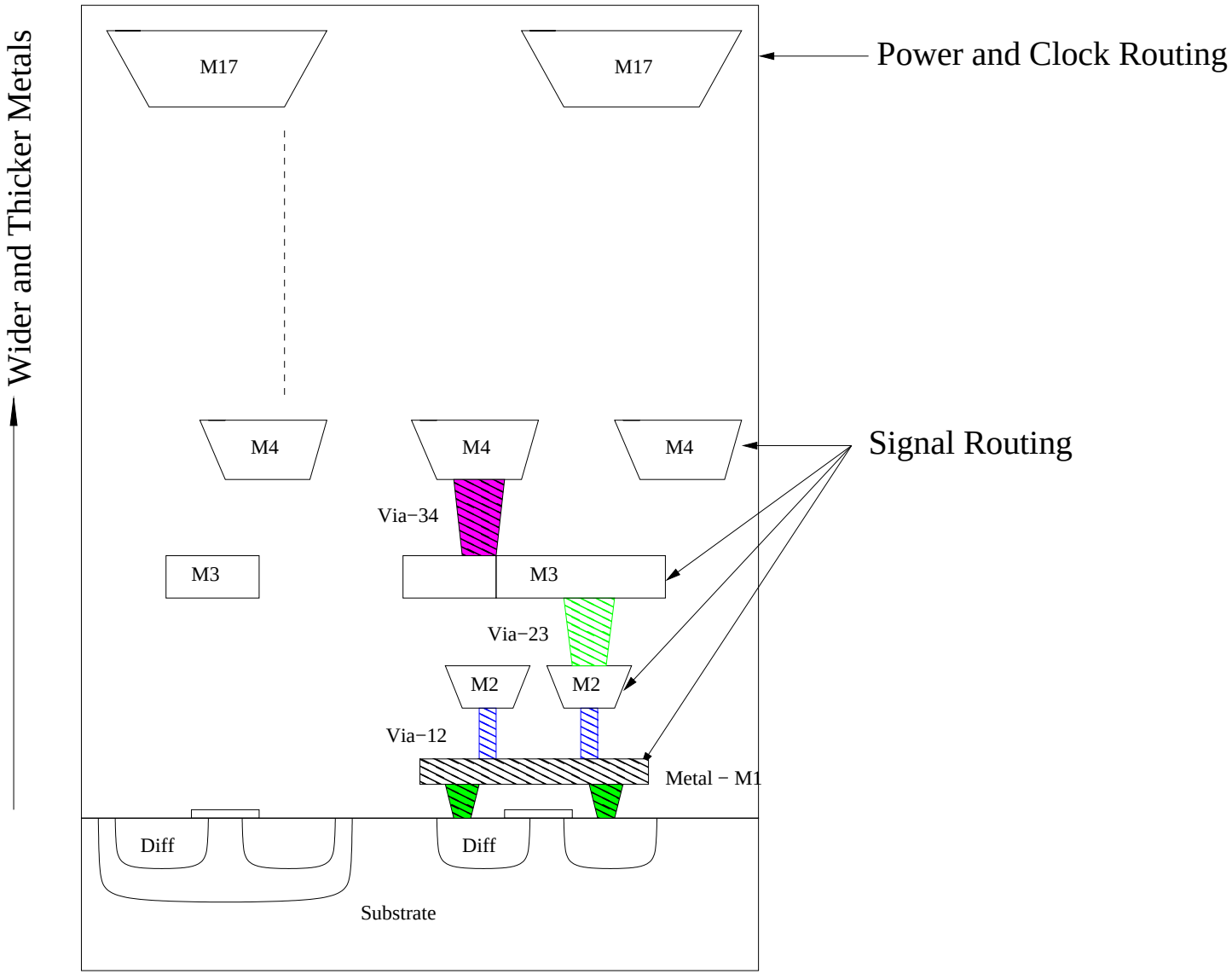
How Complex are todays Designs?

Chip	IBM $P9^{TM}$	IBM $P10^{TM}$
Technology	14nm FinFET SOI	7nm Bulk
No. Cores	24	60
Area(mm^2)	695	602
No. of Transistors (B)	8	18
No. Vias(B)	-	110
No. Metal Levels	17	18
M1-M3 Pitch (nm)	64	-
M4-M5 Pitch (nm)	80	-
MX-M(X-1) (nm)	2400	2160

1. C. Gonzalez et al., "3.1 POWER9: A processor family optimized for cognitive computing with 25Gb/s accelerator links and 16Gb/s PCIe Gen4," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 50-51.

2. R. M. Rao et al., "POWER10: A 16-Core SMT8 Server Processor With 2TB/s Off-Chip Bandwidth in 7nm Technology," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 48-50, doi: 10.1109/ISSCC42614.2022.9731594.

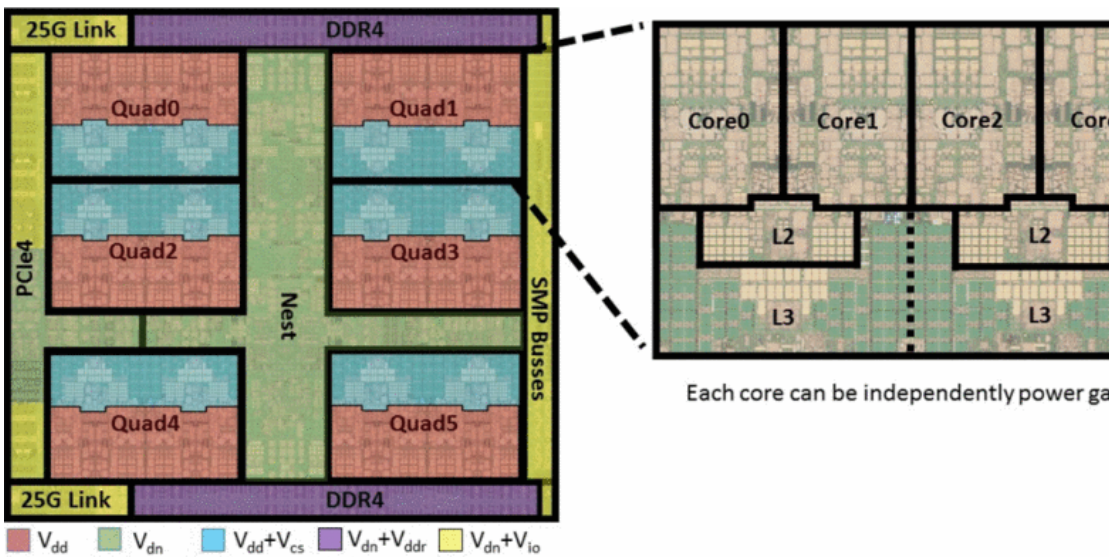
Chip Cross Section



Chip Components

- 6 quadrants with 4 cores each
- Each quadrant has shared L2 and L3 cache
- Each core has its own L1 cache
- L1, L2 - SRAM
- L3 - eDRAM
- How do you design such a complex chip? Manually?

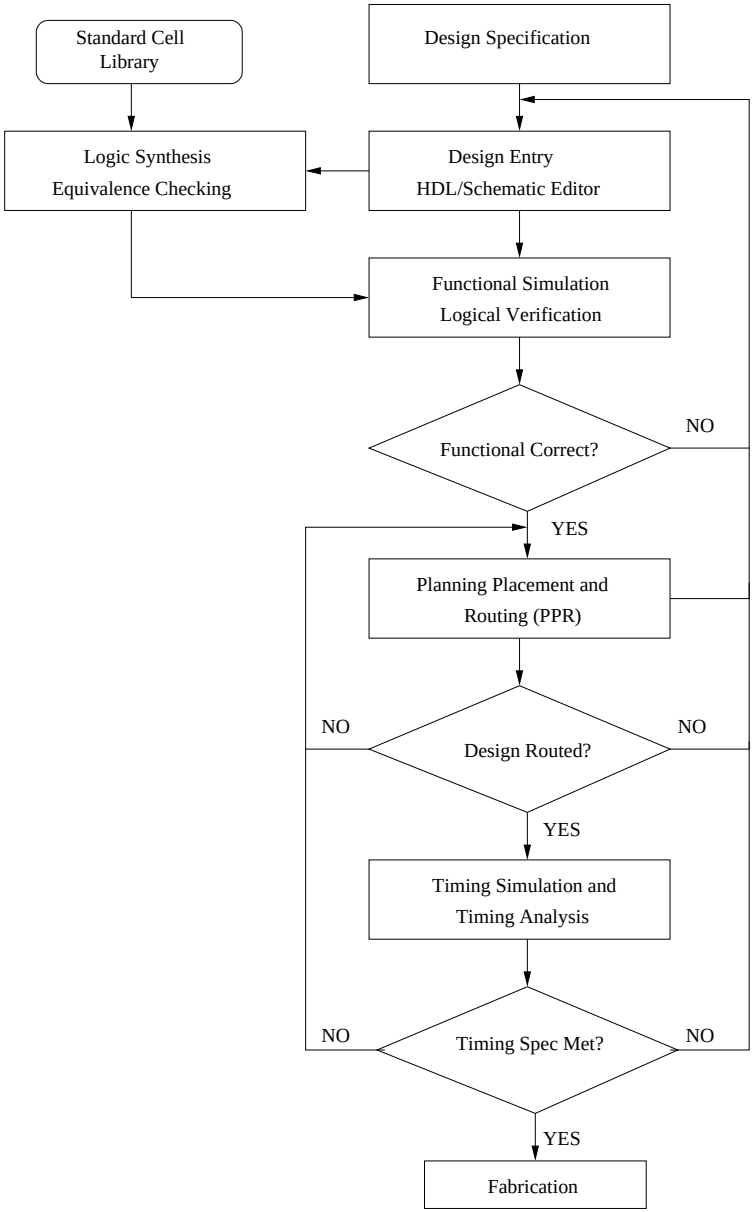
C. Gonzalez et al., "3.1 POWER9: A processor family optimized for cognitive computing with 25Gb/s accelerator links and 16Gb/s PCIe Gen4," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 50-51.
Image Source: IEEE Explore



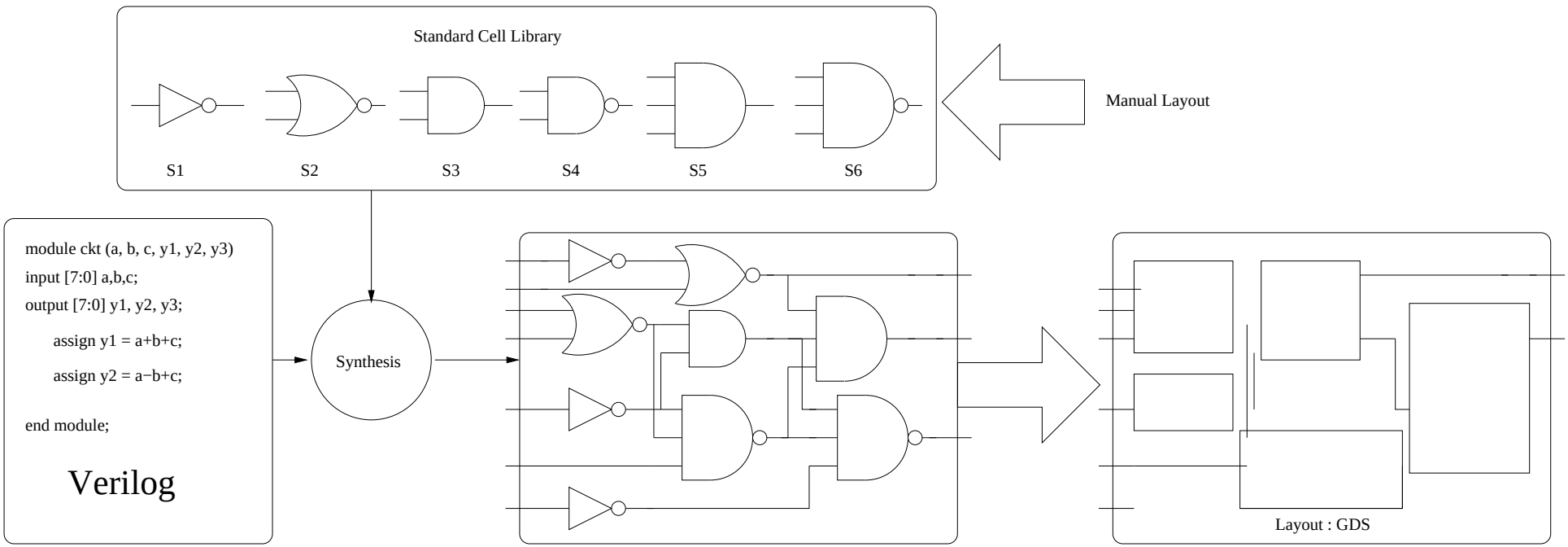
VLSI Design Flow

- Chip design is heavily automated
- Only critical blocks are hand laid out
- Significant portion of the chip is described using Hardware Description Language
- Only standard cells are laid out manually
- Analog blocks are custom designed - Heavily layout sensitive
- Push button level automation is available!

Design Flow

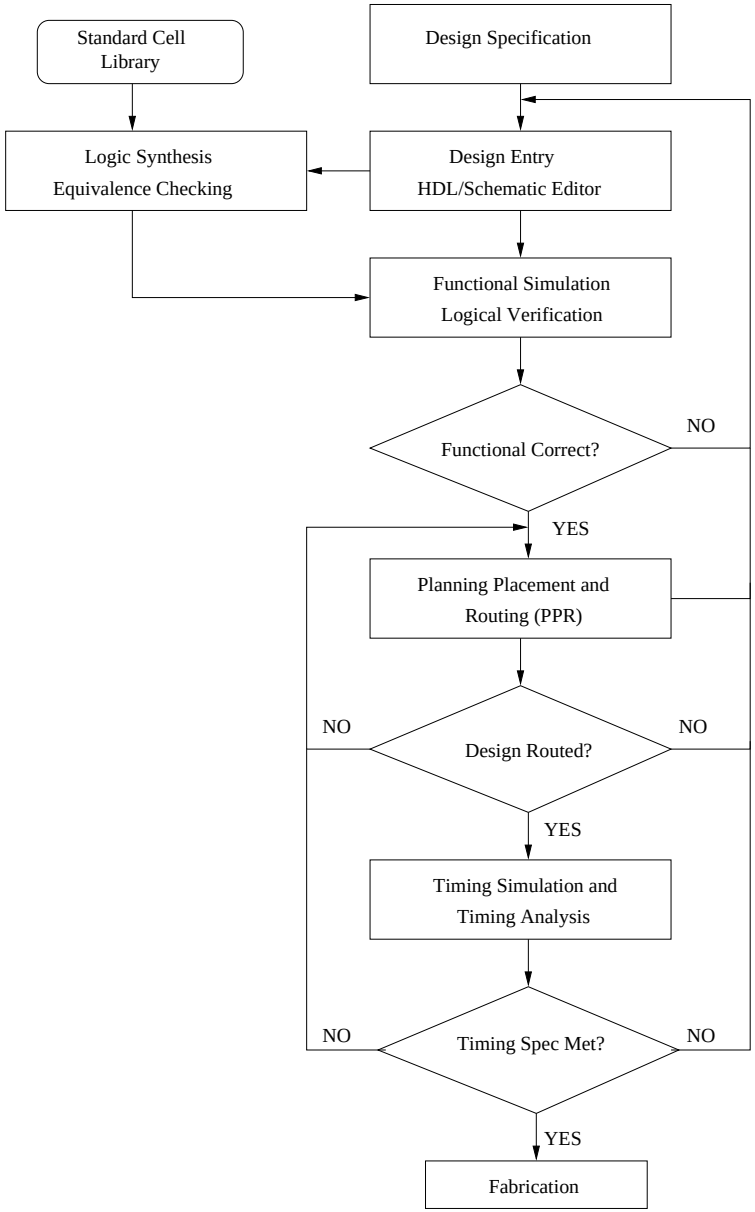

Standard Cell Library
Design Specification
Logic Synthesis
Equivalence Checking
Design Entry
HDL/Schematic Editor
Functional Simulation
Logical Verification
Functional Correct?
NO
YES
Planning Placement and
Routing (PPR)
NO
Design Routed?
NO
YES
Timing Simulation and
Timing Analysis
NO
Timing Spec Met?
NO
YES
Fabrication

Design Flow



Looks great! Why waste our time?

Loops Need Not Converge



Why Study This Course?

- Not guaranteed to get an optimized output
- Doesn't tell you how to make a design better
- Tools are only as intelligent or stupid as the information they're provided with
- Humans (hopefully!) are a little better

Course Structure

Course comprises of FIVE modules

1. The Transistor - Abridged version
2. The Inverter
3. Combinational Circuit Design
4. Sequential Circuit Design
5. Design of Adders and Multipliers

Learning Objectives

- Characterize the key delay quantities of a standard cell
- Evaluate power dissipated in a circuit (dynamic and leakage)
- Design a circuit to perform a certain functionality with specified speed
- Identify the critical path of a combinational circuit
- Convert a combinational block to pipelined circuit
- Calculate the maximum (worst case) operating frequency of the designed circuit

What This Course is NOT about.

- Automated tool flow
- Verilog Design
- Digital logic design (pre-requisite)
- Microprocessor instruction design

Text Books

- Digital Integrated Circuits Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic 2nd Edition, Prentice Hall India
- CMOS VLSI Design, Neil H.E. Weste, David Harris and Ayan Banerjee, 3rd Edition, Pearson Education