Replica Bias Scheme for Efficient Power Utilization in High-Frequency CMOS Digital Circuits

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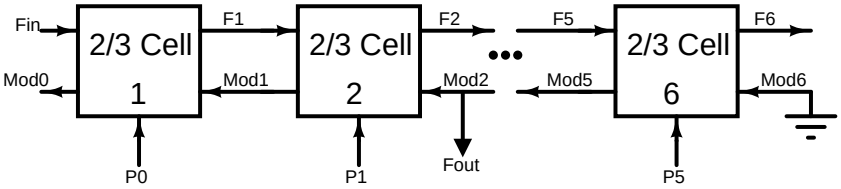
Overview

Introduction

- High frequency designs favor standard CMOS implementations
- Need low power dissipation, low delay and delay spread over PVT
- Technology scaling increases process variations [1]
- Supply and temperature shifts further affect cell delays
- Mitigating cell delay spread through increased current is inefficient

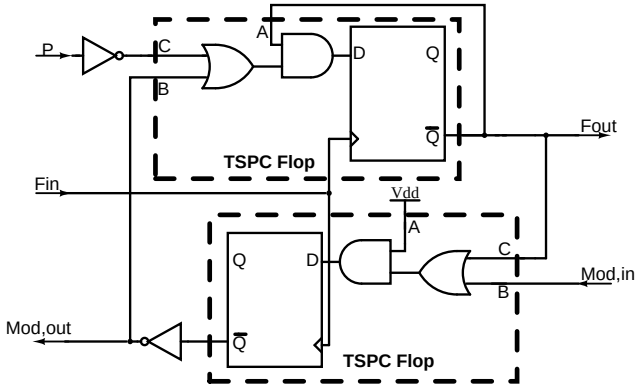
Chosen application - Feedback divider in PLL

- Carrier signal required for modulation/demodulation
- Frequency synthesizer generates LO output from crystal reference
- Feedback divider operates at high frequencies dissipating large power
- Modular divider architecture [2]

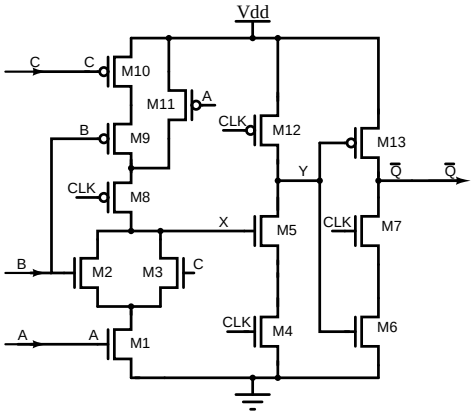


Fin=4.8GHz; Fref=40MHz; N=120;

Conventional implementation - 2/3 cell



Conventional implementation - TSPC flip flop



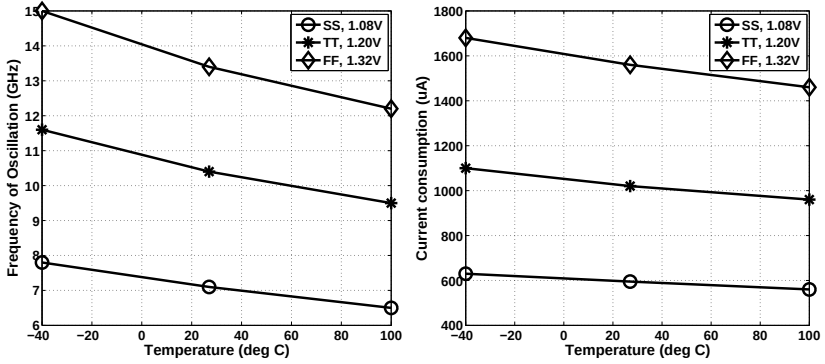
Conventional implementation - Simulation results

Parameter	Min	Typ	Max	Units
Supply voltage	1.08	1.2	1.32	V
Temperature	-40	27	100	°C
Frequency of operation	0.02	4.8	6.5	GHz
Current consumption	1.5	2	2.51	mA
Power dissipation	1.62	2.4	3.3	mW
Clk to Out delay	145	235	360	ps

- Power dissipation and clock-to-output delay show 2X and 2.5X spread respectively

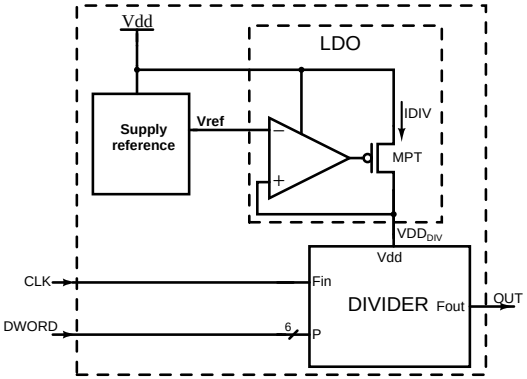
Variations in current consumption and delay

- TSPC flop works like a 3-stage ring oscillator
- A 3-stage ring oscillator frequency and current consumption indicates PVT spread
- 3X variation in ring oscillator current : suboptimal operation

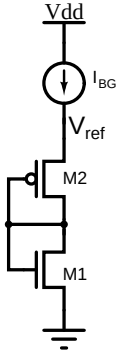


Power and delay optimized divider

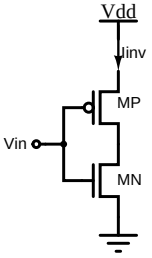
- Changes in process and temperature can be nullified by adjusting supply accordingly
- Similar techniques have been reported for analog circuits targeting supply rejection [3],[4],[5]

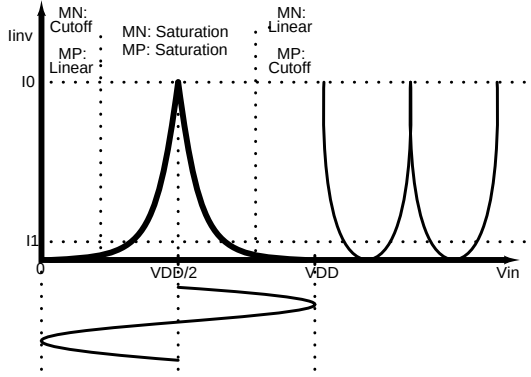


Reference selection



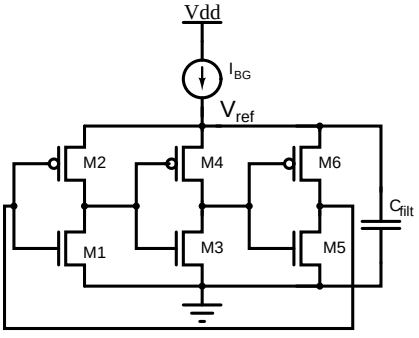
Static Inverter reference





- I-V characteristics of the reference and divider must match
- Current limited static inverter cannot function as reference

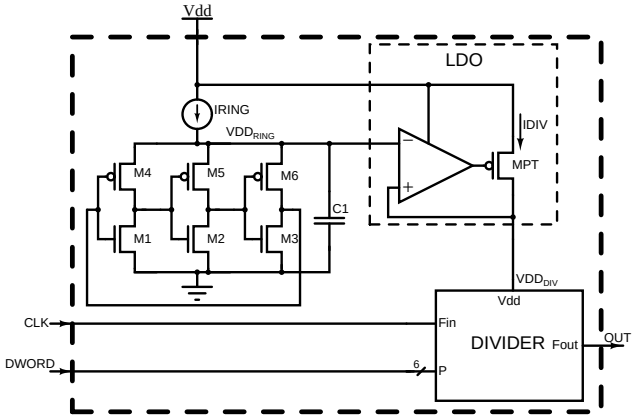
Reference selection



Oscillating Inverter reference

- Current starved ring oscillator can function as a reference generator
- Inveters forced to operate on a fixed current and have fixed delays

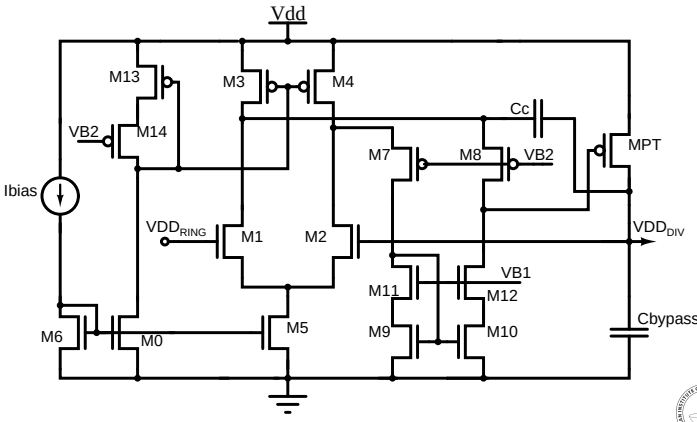
Proposed Divider



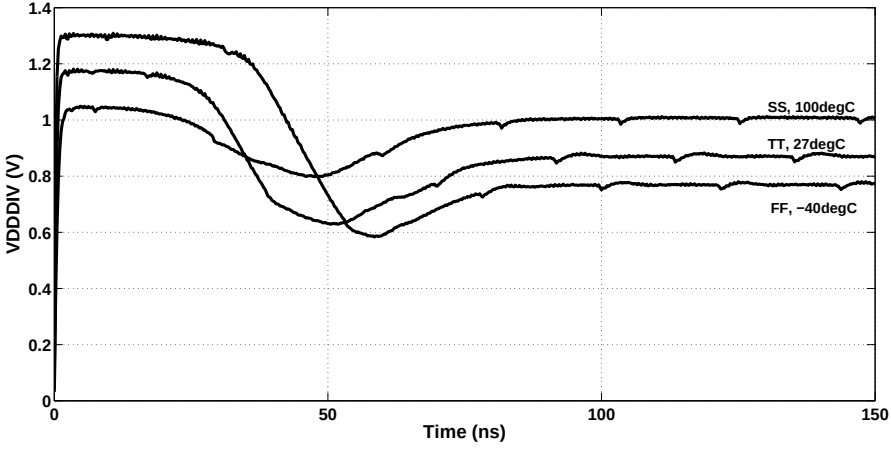
- Process and temperature variations are nulled by reference profile
- Regulator shields from supply changes

Regulator design - Schematic

- Two stage design
- Miller compensated
- No external capacitor



Regulator design - Load transient response

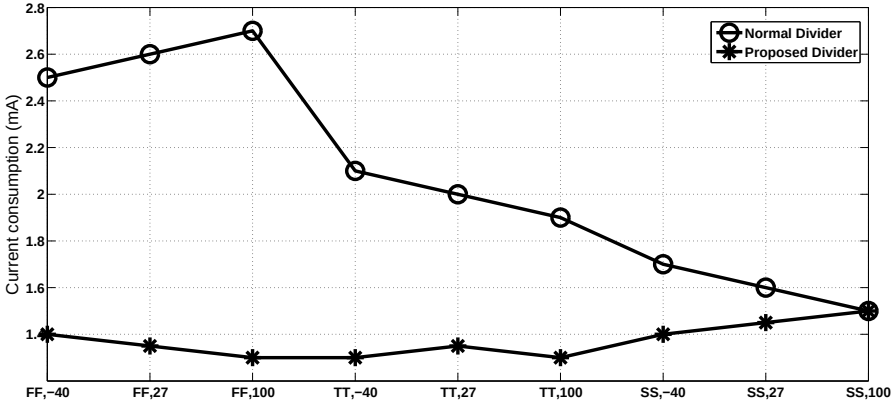


Proposed divider - Simulation Results

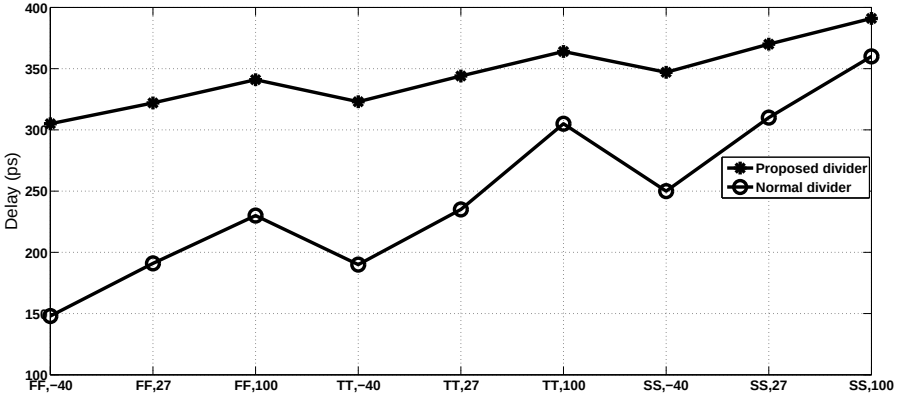
Parameter	Min	Typ	Max	Units
Supply voltage	1.08	1.2	1.32	V
Temperature	-40	27	100	°C
Divider Supply voltage	0.77	0.87	1	V
Frequency of operation	0.005	4.8	5.8	GHz
Current consumption	1.2	1.4	1.5	mA
Power dissipation	1.3	1.68	1.98	mW
Clk to Out delay	305	345	400	ps

- Ring oscillator biased at 100uA, LDO consumes 10uA
- Current consumption decreases by 43% and 67% in the typical and extreme cases
- Delay variation brought down to $[-11\%, +19\%]$ from $[-39\%, +50\%]$
- Maximum operational frequency decreases

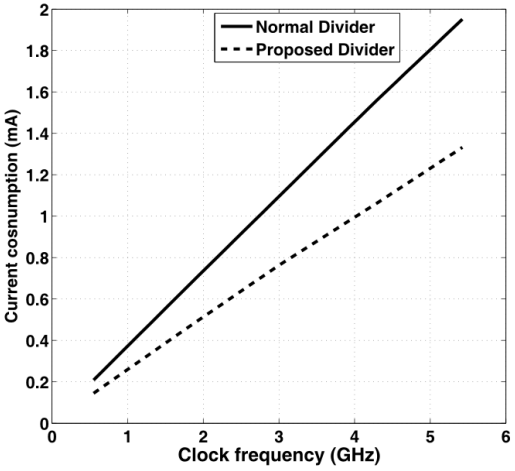
Results comparison - Current consumption

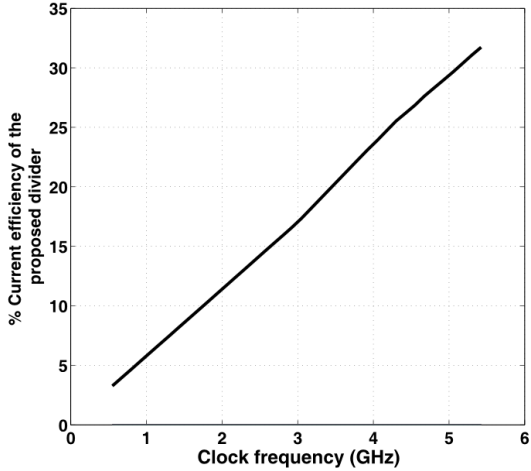


Results comparison - Delay



Results comparison - Frequency





At Typical, 27°C, 1.2V

Conclusion

- Power dissipation is optimum over PVT
- Delay variability is minimized
- Divider operates on regulated supply
- Efficiency increases with required current
- Reference voltage indicates process - can be used as a process monitor

References

[1] Y. Cao and L. Clark, "Mapping statistical process variations toward circuit performance variability: An analytical modeling approach," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 26, no. 10, pp. 1866–1873, 2007.

[2] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35μm cmos technology," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 7, pp. 1039–1045, 2000.

[3] V. V. Ivanov and I. M. Filanovsky, *Operational amplifier speed and accuracy improvement*. Kluwer academic publishers, 2004, section 3.5.

References (cont.)

[4] M. A. T. Sanduleanu and J. Frambach, "1GHz tuning range, low phase noise, LC oscillator with replica biasing common-mode control and quadrature outputs," in *Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th European*, 2001, pp. 506–509.

[5] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 11, pp. 1723–1732, 1996.