Ground-Bounce Reduction in Narrow-band RF Front-Ends

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***Abstract*—Ground-bounce due to bond wire inductance is a well known problem in Radio-Frequency (RF) Integrated Circuits. In this paper we propose the use of series resonance with an extra bond wire to substantially reduce ground-bounce effects in narrowband RF front-ends. Instability caused by the ground bond wire is also tackled. Impedance balancing of output stage to null ground-bounce due to other on-chip circuitry is discussed. The proposed techniques are applied to the design of a power amplifier (PA) for 2.5GHz applications and detailed simulations are performed to support the same.**

I. Introduction

Recent years have seen complete integration of RF circuits on an IC. At RF frequencies, the impedance offered by package parasitics in the form of bond wires and leads become comparable to the load and source impedances. Unless taken into account, it is very difficult for RF signals to cross the barrier between chip and board formed by these package parasitics. It is common to use lead-less packages (such as QFN) for RFICs but the presence of bond wires still adds parasitic inductance that adversely affects circuit performance. Bond wire inductance can be absorbed into matching networks at input and output nodes but ground-bounce due to bond wire inductance at ground node still remains a problem. In digital ICs, the use of conductive substrates [1] provides a low impedance path for ground and alleviates latch-up issues at the same time. However, this is not possible in modern mixed-mode CMOS technologies which use moderately conductive substrates to reduce substrate coupling and substrate losses. In switching circuits, ground-bounce can be reduced by controlling signal slew at the output, using output buffers with RLC damping [2] or by modulating the clock frequency [3]. Techniques to reduce ground-bounce in switching circuits cannot be directly used in RFIC front-ends because in the latter, performance metrics are based on sinusoidal steady state rather than time domain settled output. The following subsections discuss the methods normally employed to minimize ground-bounces and their effects in RFICs.

A. Minimizing bond wire inductance

Generally, it is preferred to minimize bond wire inductance as much as possible. This is done by preferentially reducing the length of bondwires connecting to sensitive nodes. Length reduction can be achieved by placing the die at an offset from the centre of package so as to bring RF bond pads closer to package pins. This can significantly increase bond wire length for other pins and cause mechanical instability. Connecting a lot of bond wires in parallel too can reduce the effective inductance if their mutual coupling is prevented. But this increases pin count and total chip area both of which are expensive.

B. Differential implementation

Differential implementation of RF front-ends can reduce ground-bounce effects as odd mode RF signal currents will not flow through the ground path. However, in most cases, the differential signal has to be converted to single-ended form outside the chip to interface with off-chip components that are tradionally single-ended. This conversion is usually done using an off-chip balun as on-chip transformers tend to be highly lossy. Any loss in the balun degrades noise figure in the receive path and increases insertion loss in the transmit path.

C. Supply decoupling capacitor

A large capacitor can be connected between power and ground inside the chip to supply transient currents. This protects on-chip circuitry from ground-bounce as all nodes are referenced to the same ground. However, RF front-end blocks still have to interface with off-chip components having a different reference node. Consequently, any RF signal flowing through the bond wire causes inductive voltage drops which is seen by the off-chip components.

From the above discussion it is clear that reducing ground-bounce due to bond wires in an RFIC is not trivial and special attention is required to transport RF signals in and out of an IC. In section II and III, we take the example of a stand-alone PA to show effects of ground-bounce and explain the proposed use of an extra bond wire to substantially reduce the effects of ground-bounce for narrow-band operation. This technique can be extended for other RF front-end blocks too. Section IV discusses impedance balancing of the output stage to null the effects of ground-bounce due to other on-chip circuits. Sections V illustrates the proposed techniques with simulation results, as applied to a CMOS PA operating at 2.5GHz and having a 1-dB compression point of 16dBm. Section VI summarizes and concludes the paper.

II. Ground-bounce in stand-alone PA characterization

PA characterization (Fig. 1) involves applying a known input and measuring the corresponding output using off-chip equipment. The PA input should be impedance-matched with the RF input source to be able to feed a known amount of power. The PA output too should only see the impedence of the measuring device. Presence of bond wires in the input,

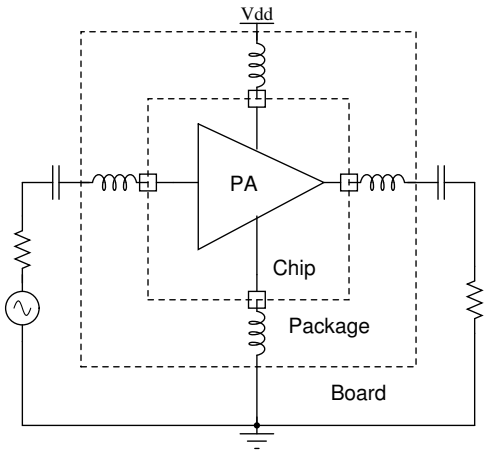


Fig. 1. Stand alone PA charcterization set-up

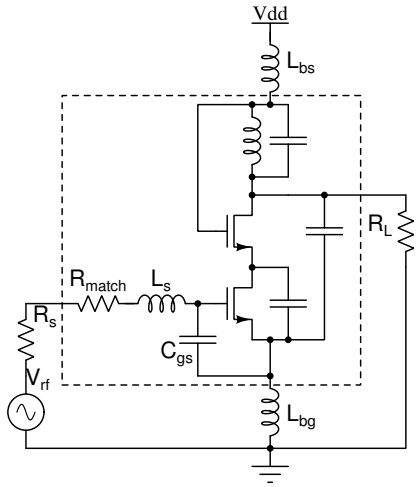


Fig. 2. Cascode PA with ground bond wire

output and ground paths makes it difficult to satisfy the above conditions. While the bond wires at input and output nodes can be resonated with suitable series off-chip capacitors, the bond wire in the ground path needs to pass DC current, and possibly, harmonics of the RF signal. Any RF signal flowing through the ground bond wire causes an inductive voltage drop which is seen as ground-bounce. Here, the example of an nMOS cascode PA (Fig. 2) is considered to illustrate problems due to ground bond wire inductance. For analysis alone, the bond wire is modelled as a simple series inductance.

A. Input and output matching

The ground bond wire is shared between input and output circuits. The impedance seen at the input of the PA is (Fig. 3a)

$$z_{in} = \frac{1}{c_{gs}} + z_b + \frac{g_m z_b}{j\omega c_{gs}} \tag{1}$$

where, z_b denotes the equivalent impedance between nMOS source and ground nodes. As the nMOS transconductance changes at high power levels, the input impedance is also affected. This change in impedance degrades matching, unless accounted for separately at the input and output.

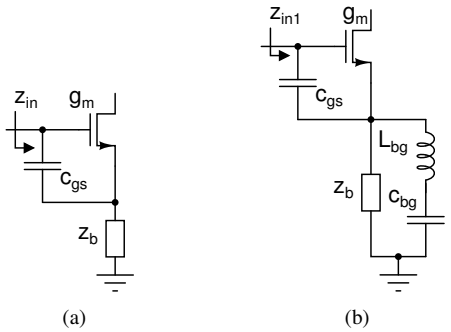


Fig. 3. Input nMOS (a) with impedance degeneration (b) with series LC to reduce feedback at desired frequency

B. Stability

Presence of an inductance at the source of the nMOS introduces feedback in the input network (Fig. 3a). This can cause a frequency-dependent negative resistance to appear at the input port, depending on the kind of matching network used. In this work, series RLC resonant matching is used at the PA input. Bond wires at input and output nodes have been neglected for stability analysis and it is assumed that the PA is stable without the ground bond wire. For global stability,

$$Re[z_{in}] + R_{match} > 0 \tag{2}$$

where R_{match} is the resistance added on-chip to match the source resistance R_s (Fig. 2). At low frequencies, z_b is inductive. As frequency increases, z_b becomes capacitive, resulting in a negative real input impedance as seen from last term of (1). This negative resistance is inversely proportional to the square of frequency and may cause instability if (2) is violated at medium frequencies.

III. Reducing ground-bounce effects in stand-alone PA characterization

As seen from the analysis in the previous sections, the primary problem due to ground bond wire is feedback at the source node of the input device. In this section, a technique is first proposed to reduce feedback at the desired frequency of operation. Following this, the circuit is stabilized at all frequencies.

A. Improving matching

If an additional bond wire is taken from on-chip ground node and connected to board ground through an off-chip capacitor as shown in Fig. 3b, then the on-chip ground node and board ground will be at the same potential for the series resonant frequency of this LC circuit. The series resonant frequency can be set to be equal to the frequency of operation to improve matching, reduce feedback and make the input impedance less dependent on the device transconductance over a narrow band of frequencies. Likewise, the output network becomes purely resistive at the operating frequency. The presence of L_{bg} and C_{bg} increases the quality factor (Q) of both input and output matching networks. For typical values of source and load impedances and bond wire inductance, the Q is low enough to allow narrow-band operation at RF frequencies. Though this technique requires an extra bond wire, bond pad

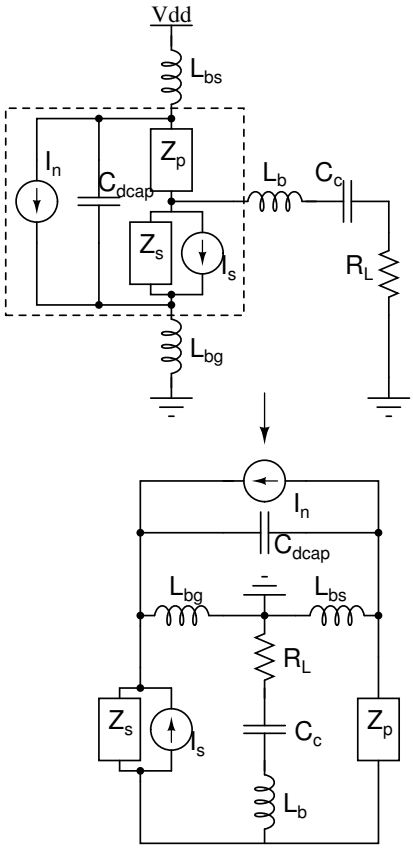


Fig. 4. Output stage with bond wires

and package pin, the improvement in matching is much better than what can be achieved by simply connecting two bond wires in parallel. For best performance advantage, the two bond wires should be placed such that there is no mutual coupling between them.

B. Stabilization

The addition of L_{bg} and C_{bg} reduces feedback only over a narrow band of frequencies. Therefore, stability at other frequencies is still of concern. Stability can be improved by reducing Q of the input network. One potential approach is to increase R_{match} in the input matching network. However, this will require a second matching network to match to R_s which is normally constrained to be 50Ω. In this work, an extra capacitance is placed between gate and source of the input nMOS device to reduce Q. At the same time, a resistance is inserted in series with the supply decoupling capacitor to inrease loss. A similar method has been used earlier to improve stability [4] in a different context. The exact value of the resistance is chosen to stabilize the network at all frequencies. Since the series resonance at the ground node weakens feedback in the desired narrow-band frequency, loss added in z_b will not affect PA performance.

IV. Impedance balancing in RF output stage

All devices on an IC share a common substrate. Similarly, the on-chip ground node is often shared among all circuitry present on the chip, especially on a small die. This causes the common chip ground to bounce with circuit switching activity. On-chip circuits that are referenced to the chip ground are affected only to a small extent. However, off-chip components interfacing with front-end blocks see a major portion of this ground-bounce because they are referenced to a different ground. Fig. 4 shows the narrow-band equivalent circuit of the output stage of an RFIC. I_n represents the equivalent RF current due to the on-chip circuitry flowing through supply and ground paths. A large capacitor C_{dcap} connected between chip supply and ground nodes provides a low impedance path for I_n. As shown in Fig. 4, L_{bs}, L_{bg}, Z_p and Z_s form a bridge network. The bridge is balanced when

$$\frac{\omega L_{bg}}{\omega L_{bs}} = \frac{Z_s}{Z_p}$$

Under balanced condition, load R_L is isolated from I_n. Hence, the portion of I_n received at the load (ground-bounce) depends on the extent of bridge imbalance and the magnitude of load impedance. Consequently, the ground-bounce due to other circuit blocks can be completely nulled by balancing the bridge. The value of C_c is chosen such that I_s sees only a real impedance of value very close to R_L. Exact estimation of bond wire inductance may not always be possible, so a few pins can be devoted for accurate bond wire characterization.

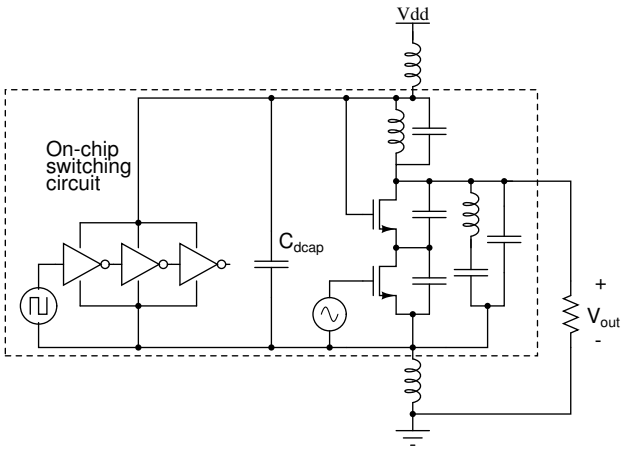
V. Simulation results

A. Stand-alone PA

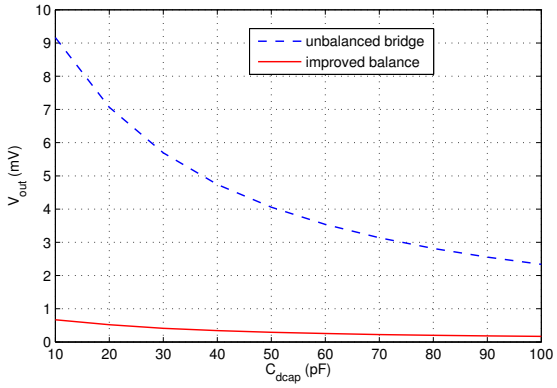
A class-AB nMOS cascode power amplifier is designed for 2.5GHz with 16dBm output P_{1dB} (Fig. 6). An additional capacitance of 5pF is added between gate and source nodes for all simulations to reduce Q of input network. A representative inductance value of 2nH with Q of 100 at 2.5GHz is used in place of a bond wire wherever applicable. The performance of the PA has been compared without bond wire, with one bond wire, with two bond wires in parallel and after applying matching and stabilization techniques discussed in section III (Fig. 7). Adding a supply decoupling capacitance degrades stability in the presence of bond wire unless some loss is added. A supply decoupling capacitance (C_{dcap}) of 30 pF is connected only in the last case along with a stabilizing resistor (R_d) of 10 ohms when L_{bg} and C_{bg} are added for matching. As shown in Fig. 7, input matching at the centre frequency is almost recovered by using the extra ground bond wire. The matching bandwidth ($S_{11} < -20dB$) with series resonance in the ground path is still 500MHz at 2.5GHz centre frequency, which is more than required for narrow-band applications. Global stability is demonstrated by the fact that $S_{11} < 0dB$ at all frequencies.

B. Impedance balancing

The same PA is now driven by an on-chip source while sharing supply and ground bond wires with a chain of three switching inverters. The bond wire at the output node does not affect bridge balance and has not been considered. The matching network is also removed for this simulation as it does not affect the illustration of this technique. Equal inductance values of 2nH have been used to represent both supply and ground bond wires. As per the discussion in the earlier section, the pull-up and pull-down impedances looking towards the PA from the load side should also be equal to achieve a balanced



(a)



(b)

Fig. 5. (a) PA with pull up and pull down impedance balanced (b) Effect of inverter switching on off-chip load for different values of supply decap (C_{dcap})

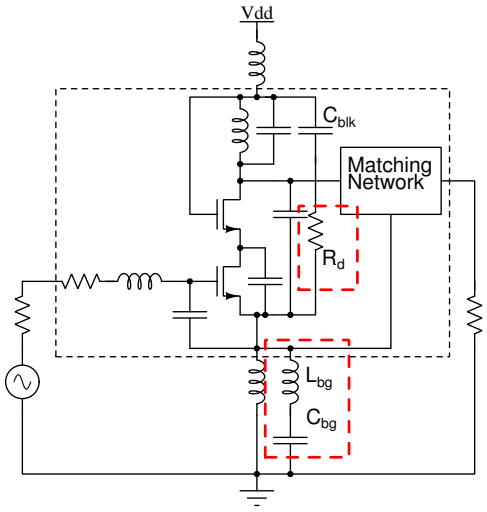


Fig. 6. Cascode PA with reduced ground-bounce

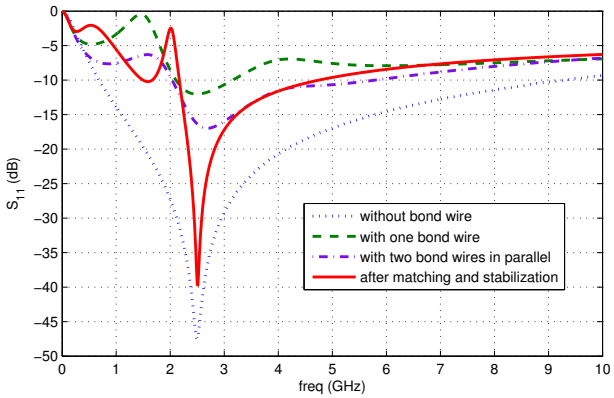


Fig. 7. Input reflection coefficient

bridge. As the parasitic capacitance of the transistor contributes to the load tank capacitance in the PA, the bridge is not balanced and switching of the inverters causes disturbances in the off-chip load. To tackle this issue, the tank circuit inductor is split into two parallel inductors (Fig. 5a). One inductor resonates with the capacitance between supply and output nodes while the other resonates with the capacitance looking downwards into the rest of the circuit. A capacitance of 10pF is added in series with the bottom inductor to prevent a dc short between supply and ground nodes. Though the impedances of the upper and lower tank circuits are not exactly equal, the disturbance injected due to the switching inverter chain is still much lower in this case, as depicted in the simulation results of Fig. 5b.

VI. Conclusion

Techniques to reduce ground-bounce in narrow-band RF front-end circuits were proposed. Addition of an extra ground bond wire with an off-chip capacitor recovers input matching without causing significant power or area overheads as with traditional approaches. Stability issues due to the presence of ground bond wire inductance were also tackled, as demonstrated with the example of an RF power amplifier. The output stage of the RFIC was treated as a bridge and the output impedance of the stage was restructured to reduce ground-bounce due to other on-chip circuits. Degradation in performance of the power amplifier was reversed by application of these techniques, as demonstrated by circuit simulations.

References

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