Multi-band RF Time Delay Element Based on Frequency Translation

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***Abstract*—Design of tunable multi-band time delay elements based on frequency translation is presented. The proposed topology exhibits time delay of multiple periods of the RF carrier. Two possible implementations of the proposed idea are presented and simulation results are shown for one such implementation. The implemented circuit exhibits an envelope delay of 2.5 ns with the RF carrier delay tunable from 0° to 360° in 45° steps in the 2.4 GHz ISM band.**

I. Introduction

A time delay element (TDE) is a circuit block that delays an input signal by a specified duration. A TDE is essentially a linear phase filter, in which the signal phase shift varies linearly with frequency. TDEs are mainly used in antenna beamforming systems, where the received signals are linearly combined with appropriate delays, so as to steer the antenna beam (gain) to an optimal direction [1].

Recently, TDEs are being used in circuitry to cancel self-interference in full-duplex wireless systems, wherein a wireless node transmits and receives in the same frequency and at the same time [2]. In Figure 1, an illustrative self-interference cancellation system is shown. Here, the signal from the transmitter antenna can reach the receiver antenna using multiple paths. In a typical wireless communication system, the transmit signal interfering at the receiver, referred to as self-interference, can be several orders of magnitude larger than the desired signal. If not suppressed, the self-interference will saturate the receiver chain and the intended receive signal cannot be recovered. Since the transmit signal is known, self-interference can be canceled by creating a weighted combination of transmit signals with different delays and subtracting from the received signal. For example, in Figure 1, $\hat{A}_1$ and $\hat{A}_2$ are the delayed and scaled versions of the transmit signals. The delays and gains are suitably chosen so that $\hat{A}_1 + \hat{A}_2 \approx A$. Since the amount of cancellation strongly depends on the delay mismatch between the interfering path and the cancelling path, circuits with a flat time delay profile across the entire frequency band of interest are desirable. Furthermore, to cancel self-interference received via multipath and reflections, the time delay should be tunable over a span of several time periods of the carrier frequency [3].

We now briefly describe current approaches to realize TDEs and their limitations.

Transmission Line Phase shifters (TLPS): TLPS or True Time Delay (TTD) cells [4] use lumped equivalents of transmission lines to achieve the required delay. An LC-based lumped equivalent of a transmission line has a cut-off frequency which is inversely proportional to its time delay. Hence, a large time-delay of the order of the time period of the carrier wave would require multiple LC sections, requiring larger chip area. Moreover, while this passive implementation of a TDE is highly linear, there is significant loss due to the low quality factor of on-chip inductors.

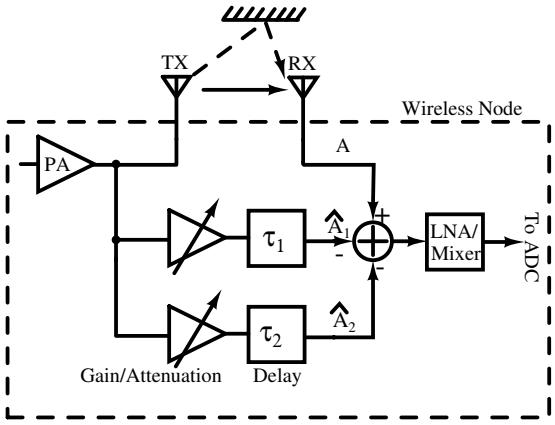
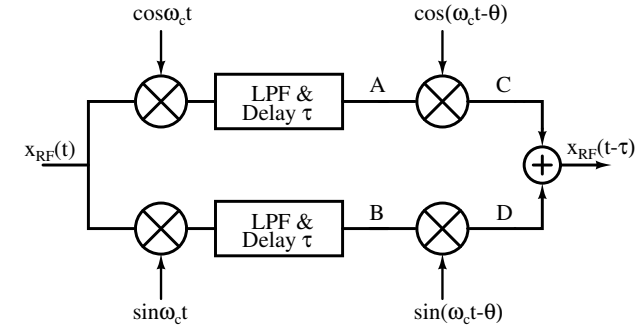


Fig. 1: An example of a self- interference cancellation system.

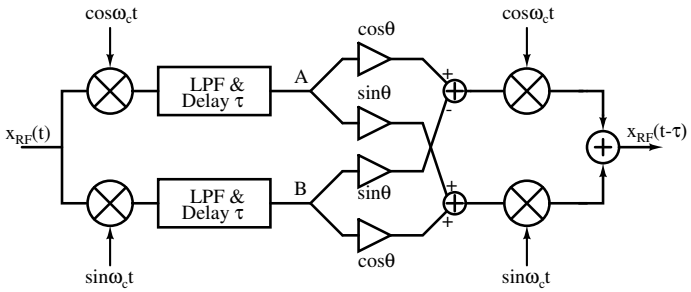
Reflection-type phase shifters (RTPS): The envelope of a narrowband RF signal varies at a much slower rate compared with the carrier. Therefore, the time-delayed signal can be approximated by simply delaying the carrier wave instead of the entire signal. Since the carrier is a sinusoid, a time shift equals a phase shift between 0 to 2π. However, this approximation becomes less accurate as the delay approaches several time periods of the RF carrier.

Based on the above principle, RTPS use lumped equivalent of a microwave coupler or circulator terminated with reactive impedance to tune the phase of an RF signal [5]. Based on the nature and magnitude of reactive impedance, the phase shift of the carrier can be controlled. However, such an implementation results in large silicon area, loss due to presence of inductors, and is not multi-band in nature.

Vector-modulation-based phase shifters: Active circuits based on the concept of vector modulation can be used to vary the phase of the signal carrier. Essentially, the RF signal is split into quadrature components and variable phase shift is obtained by controlling the gain of each component [6]. While these implementations are very compact, the presence of active circuits limits their linearity and noise performance. Moreover, since self-interference cancellation is a strong function of the matching of delays through various paths, the approximate approach of carrier phase shifting might result in poor cancellation across the entire frequency band.



(a) Central idea of the proposed time delay.



(b) One possible implementation of the proposed idea.

Fig. 2: Proposed Time delay element.

In this paper, we extend the idea of frequency translation for RF filtering [7] to realize area efficient tunable delay circuits with time delays of several time periods of the RF carrier signal. In Section II, the central idea and the resulting circuit topology are described. The circuit implementation and trade-offs between various design parameters are described in Section III. Simulation results are presented in Section IV.

II. Delay based on Frequency translation

Let $x_{RF}(t)$ denote a narrowband modulated signal [8] at a carrier frequency ω_c, *i.e.*,

$$x_{RF}(t) = a(t)\cos(\omega_c t + \phi(t)), \tag{1}$$

where $a(t)$ and $\phi(t)$ refer to the envelope and phase of the information signal respectively. The signal delayed by time τ is given by

$$\begin{aligned} x_{RF}(t-\tau) &= a(t-\tau)\cos(\omega_c(t-\tau)+\phi(t-\tau)) \\ &\overset{(a)}{=} a(t-\tau)\cos(\phi(t-\tau)+\omega_c t-\theta), \end{aligned} \tag{2}$$

where $\theta = \omega_c\tau \mod 2\pi$ and (a) follows since $\cos(x)$ is periodic with period 2π. This implies that a narrowband modulated signal can be delayed by the required time delay τ if its amplitude and phase are delayed by τ and the phase of the carrier is shifted by θ.

Figure 2(a) shows a block diagram illustrating one possible way to realize (2). The input RF signal is down-converted to baseband to obtain the envelope and phase information. Since most modern modulated signals have asymmetric frequency spectra about the origin, quadrature down-conversion is necessary [8]. The baseband signals are then low-pass filtered to suppress the content at higher frequencies generated due to mixing. Since a low-pass filter with cut-off frequency sufficiently higher than the signal bandwidth acts as a linear phase filter, it can be used to delay the envelope $a(t)$ (and the phase $\phi(t)$) by the desired amount. The time delay can be controlled by tuning the cut-off frequency of the low-pass filter. The delayed baseband envelope is again upconverted to the RF frequency by multiplying with carrier signals that have an additional phase shift θ. From (1), the signals at A and B in Figure. 2 are

$$x_A(t) = a(t-\tau)\cos(\phi(t-\tau)) \tag{3}$$

$$x_B(t) = -a(t-\tau)\sin(\phi(t-\tau)). \tag{4}$$

After upconversion and summing, the output of the delay element is

$$\begin{aligned} x_{RF}(t-\tau) = &[x_A(t)\cos(\theta) - x_B(t)\sin(\theta)]\cos(\omega_c t) \\ &+ [x_A(t)\sin(\theta) + x_B(t)\cos(\theta)]\sin(\omega_c t). \end{aligned} \tag{5}$$

A simplified implementation based on (5) is shown in Figure 2(b). From (5), we also observe that if $\cos(\theta)$ and $\sin(\theta)$ were replaced by A_1 and A_2 such that $\theta = \arctan(A_2/A_1)$, then the resulting signal would be a scaled version of $x_{RF}(t-\tau)$, *i.e.*$\sqrt{(A_1^2+A_2^2)}x_{RF}(t-\tau)$. A circuit implementation to obtain the attenuations A_1 and A_2 such that $A_1^2 + A_2^2 = 1$ is provided in [6]. The architecture in Figure 2(b) requires three summing blocks. Summing at baseband frequencies may add flicker noise to the signal and degrade signal-to-noise ratio. Moreover, since the summation is easier if done in current domain, any V-to-I conversion will further worsen non-linearity and noise. Figure 3 shows an alternative implementation that requires only one summer at the output, but at the expense of using two additional mixers. Since passive mixers are highly linear and less noisy [8] when compared to active mixers, consuming extra power to drive the additional mixers may often be acceptable.

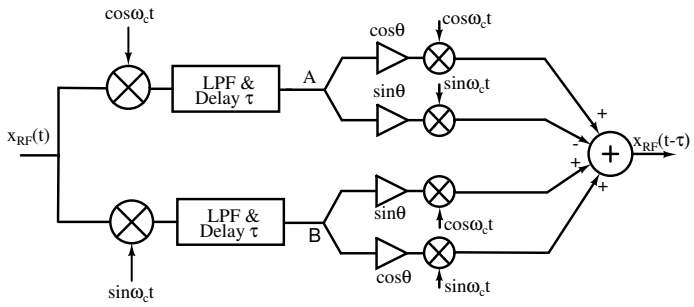


Fig. 3: Alternative implementation of the proposed idea.

Since the time delay realized by the circuit is independent of the RF signal frequency, this topology can be used for multi-band applications. In addition to the desired time shifted signal, the output may also contain components around harmonics of the carrier frequency depending on the mixer topology. However, these harmonics can be easily suppressed at an architecture level in most narrowband systems.

III. Circuit Implementation

The proposed architecture in Figure 3 is implemented in a UMC 130 nm CMOS process. Figure 4 shows a schematic

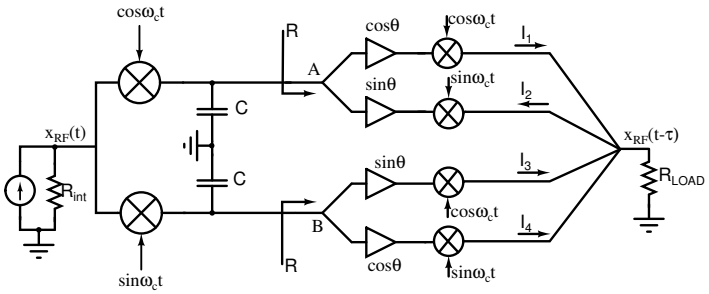


Fig. 4: Time delay circuit.

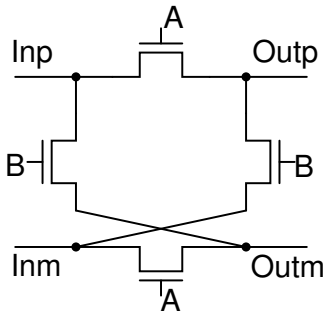


Fig. 5: Circuit with gain of $+1, 0, -1$.

representation of the implemented circuit. It is easy to obtain gains of $\{+1, 0, -1\}$ in a differential system by using switches as shown in Figure 5, without compromising linearity and noise performance. Therefore, discrete tuning in steps of $45°$ is chosen for illustration of the proposed idea. When A is logic high and B is logic low in Figure 5, the equivalent gain between input and output is $+1$. Similarly, when B is logic high and A is logic low, the effective gain is -1. When both A and B are logic low, the effective gain from input to output is 0. The phase of the carrier is controlled by changing the gain through each path.

Current driven passive mixers are used for frequency translation as they are highly linear and offer low flicker noise due to the absence of DC current [8]. All the switches in the mixers are realized using nMOS transistors for ON resistance of $\approx 13\Omega$, and are driven by rail-to-rail signals with 25% duty cycle. The input signal to the phase shifter is a current source with internal resistance of 2 kΩ, representing the current tapped from the output of PA in Figure 1. The output is terminated with a differential resistance of 50Ω, exemplifying the case when the time delay circuit is connected to the input of a receiver that is matched to 50Ω.

The time delay applied to the down-converted baseband signal (envelope) is equal to RC, where C is the filter capacitance and R is the equivalent looking-in resistance of the succeeding circuitry, both as shown in Figure 4. The maximum and minimum time delay that can be obtained from the circuit are solely determined by the cut-off frequency of the LPF which is given by $\frac{1}{2\pi RC}$. If the cut-off frequency is comparable to or lower than the bandwidth of the down-converted baseband signal, the time delay shows significant variations with frequency. On the other hand, a higher cut-off frequency reduces the attenuation of high-frequency mixing components, especially at around twice the carrier frequency. Any components present at around twice the original RF frequency will fold back down to the desired RF band in the second set of mixers.

In this design, an example of a typical WLAN system has been chosen, with RF channel bandwidth of 20 MHz and RF carrier frequency between $2.4 - 2.5$ GHz. Considering trade-offs in circuit design as well as size of realizable components for given impedance levels, a convenient value of $RC \approx 2.5$ ns was chosen, which corresponds to ≈ 6 cycles delay of the RF carrier. In practice, envelope delay can be tuned over a large range using using switched capacitor banks, with fine tuning accomplished through the use of varactors. The 25% duty-cycle signals driving the mixers are generated using a divide-by-2 circuit as described in [9].

IV. Simulation Results

The circuit designed as per the above specifications is simulated in Spectre. Fig. 6 shows the quadrature clocks applied to the mixers. The divide-by-2 and drive circuitry draws an average current of 8.2 mA from a 1.2 V power supply at the input clock frequency of 4.9 GHz. Figure 7 shows the phase as a function of RF frequency for different phase settings. For each setting, apart from the desired phase shift, the circuit also contributes a constant phase shift of $\approx 10°$ due to other circuit effects such as parasitic capacitance. The envelope delay is ≈ 2.5 ns.

Figure 8 shows the noise current spectral density at the output. Thermal noise of the upconverting mixers contributes towards 60% of the output noise, while the rest is due to the down-conversion mixers and the gain element. The output frequency components around the third harmonic of the carrier (7.35 GHz in this case) are 10 dB below the desired signal. These can be easily suppressed elsewhere in most narrowband systems. Table 1 summarizes these simulation results and compares them with other implementations. The output frequency components around the third harmonic of the carrier (7.35 GHz

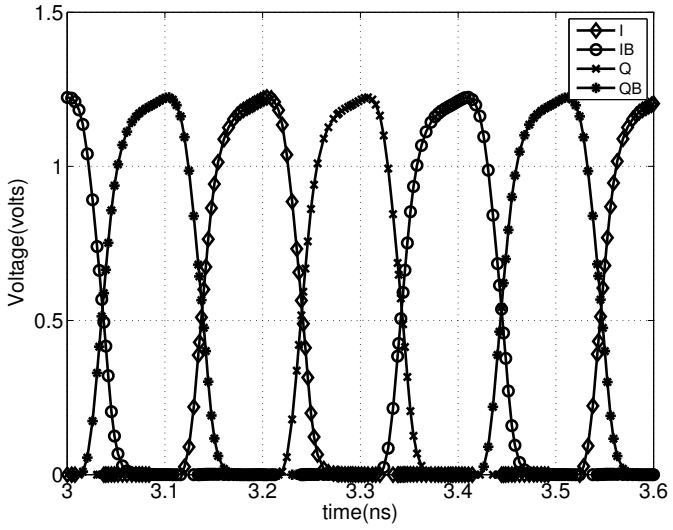


Fig. 6: In-phase and Quadrature carrier waveforms.

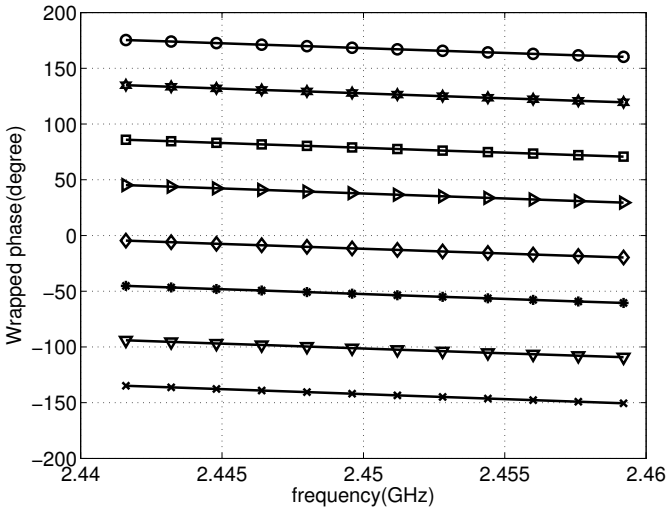


Fig. 7: Wrapped phase versus input signal frequency for different phase settings.

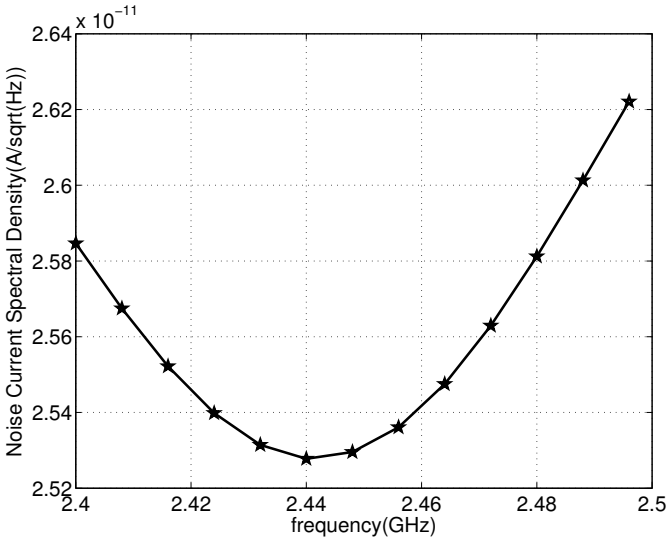


Fig. 8: Output noise current density.

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V. Conclusion

The concept of frequency translation for RF filtering is extended to the design of area-efficient time delay elements with delays of the order of several periods of the RF carrier. The proposed architecture is also capable of operating across multiple frequency bands. Simulation results at the circuit level show competitive performance. Circuit implementation using MOSFET switches is likely to benefit heavily with down-scaling of CMOS technology in terms of area and power consumption.

TABLE I: Result summary and comparison

	This work	[5]	[10]	[6]	[11]
Frequency (GHz)	2.4-2.5	2.4-2.5	2.6	1-2.1	2.5-3.2
Phase tuning range (degree)	360	120	96	90	360
Min. Gain (dB)	-13	-5	-3.8	4.8	-2.5
Max. Noise figure (dB)	–	23.8	12.8	15.1	7.1
Power (mW)	9.84	111	31.5	4.2	60
Area (mm^2)	0.10 (estimated)	0.357	0.364	0.06	4.16
Circuit topology	Frequency translation	RTPS	TLPS	Vector sum	switched TL
Technology	130nm CMOS	180nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS

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