EE6320 Homework 5: Due Sunday 02/05/2021

1. A class-A power amplifier is shown in figure 1 below. The device bias current chosen to be exactly equal to the peak signal current so that the transistor just touches cut-off at the negative end of the input signal cycle and just touches linear region at the positive end of the input signal cycle. Neglect the saturation voltage $V_{D,SAT}$ of the transistor in relation to V_{DD} (so that the drain output voltage V_X swings between 0 and V_{DD}). Assume that L_1 is very large and that the matching network is ideal.

   (a) Prove that the drain efficiency of the class-A PA is exactly 50%

   (b) Prove that other ("wasted") 50% of the supply power is dissipated in M_1.

2. A cascoded class-A power amplifier is shown in figure 2 below. Assume that M1 and M2 are biased such that M1 is biased at the edge of triode region. Determine the maximum possible drain efficiency. In this problem, do not ignore the saturation voltage $V_{D,SAT}$ of the transistors. Assume that L_1 is very large and that the matching network is ideal.

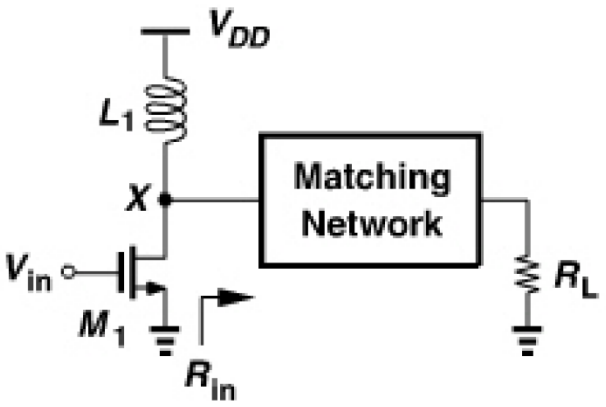

Figure 1

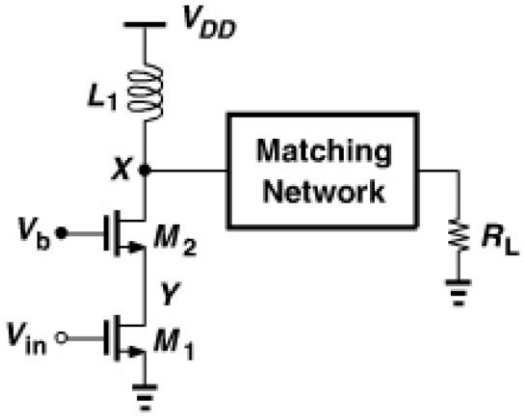

Figure 2