EE6320 Design Project 3: VCO Design – due 11:59pm Sunday 24/05/2019

In this project, you are asked to design a fully-differential LC-VCO that meets or exceeds the specifications given below. Use the IBM 130nm CMOS process parameters used by you earlier. Design the VCO for the following specs:

- f_0 = 4.6 to 5.2GHz (600 MHz tuning range)
- V_{DD} = 1.3V
- Minimum VCO output amplitude (on each side) = 1V
- Phase noise specification: -117dBc/Hz @ 1MHz offset and -140dBc/Hz @ 20MHz offset
- Maximum number of inductors = 1. In the case of a nmos-only or pmos-only VCO, the two sections of a symmetrical centre-tap inductor is considered as 1 inductor, with the centre tap connected to V_{DD}/ground.
- Tuning should be done using a combination of MOS-transistor-based varactors for fine-tuning and a binary weighted switched-capacitor bank for coarse-tuning. The fine-tuning circuit should exhibit a nominal K_{VCO} of 200MHz/V over the usable tuning range.
- Minimise overall power consumption

Notes:

1. Include and discuss your VCO design procedure and architecture choice in your report. Remember to include the K_{VCO} plot as well as VCO transient simulation output.