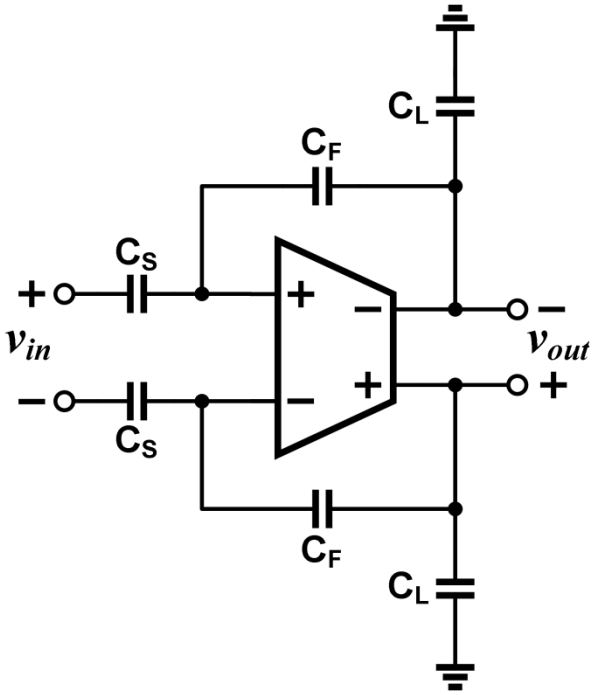
Assignment #5 **Deadline: 10th May, 11:59pm**

Problem-1:

Design the fully differential feedback amplifier shown in the below figure. The specifications for the closed loop system are given in the table below.



Technology	**EE5320 130nm CMOS**
V_{DD}	**1.3V**
Closed loop gain	**4**
C_L	**2pF**
Settling time	**≤ 5ns**
Settling error (Static + Dynamic)	**≤ 800μV**
Maximum differential input step	**200mV**
Power consumption	**Minimum**

(a) For the above closed loop system, assuming an appropriate model for the amplifier, write the expression for $V_{out}(s)/V_{in}(s)$ and its DC gain, poles and zeroes. If a differential input step of $V_{in,step}$ is applied at t=0, write the expressions for the differential output response $V_{out}(t)$ and absolute values of static and dynamic error voltages.

(b) For C_S= 2pF, derive the required -3dB bandwidth of the closed loop system, the open loop DC gain of the amplifier block and the value of C_F from the given specifications. Include the parasitic capacitance due to the amplifier's input FETs. Show all relevant calculations and justify your choices.

(c) From the specifications derived in (b), design the differential amplifier. Use a single ideal external current source. Justify the topologies of main amplifier, biasing and CMFB circuitry and explain the

sizing based on the results of (b). Simulate to verify performance. Clearly drawn amplifier schematic along with tabulated device sizes, currents and g_m of all devices should be shown.

(d) Plot the differential AC magnitude and phase of $V_{out}(s)/V_{in}(s)$ with clearly marked DC Gain and -3dB bandwidth.

(e) Plot the magnitude and phase of the differential loop-gain with clearly marked DC Gain, unity gain bandwidth and phase margin.

(f) Plot the common mode loop-gain AC response(s) (magnitude and phase) with clearly marked DC Gain, unity gain bandwidth and phase margin.

(g) Plot the positive and negative differential step responses of the closed loop system with maximum input differential step and clearly marked initial and final voltages, settling time and settling error on a separate zoomed-in plot. Use initial conditions as necessary.