Assignment: #4

Due Date: Sunday Mar. 22, 2020, 11:59pm

For circuit design, use the 130nm CMOS models given to you.

PROBLEM 1. Design a differential amplifier with DC gain 25 V/V and -3 dB bandwidth of 75 MHz. Schematic of the differential amplifier is shown below with common mode feedback loop using amplifier **A**. The common mode feedback loop should have phase margin $\geq 70°$.

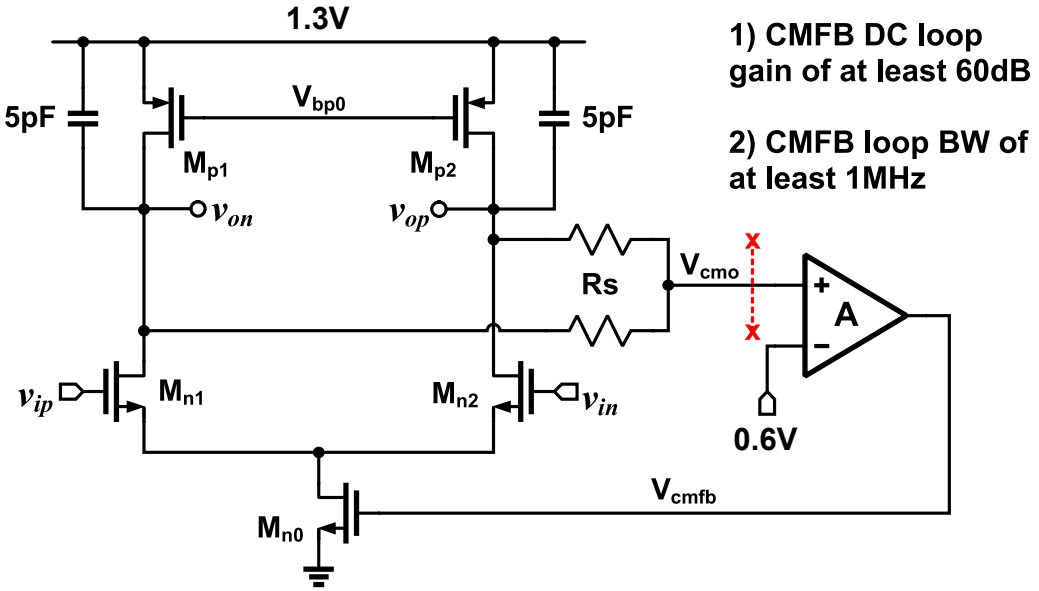
(a) Derive the transfer function $(V_{op}(s) - V_{on}(s))/(V_{ip}(s) - V_{in}(s))$ for differential amplification with dominant parasitic capacitors for MOSFETs. Use the database generated in previous assignment to find device sizes. Verify the performance in simulation. Revise device sizes through simulation or modeling to achieve the desired performance.

(b) Design amplifier for common mode feedback loop with $\leq 1/4^{th}$ current in the main amplifier. Close the common mode feedback loop and check the stability of the feedback loop (loop gain and phase margin) using a 'VSTB source' or 'iProbe' at the dashed location in the schematic and 'STB' analysis. Crosscheck hand calculated poles and zeros with simulated ones using 'PZ' analysis.

(c) Stabilize the common mode feedback loop using Miller compensation and plot final loop gain and phase margin.

(d) Replace the 'VSTB source' or 'iProbe' with inductor (1H) and capacitor (1F) as discussed in class and check for loop gain and phase margin using AC analysis. AC analysis results should be in close approximation with stability analysis results.

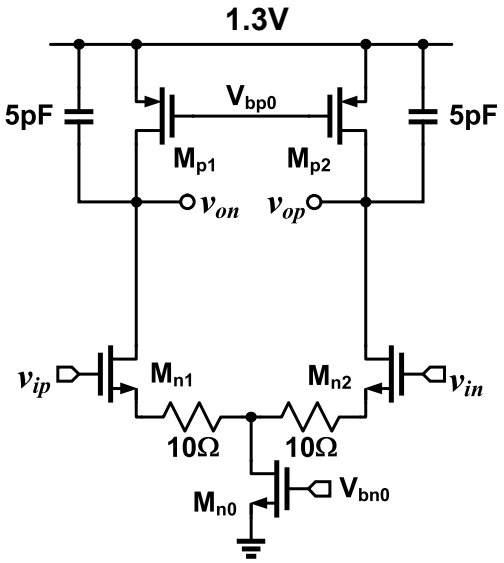
(e) Plot input-to-output differential AC response and clearly indicate the DC gain, -3 dB bandwidth, and unity gain bandwidth.



PROBLEM 2. Use devices sizes and biasing voltages for the differential amplifier shown below as obtained in Problem 1. Set the input common mode voltage for M_{n1}, M_{n2} such that all MOSFETs are biased in saturation. The CMFB is the same as in Problem 1 above.

(a) Find input-to-output differential voltage transfer function. Plot magnitude and phase for voltage transfer functions.

(b) Find noise transfer functions for different noise sources to the output. Simulate for total output and input referred noise spectral density. Check the %age contribution of each noise source when output noise is integrated for 0.01-100 MHz.



PROBLEM 3. Use devices sizes and biasing voltages for the differential amplifier shown below as obtained in Problem 1. Split current source M_{n0} (in Problem 1) equally between M_{n00} and M_{n01}. Set the input common mode voltage for M_{n1}, M_{n2} such that all MOSFETs are biased in saturation. The CMFB is the same as in Problem 1 above.

(a) Find input-to-output differential voltage transfer function. Plot magnitude and phase for voltage transfer functions.

(b) Find noise transfer functions for different noise sources to the output. Simulate for total output and input referred noise spectral density. Check the %age contribution of each noise source when output noise is integrated for 0.01-100 MHz.