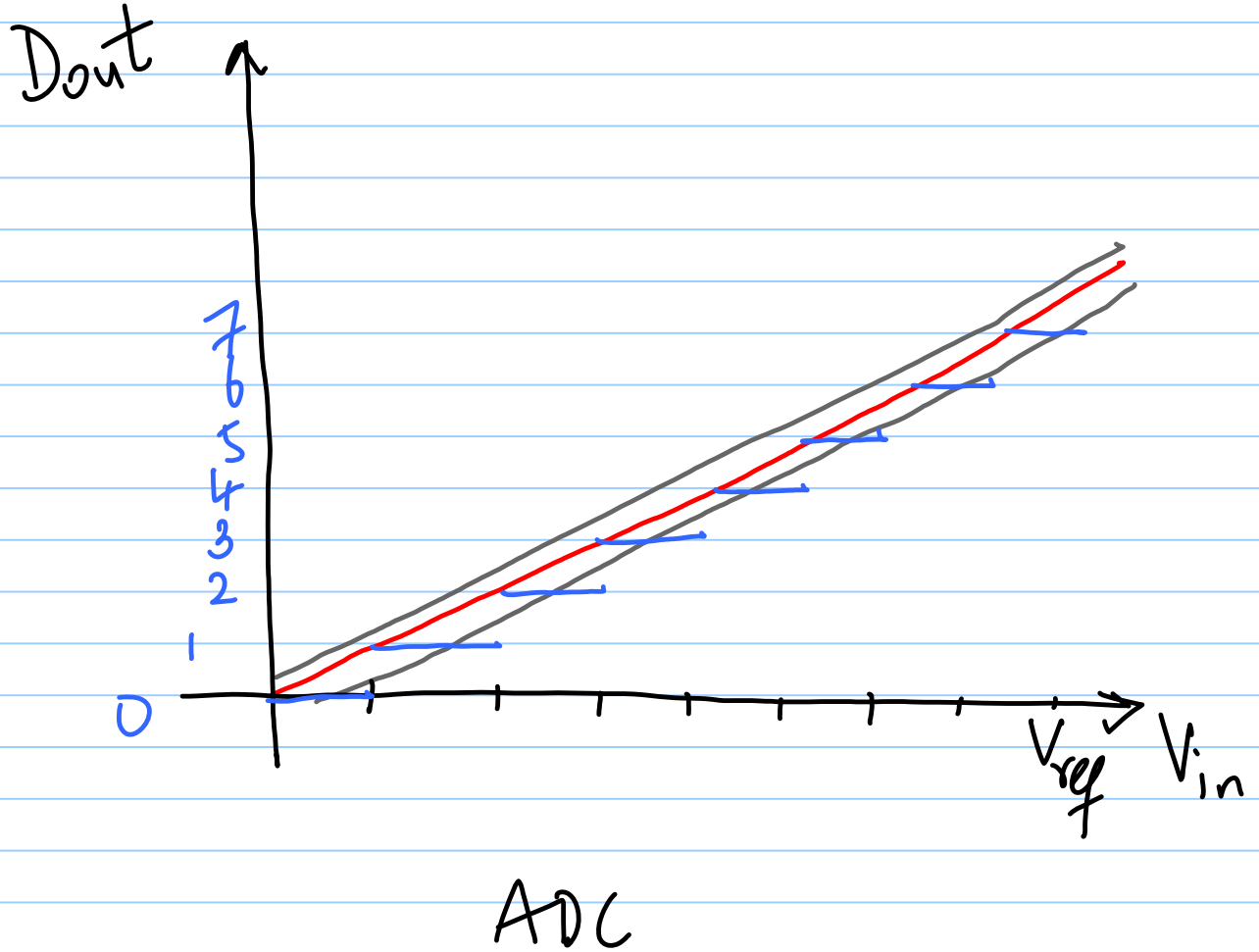
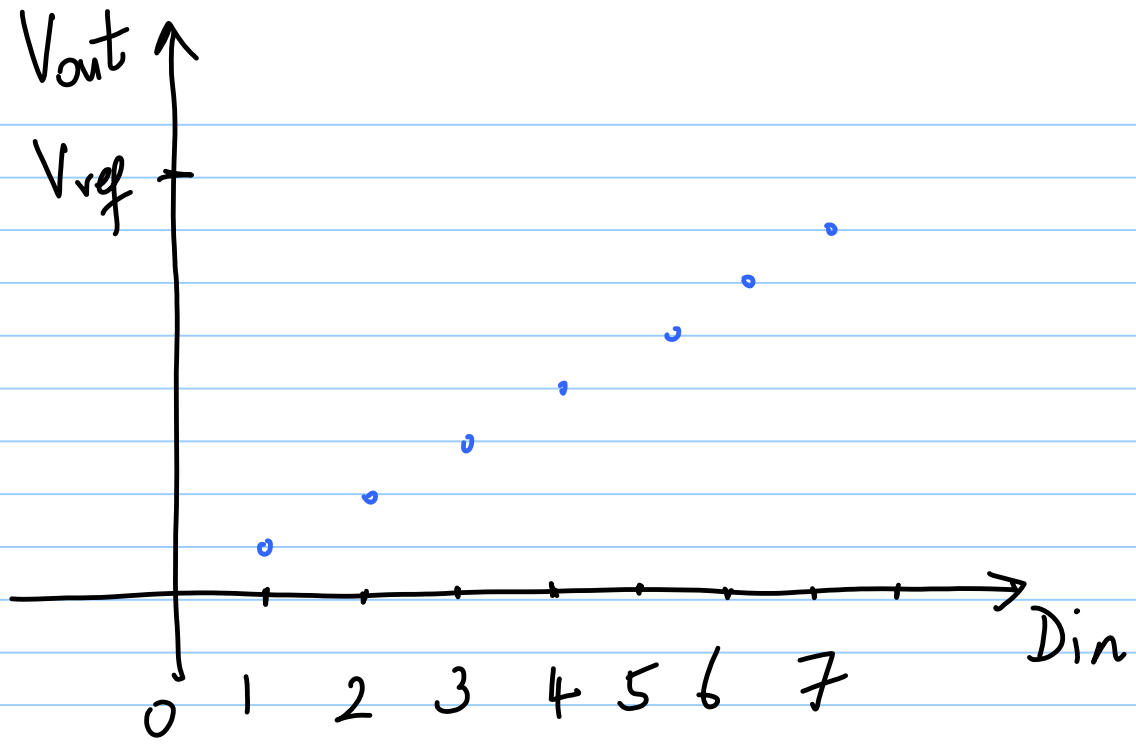
16/04/2019

Lecture 40

Non-idealities in ADCs & DACs



ADC



Simple Errors

1) offset in the wire:

All ADC transition levels move by Voff. } offset errors.
" DAC output " " " "

2) Equally sized steps, but different from $\frac{V_{ref}}{2^n}$

$\frac{V_{ref}}{2^n} \neq V_{LSB}$ { V_{ref} : intended ref. voltage }

Actual $V_{ref}' = 2^n V_{LSB}$ { Gain error }

Complex Errors

* Non-uniform steps
* You will lose a step (No longer 2^n thresholds) if error $> \pm \frac{1}{2} \frac{V_{ref}}{2^n}$ or $\pm \frac{1}{2} V_{LSB}$

1) Integral Non linearity error (INL)

$$V_{ADC}[k] \neq \frac{V_{ref}}{2^n} k$$

$$INL[k] = \frac{V_{ADC}[k] - \frac{V_{ref}}{2^n} \cdot k}{V_{ref}/2^n}$$

If $|INL| < \frac{1}{2} LSB$: no missing bit for all k

2) Differential Nonlinearity error:
(DNL)

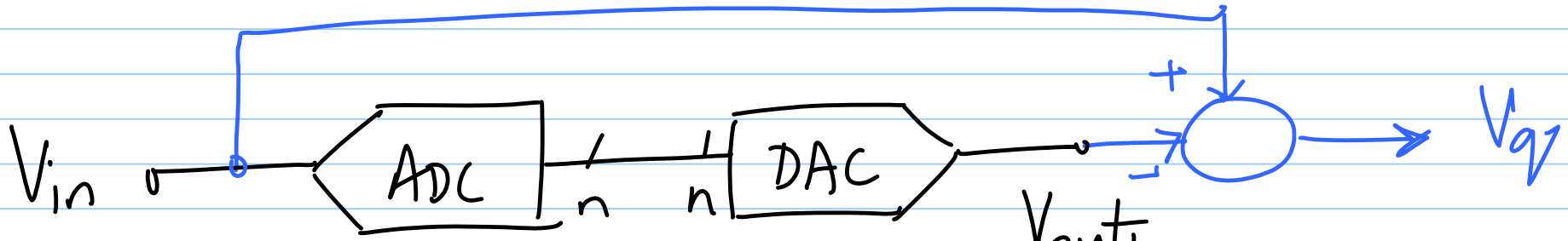
$$DNL[k] = \frac{V_{ADC}[k] - V_{ADC}[k-1] - \frac{V_{ref}}{2^n}}{V_{ref}/2^n}$$

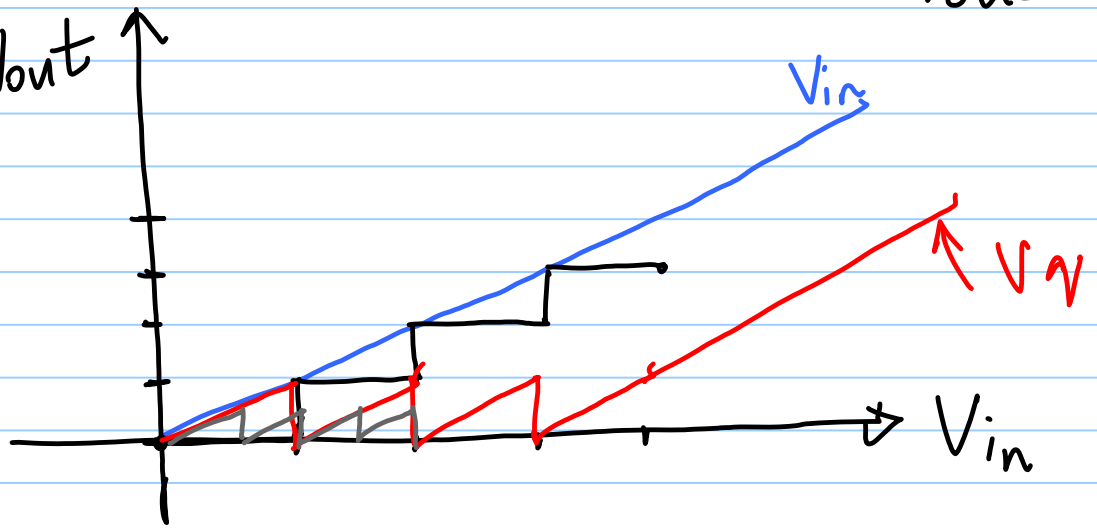
LSBs

If $|DNL[k]| < \pm 0.5$ LSB for all k, no missing bits

$$DNL[k] = INL[k] - INL[k-1]$$

DNL & INL are static errors.





as n ↑, energy in V_q reduces.