EE6240 Design Project 3: VCO Design – due Friday 08/11/2013

In this project, you are asked to design a fully-differential LC-VCO that meets or exceeds the specifications given below. Use the IBM 90nm CMOS BSIM4 process parameters supplied to you. Use the scalable inductor model supplied to you in the LNA project to model all inductors in your circuit; no ideal inductors are allowed! Design the VCO for the following specs:

- f_0 = 4.6 to 5.2GHz
- V_{DD} = 1.2V
- Minimum VCO output amplitude (differential) = 0.8V
- Phase noise specification: -97dBc/Hz @ 100kHz offset and -146dBc/Hz @ 20MHz offset
- Maximum number of inductors = 2
- Tuning should be done using a combination of MOS-transistor-based varactors for fine-tuning and a binary weighted switched-capacitor bank for coarse-tuning. The fine-tuning circuit should exhibit a nominal K_{VCO} of 50MHz/V over the usable tuning range.
- Design a VCO buffer to produce 0-V_{DD} swing across two single-ended load capacitors of 100fF each
- Minimise overall power consumption

Notes:

1. Include and discuss your VCO and VCO buffer design procedure and architecture choice in your report. Remember to include the K_{VCO} plot as well as VCO transient simulation output.