Lecture 38: Analog & RF Layout - II

a) matching environment:

![Diagram](diagram)

- Metal lines can affect parasitic cap to device nodes!

e) 45° lines:

![Diagram](diagram)

- Help with charge winding at corners
- Improve electromigration effects

f) maintain symmetry in routing (differential)

- e.g.

![Diagram](diagram)

- Passive Devices
  - Resistors:
    - Polysilicon Rs: *small Rs, high linearity*
    - Low cap to substrate
    - Smaller mismatches
$p^+/n^+ S-D$ diffusion $R_s$ (silicide or salicide)

- Low to medium $R_s$ (3-5kΩ)
- Very sensitive to process, temp (depends on doping level)

Non-silicided resistors

- Medium $R_s$ (50-100kΩ)
- Sensitive to process, temp

n-well resistors

- Large $R_s$ (few kΩ)
- Process, temp sensitive
- Large cap to substrate (don't use in RF path)

Very large $R_s$ - use NMOS/PMOS with W/L << 1!

- Process, temp sensitive
- Voltage sensitive
- Can exhibit "flicker noise"

⇒ For $R_{(oc)}$ matching, use identical units with same orientation placed in series or parallel

E.g.

\[ \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \]
say \( \text{gain} = -2, \quad R_2 = 2R_1 \)

\[
\begin{array}{c}
\frac{R_2}{R_1} \times \frac{R_1}{R_2} = 1
\end{array}
\]

- \( C, L \) have been covered before
- very important for RF

4) Transistor layout:

- parameters in schematic & layout:
  \( W = \) total width of device
  \( L = \) length of device
  \( n_f = \# \text{ of fingers} \)
  \( m = \text{multiplier (not factored into } W) \)

- e.g. \( W = 10 \mu m \) \( n_f = \frac{W}{n_f} = \frac{10 \mu m}{5} = 2 \mu m \)
  \( L = 0.18 \mu m \)

- \( n_f = 5 \)
  \( m = 2 \Rightarrow \text{effective } \frac{W}{L} = 2 \times 10 \mu m = 0.18 \mu m \)
- $n_f \uparrow \Rightarrow R_g, C_m \downarrow$
  - faster transistor
  - lower $R_g$ noise
- $n_f \& m$ allow setting of aspect ratio
- For devices in signal path, try to follow:
  \[ 1 \text{ mm} < W_f < 5 \text{ mm} \]
  - $R_g$ is large
  - parasitics/finger are large

- model limits max $W, L$ in schematic/layout
  - use $m$ to increase $W$ further
- $m \& n_f$ can also affect shape
  - e.g., $m = 9$

- may layout a bias device this way to fit into overall layout plan
5) Metal Routings:

- lower metals - larger cap to sub
  \(\text{M}_1, \text{M}_2\) - larger \(\ell\) (thinner, \(\text{Al}\))

- middle metals - lower cap to sub
  \(\text{M}_3, \text{M}_4\) - larger \(\ell\) (thinner, \(\text{Al}\))

- higher metals - lower \(\ell\) (thicker and/or \(\text{Cu}\))
  \(\text{M}_5\) and/or \(\text{M}_6\) - more fringing leads to more cap to sub

\[\rightarrow\] DC signals - \(\text{M}_1, \text{M}_2\)

analog, RF, clock signals - \(\text{M}_4\) (and \(\text{M}_3\), if necessary)

VDD, GND, high-current lines - \(\text{M}_5, \text{M}_6\) (thick metal)

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**Antenna Effect:**

Large metal sheet can build up charge during etching. It can breakdown gate.

- add a discontinuity (e.g., go to different metal and come back)
- add a reverse biased diode to prevent large voltage buildup
- antenna rule check is part of physical verification
Density:
Process requires minimum densities of diff. layers to maintain integrity
E.g. $M_1 - M_4$ (lower metals) ~ 90%.

Typical det ~ 20% or less

\[ \begin{array}{ccccccc}
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\end{array} \]
\[ = \text{dummy metal fill} \]

\[ \Rightarrow \text{adds extra cap parasitic} \]

Intensive det \(\Rightarrow\) use "auto fill" (i.e. random)
E.g. digital std. cells, control lines, bias det etc.

\* RF det: use "custom fill"
\(\Rightarrow\) manual fill to maintain symmetry
E.g. diff. lines

\[ \begin{array}{ccccccc}
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\end{array} \]

\* RF inductor: avoid fill (foundry can give waiver)
Foundry requires these checks before fab:

- DRC
- EDA

Your responsibility:

- LVS
- ERC
- LPE