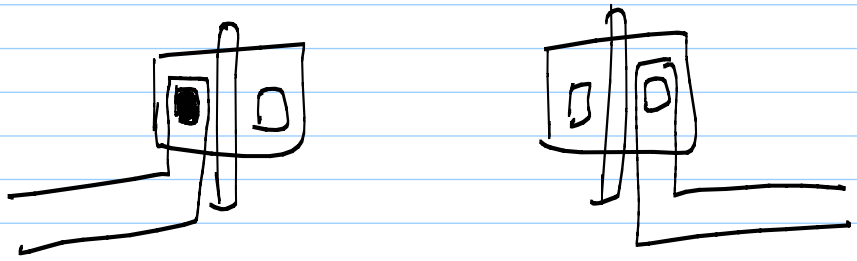
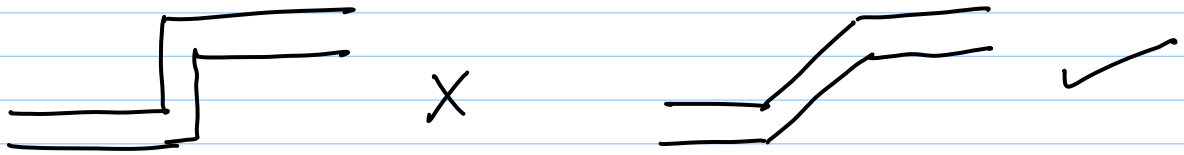
Lecture 38: Analog & RF Layout – II

d) matching environment:



metal lines can affect parasitic cap to device nodes!

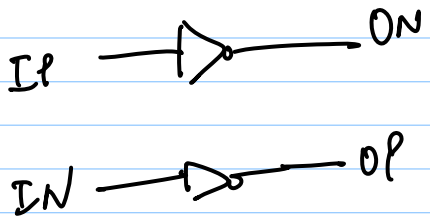
e) 45° lines:

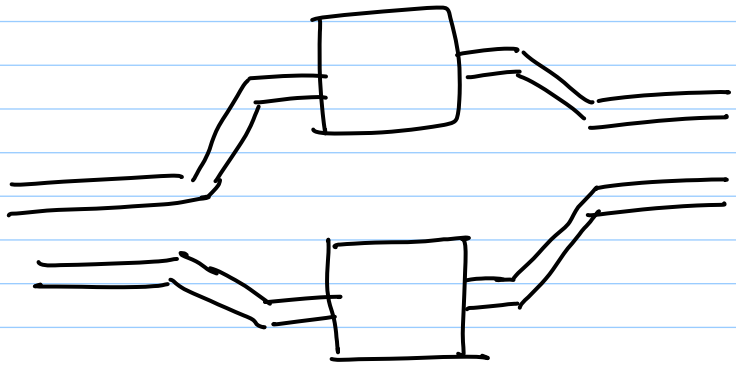


→ help with charge crowding at corners
→ improves electromigration effects

f) maintain symmetry in routing (differential)

e.g.





4) Passive Devices

Resistors:

polysilicon Rs
* small Rs, high linearity
* low cap to substrate
* smaller mismatches

p+/n+ S-D diffusion Rs (silicide or salicide)

* low to medium R_s (3-5 Ω/□)
* very sensitive to process, temp (depends on doping levels)

non-silicided resistors

* medium R_s (50-100s of Ω/□)
* sensitive to process, temp

n-well resistors

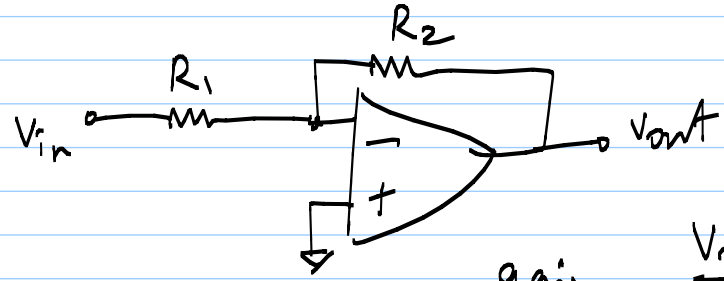
* large R_s (few kΩ/□)
* process, temp sensitive
* large cap to substrate (don't use in RF path)

very large R_s – use NMOS/PMOS with W/L << 1 !

* process, temp sensitive
* voltage sensitive
* can exhibit "flicker noise"

→ for R (or C) matching, use identical units with same orientation placed in series or parallel

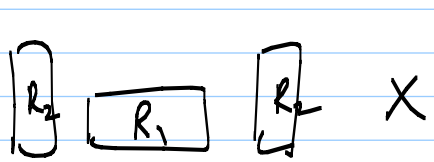
e.g.

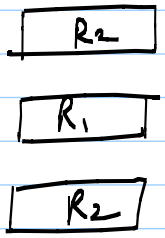


gain $\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$

Say gain $= -2$, $R_2 = 2R_1$

$R_1 \equiv$ 



X


✓

C, L → have been covered before

→ very important for RF

4) Transistor layout:

parameters in schematic & layout:

W = total width of device

L = length of device

n_f = # of fingers

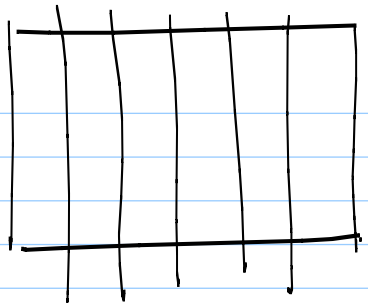
m = multiplier (not factored into W)

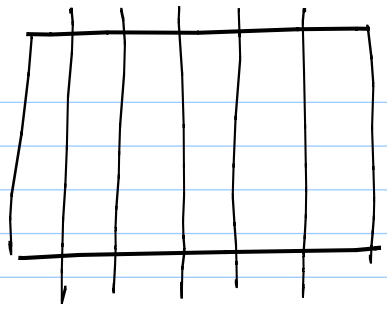
e.g. $W = 10\mu$, $L = 0.18\mu$, $n_f = 5$, $m = 2$

$W_f = \frac{W}{n_f} = \frac{10\,\mu m}{5} = 2\,\mu m$

= width of each finger

$m = 2 \Rightarrow$ effective $\left.\frac{W}{L}\right|_{tot.} = \frac{2 \times 10\mu}{0.18\mu}$





* $nf \uparrow \Rightarrow r_g, C_{db} \downarrow$
  - → faster transistor
  - → lower r_g noise
* nf & m allow setting of aspect ratio
* For devices in signal path, try to follow:

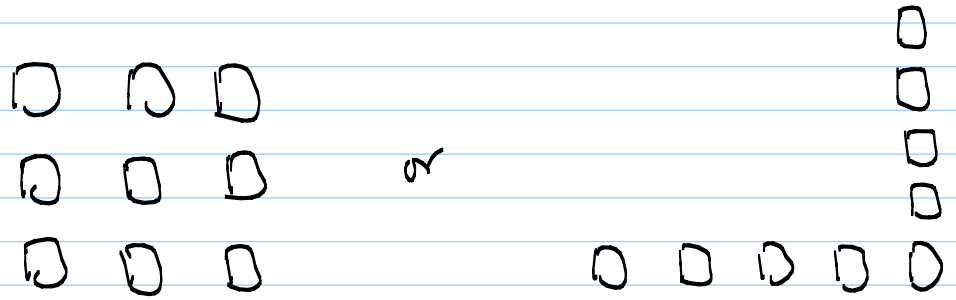
$$1\mu m < W_f < 5\mu m$$

W_f too small → parasitics/finger are large

W_f too large → r_g is large

* model limits max W, L in schematic, layout
  - → use m to increase W further
* m & nf can also affect shape

e.g. m = 9



or

may layout a bias device this way to fit into overall layout plan

5) Metal Routings:

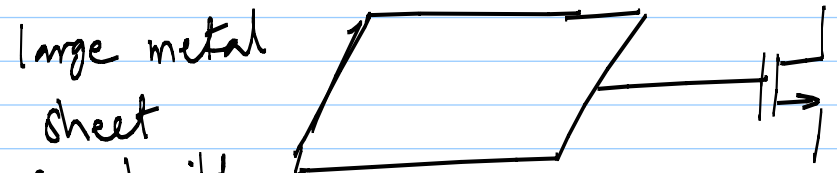
* lower metals (M_1, M_2) – larger cap to sub
  – larger ρ (thinner, Al)
* middle metals (M_3, M_4) – lower cap to sub
  – larger ρ (thinner, Al)
* higher metals (M_5 and/or M_6) – lower ρ (thicker and/or Cu)
  – more fringing leads to more cap to sub

→ DC signals – M_1, M_2

analog, RF, clock signals – M_4 (and M_3, if necessary)

VDD, GND, high-current lines – M_5, M_6 (thick metal)

Antenna Effect:



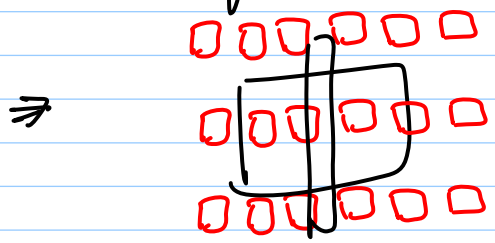
* add a discontinuity (e.g. go to different metal and come back)
* add a reverse biased diode to prevent large voltage buildup
* Antenna rule check is part of physical verification

Density :

Process requires minimum densities of diff. layers to maintain integrity

e.g. $M_1 - M_4$ (lower metals) ~ 90%.

typical dct ~ 20% or less



⇒ □ = dummy metal fill

⇒ adds extra cap parasitic

intensitive dcts ⇒ use "auto fill" (i.e. random)

e.g. digital std. cells, control lines, bias dcts etc.

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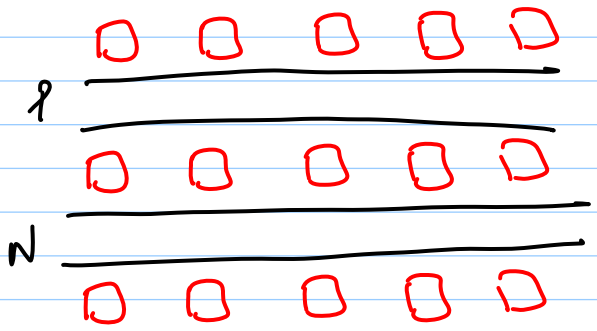
* RF dcts : use "custom fill"

⇒ manual fill to maintain symmetry

e.g. diff. lines



* RF inductors : avoid fill (foundry can give waiver)

Foundry requires these checks before fab:

- ⇒ DRC
- ⇒ Density

Your responsibility:

- → LVS
- → ERC
- → LPE