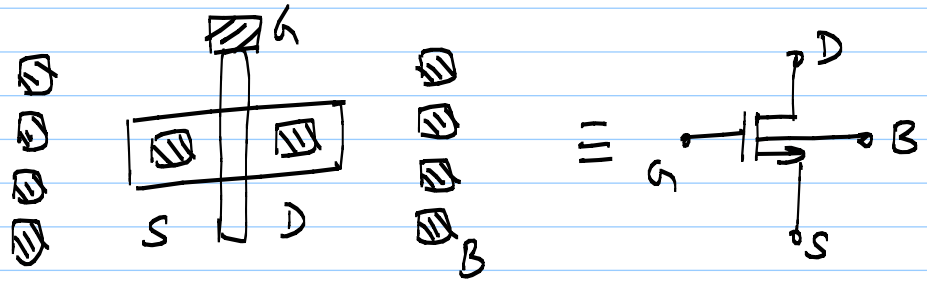
# Lecture #37: Analog & RF Layout

Note Title 7/6/2011

**Layout:** Geometries that appear on masks used in fabrication ⇒ top view of the devices and associated connections (routings)

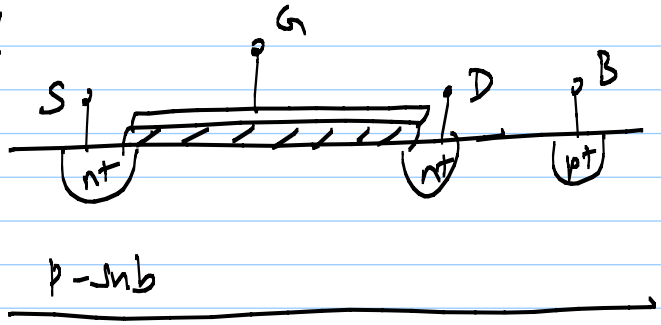
top view of a MOSFET (layout)




**reminder:** MOSFETs are 4-terminal devices

→ Bulk (substrate) contacts are critical!

**Side view** (conceptual):




Why should you know layout? (and why not let the layout engineer take over completely)?

→ Designer has ultimate responsibility

→ RF circuits are very sensitive to layout

* design & layout go together

* be aware of noise-sensitive & noise-producing circuits in and around your circuit location
* time: only ~50% time spent in design
  other 50% time — layout
* several iterations are common for sensitive circuits ⇒ increases design cycle time
* may identify weaknesses of design

General Considerations:

→ Design Rules: mainly limited by lithography (L) or processing (P) constraints

* minimum widths (P) – e.g. metal line, device etc.
* min. spacing (L) – e.g. metal-metal, poly-active
* min. enclosure (P) – e.g. metal over contact/via
* min. extension (P) – e.g. gate poly beyond active

poly = polysilicon (gate); active = diffusion

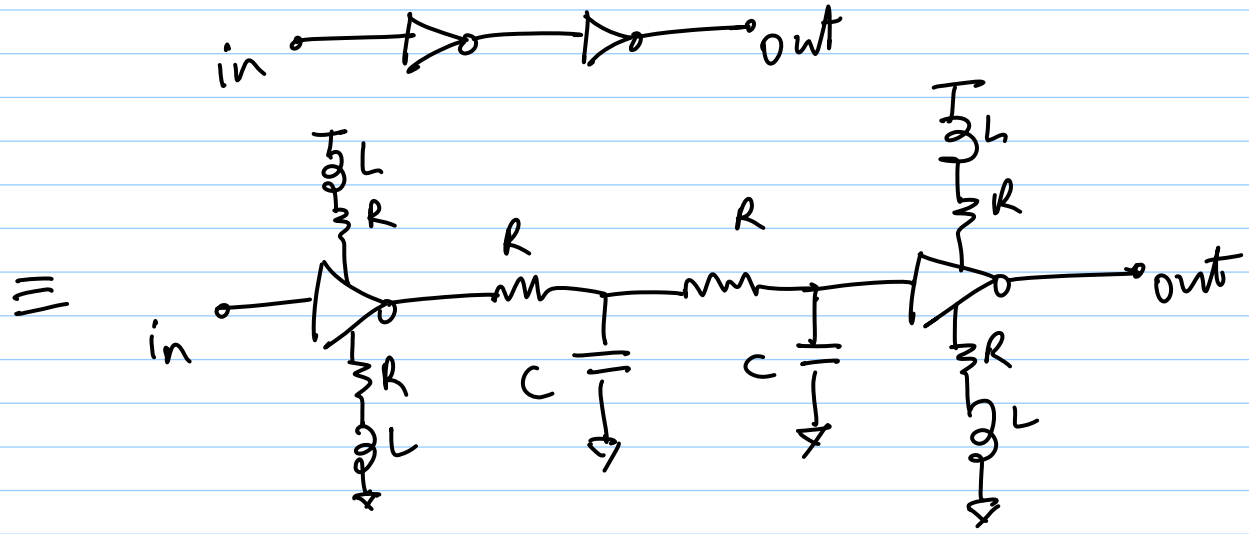
Physical Verification

* DRC = design rule check (widths, lengths, spacings etc.)
* LVS = Layout vs schematic (electrical connection match)
* ERC = electrical rule check (e.g. thin oxide device connected to higher supply)

→ Layout Parasitic Extraction (LPE)

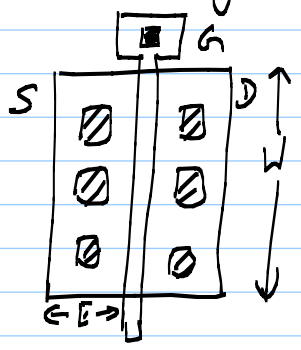
* ensure that circuit works with R, L & C parasitics related to layout (e.g. routing)

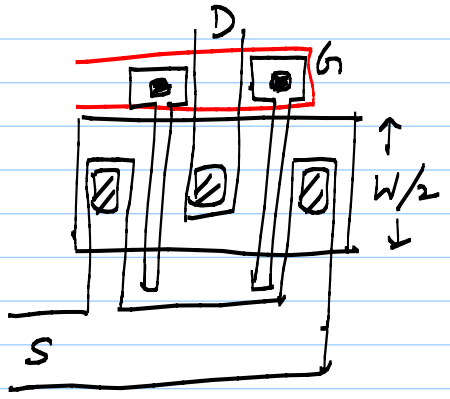
e.g. simple 2-inverter cascade

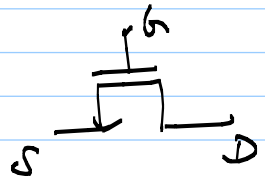



## Analog/RF layout practices

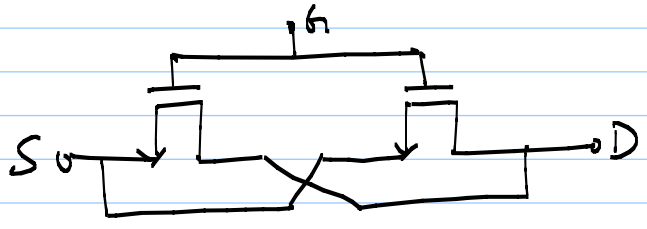
### 1) Multi finger transistors



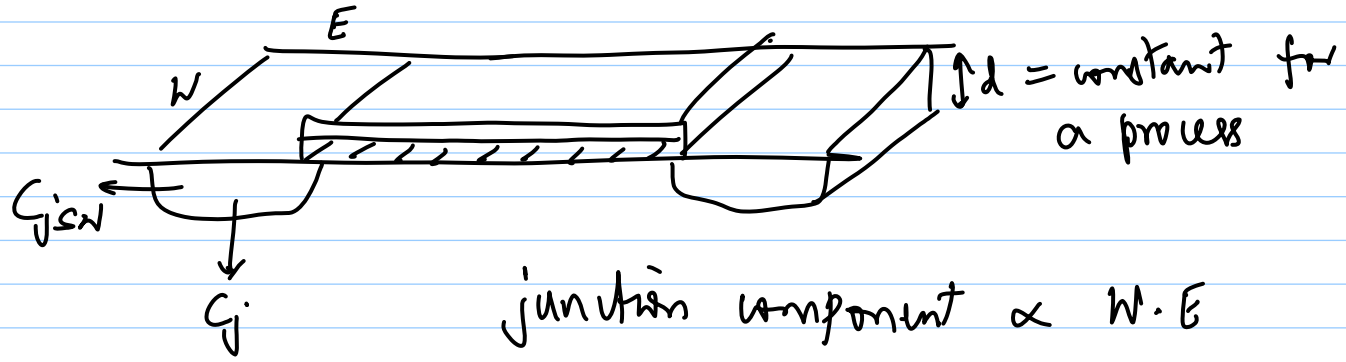

(a)




(b)

## S/D Capacitance

$C_{DB}$ & $C_{SB}$ : → junction cap - $C_j$
→ sidewall cap - $C_{jsw}$




junction component $\propto W \cdot E$

SW component $\propto W$

Note: $C_j$ = ____ $fF/\mu m^2$

$C_{jsw}$ = ____ $fF/\mu m$

(a) : $C_{DB_a} = C_{SB_a} = W \cdot E \cdot C_j + 2(W+E) C_{jsw}$

(b) : $C_{DB_b} = \frac{W}{2} \cdot E \cdot C_j + 2\left[\frac{W}{2} + E\right] \cdot C_{jsw}$

$$C_{SB_b} = 2\left[\frac{W}{2} \cdot E \cdot C_j + 2\left(\frac{W}{2} + E\right) \cdot C_{jsw}\right]$$

$$= W \cdot E \cdot C_j + 2(W + 2E) \cdot C_{jsw}$$

for same total W/L,

$$C_{DB_b} < C_{DB_a}$$

Gate resistance = $r_g$

poly resistance is usually given in $\Omega/\square$

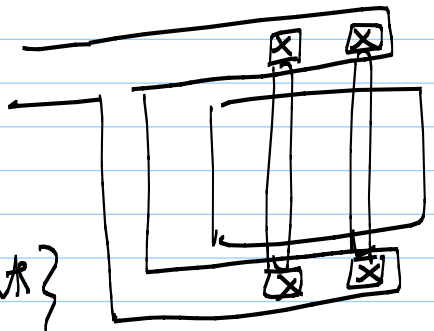
In this specific case,

$r_{gb} \sim \frac{r_{ga}}{4}$ { accurate expression has been given earlier }

in general, $r_g \propto W_{finger}$ i.e. $r_g \propto \frac{1}{n_f}$

* Try to contact gate from both sides
* $r_g$ can also produce resistive noise
* Do not route gate in poly
  → between fingers or
  → in any connection to gate

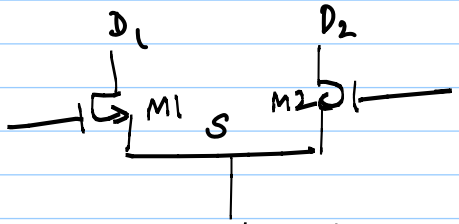
{ this is done in CMOS gate layouts for layout efficiency }



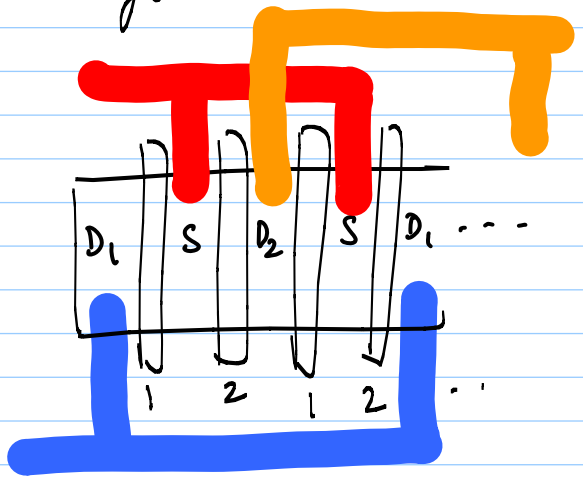
D, S resistance — can become significant in single finger devices with large W.

Aspect ratio — device layout can be made more squarish or fit into layout constrained spaces.

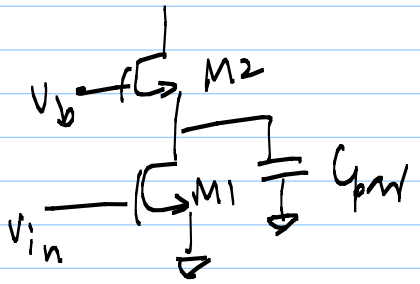
2) Interdigitisation :




* process related effects are distributed out

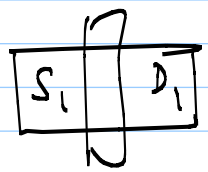


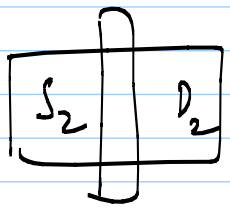
* improves matching and symmetry in current mirrors, diff pairs, cascodes etc.
→ reduces CM noise coupling, even order non-linearities



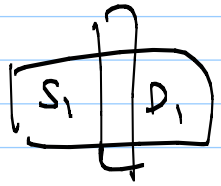

* reduces cap between cs & cascode through shared S-D node
* saves area

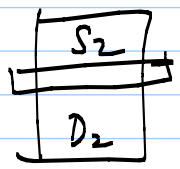
3) <u>other techniques for Symmetry</u> :
→ Intn digitisation is layout-intensive
→ can also add extra R-C parasitics
a) Same orientation – to remove proces effects




✓

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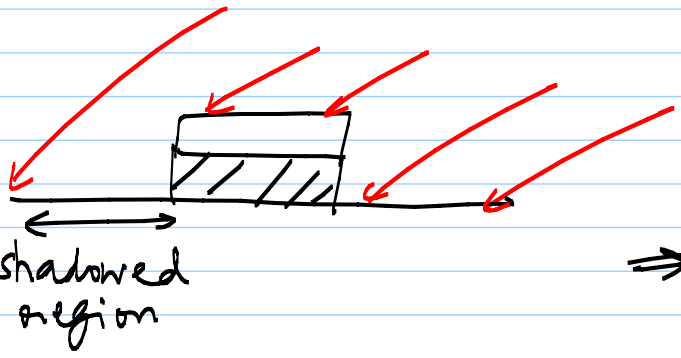
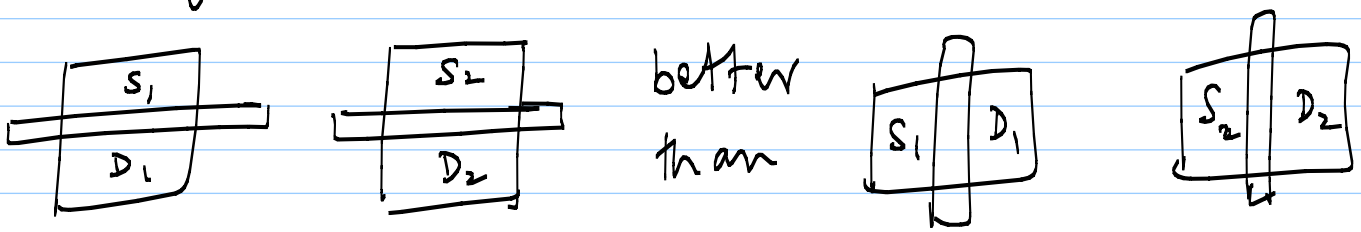
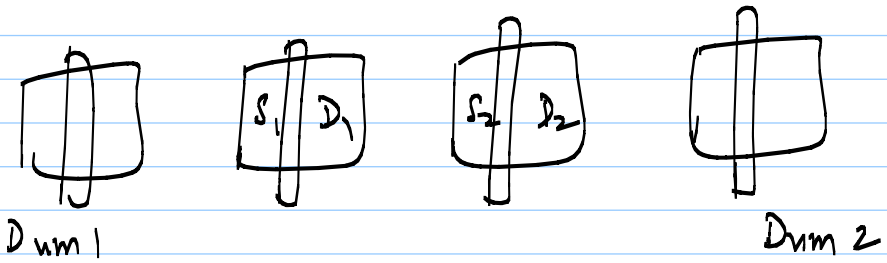
b) Add dummies (takes care of gate-shadowing)

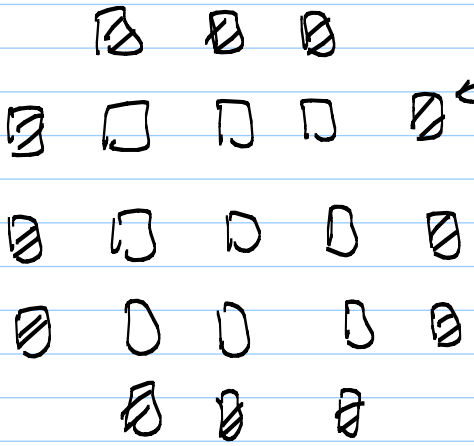



⇒ S-D asymmetry



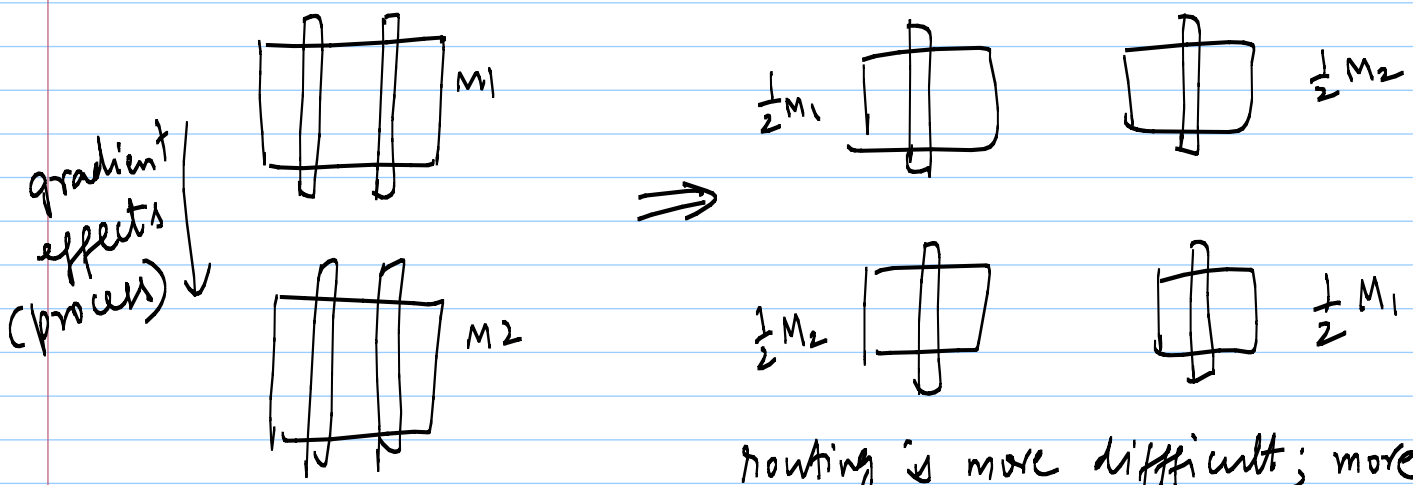

better option — add dummy devices




Basic idea: maintain same environment on either axis of symmetry

c) Common centroid:




routing is more difficult; more parasitic cap is possible

→ common centroid is of limited value in RF layouts due to extra parasitics