Lecture #37: Analog & RF Layout

Layout: Geometries that appear on masks used in fabrication ⇒ top view of the devices and associated connections (routings)

Top view of a MOSFET (layout)

```
          
         P

S         D

B
```

remind: MOSFETs are 4-terminal devices ⇒ Bulk (substrate) contacts are critical!

Side view:

(Conceptual)

```
| S |  |

P-sub
```

Why should you know layout? (And why not let the layout engineer take over completely)?

→ Designer has ultimate responsibility
→ RF circuits are very sensitive to layout
  * design & layout go together
* Be aware of noise-sensitive & noise-producing circuits in and around your circuit location
  * Time: only ~50%. Time spent in design
  * Other 50%, time - layout
  * Several iterations are common for sensitive circuits ⇒ increases design cycle time
  * May identify weaknesses of design

**General Considerations:**

⇒ Design rules: mainly limited by lithography (L) or processing (P) constraints

* Minimum width (P) - e.g. metal line, device, etc.
  * Min. spacing (L) - e.g. metal-metal, poly-active
  * Min. enclosure (P) - e.g. metal over contact/via
  * Min. extension (P) - e.g. gate poly beyond active

**Physical Verification**

* DRC = design rule check (widths, lengths, spacings etc.)
  * LVS = Layout vs. schematic (electrical connection match)
  * ERC = electrical rule check (e.g. thin oxide device connected to higher supply)
Layout Parasitic Extraction (LPE)

* ensure that circuit works with RC, LC parasitics related to layout (e.g., routing)

* e.g., simple 2-inverter cascade

![Diagram of a 2-inverter cascade circuit]

Analog/RF layout practices

1) Multi-finger transistors

![Diagram of multi-finger transistors]

(a)  

(b)
S/D Capacitance

\[ \frac{C_{DB} \& C_{SB}}{} \rightarrow \text{junction cap. } C_j \]
\[ \text{external cap. } C_{JSW} \]

\[ E \]

\[ d = \text{constant for a process} \]

\[ \text{junction component } \propto W \cdot E \]
\[ \text{SW component } \propto W \]

\[ \text{Note: } C_j = \frac{fF}{\mu m^2} \]
\[ C_{JSW} = \frac{fF}{\mu m} \]

(a) \[ C_{DBa} = C_{SBa} = W \cdot E \cdot C_j + 2(W+E) \cdot C_{JSW} \]

(b) \[ C_{DBb} = \frac{W}{2} \cdot E \cdot C_j + 2 \left[ \frac{W}{2} + E \right] \cdot C_{JSW} \]
\[ = W \cdot E \cdot C_j + 2(W+E) \cdot C_{JSW} \]

\[ \text{for same total } W/L, \]
\[ C_{DBb} < C_{DBa} \]

Gate resistance \( R_g \)

Poly resistance is usually given in \( \Omega/\mu m \)
In this specific case, 
\[ \frac{g_{bs}}{g_{ds}} \] \{ accurate expression has \} 
been given earlier.

In general, 
\[ r_g \propto \frac{1}{n_f} \]
* Try to contact gate from both sides
* \( r_g \) can also produce resistive noise
* Do not route gate on poly
  - between fingers or
  - in any connection to gate
  \{ this is done in cmos gate layout \} for layout efficiency

\[ D_s \text{ resistance} \] - can become significant in single finger devices with large \( W \).

Asper ratio - device layout can be made more squarish or fit into layout constrained spaces.

2) Interdigitisation:

\[ D_1 \quad D_2 \]
\[ M_1 \quad M_2 \]

* process related effects are distributed out
* improves matching and symmetry in current mirrors, diff pairs, cascades etc.
  → reduces CM noise coupling even order non-linearities

\[ V_b \xrightarrow{\text{M}^2} V_{in} \overset{\text{C}_{M1}}{\xrightarrow{\text{S}} \text{C}_{PSL}} \]

* reduces cap between cs & cascode through shared S-D node
* saves area

3) Other techniques for symmetry:

→ Introducing is layout-intensive
→ can also add extra R-C parasitics

a) Same orientation → to remove process effects

\[ S_1 \rightarrow D_1 \quad S_2 \rightarrow D_2 \quad \checkmark \]

\[ S_1 \rightarrow D_1 \quad S_2 \rightarrow D_2 \quad \times \]
6) Add dummy devices (takes care of gate-shadowing)

S/D implant @ 7°

shadowed region

⇒ S-D asymmetry

\[
\begin{align*}
S_1 & \quad D_1 \\
S_2 & \quad D_2
\end{align*}
\]

better than

\[
\begin{align*}
S_1 & \quad D_1 \\
S_2 & \quad D_2
\end{align*}
\]

better option — add dummy devices

Dum 1

Dum 2

Basic idea: maintain same environment on either axis of symmetry
c) Common centroid:

\[ \frac{1}{2} \text{M}_1 \quad \frac{1}{2} \text{M}_2 \]

\[ \Rightarrow \]

\[ \frac{1}{2} \text{M}_2 \quad \frac{1}{2} \text{M}_1 \]

Routing is more difficult; more parasitic cap is possible.

\[ \Rightarrow \text{Common centroid is of limited value in RF layouts due to extra parasitics} \]