Lecture 8: Capacitors, Varactors

Linear caps

* Special RF processes - metal-insulator-metal (MIM)
  * Capacitors - use special high-k dielectrics (caps)
  * Standard processes - MOM caps (oxide)

Problem: Oxide thickness is normally large to reduce cap between layers - 
  cap/unit is small area 
  ($\sim 0.1-0.2 \, \text{fF/\mu m}^2$)

\[ C \approx \varepsilon \frac{W \cdot L}{d} \]

\[ d = \text{thickness of oxide between metal layers} \]

* another issue: bottom-plate cap. (to lower metal or substrate)

\[ \Rightarrow \text{can be as high as 10-30\% of cap} \]

\[ \text{Vin} \quad \Rightarrow \frac{C}{L} \quad \downarrow \]

\[ \text{Signal} \quad \Downarrow \quad C_{\text{bot.}} \]

* Be careful how you design ac coupling caps!

* Fringing can be significant for caps with small \( W \cdot L \)

* Temperature coefficient is often small

Lateral flux capacitor

\[ \Rightarrow \text{better density} \]

Plate 1

* can use multiple layers to increase density

Plate 2

* min. metal-metal spacing decreases with process scaling
* Parapletic bottom plate cap is smaller (because of better density)
* Lateral cap depends on perimeter
  \[ \Rightarrow \text{use layouts that maximise perimeter (e.g. fractals)} \]

\[ \text{MOS capacitance} \]

* Gate capacitance of MOSFET \( \sim 1-2 \, \text{fF/mm width} \)
* Larger temp-co (depends on doping levels)
* Single-ended caps - can be used for ground caps (e.g. supply bypass, single-ended filtering etc.)

\[ \frac{V_{in}}{V_{out}} \]

\[ C_{mos} = f(V) \]

\[ \Rightarrow \text{small-signal case only} \]
\[ \Rightarrow \text{DC bias is critical} \]

\[ \text{Varactor} \Rightarrow \text{device whose capacitance can be varied using a voltage (i.e. voltage controlled capacitance)} \]

* Can be used to tune a resonant circuit, and hence a receiver/transmitter

\[ \text{Remember: For a reverse-biased p-n Junction} \]

\[ C_{var} = \frac{C_0}{(1 + \frac{V_R}{\Phi_B})^n} \]

\[ \Phi_B = \text{built-in potential of junction} \]
\[ m = 0.5 \text{ for an abrupt junction} \]
\[ m \sim 0.3 - 0.4 \text{ for typical CMOS processes} \]

Thickenss of depletion region changes with \( V_R \)
Varactor diodes: diodes whose junctions are graded to:

- Control \( C = f(V_J) \) \{linear, quadratic, etc.\}
- Maximise \( \frac{C_{\text{max}}}{C_{\text{min}}} \) \{i.e., maximise tuning range\}

Symbol: \[ \rightarrow \]

Not so common in CMOS processes nowadays.

**MOS Varactors**

- Cox
- Cmos

1: Accumulation
2: Depletion
3: Weak Inversion
4: Moderate Inversion
5: Strong Inversion

(Vgb > |Vt|) \( \Rightarrow \) Strong inversion \{transistor behaviour\}

\( V_{gb} < 0 \) \( \Rightarrow \) Accumulation

\( (\text{i.e.} \ V_g > V_b) \) gate oxide - substrate interface allows electrons to flow freely \{Interface voltage > 0\}

In both conditions, \( C_{\text{mos}} = C_{\text{ox}} \) (across gate oxide)

In depletion, weak and moderate inversion

\( \rightarrow \) very few \{mobile\} charge carriers @ oxide - substrate interface

\( \rightarrow \) \( C_{\text{mos}} < C_{\text{ox}} \)

\* In strong inversion, \( \frac{L}{12 K_p W (V_{gb} - |V_t|)} \) \{not valid @?\}

\( V_{gb} = |V_t| \)
* Cmos vs. VBA is non-monotonic
  → not good for tuning!

1) Inversion-mode varactors
  → prevent transistor from enter accumulation region

  * disconnect D-S from B
  * connect B to highest voltage available (i.e. VDD)

* VT1 > VT0 due to substrate effect (VB > VS)
* tuning range of I-MOS is much wider
* NMOS cap shows similar effect
  → lower RMOS due to |μn| > |μp|
  → more sensitive to substrate noise
  (PMOS is in an n-well)

2) Accumulation mode varactors
  → inhibit formation of inversion layer
  * remove D-S p+ diffusion
  * place bulk contacts to reduce parasitic n-well resistance

* No extra process step required; however A-MOS device may not be characterised/modelled
- $Q_{\text{S-MOS}} > Q_{\text{A-MOS}}$
- nMOS varactor shows better $Q$
- gate node is usually connected to signal
  - higher $Q$
  - lower parasitic cap
- $\frac{C_{\text{max}}}{C_{\text{min}}}$ is limited by $C_{\text{D}}$ and $C_{\text{AS}}$ overlap caps (i.e., $C_{\text{min}}$)
- high $Q \Rightarrow$ minimum $L$ (R-MOS is lower) 
- basic varactor
  - high $\frac{C_{\text{max}}}{C_{\text{min}}}$ \Rightarrow large $L$ (overlap fraction) 
- lower tradeoff
- CMOS - var characteristic are for small signal
  - applied around DC $V_{\text{BA}}$; If signal is large (e.g., VCO), instantaneous value of CMOS changes
through signal period.

$\Rightarrow$ average $C_{mos} = f(V_{bn})$

$\Rightarrow$ monotonicity is very important

* Varactor $Q$s are usually much higher (20-40) than inductor $Q$s (5-10)

* Varactor Diode $C_{max}/C_{min}$ can be increased by biasing the diode closer to forward-biasing

$\Rightarrow$ However, $Q$ drops very quickly

$\Rightarrow$ large signal conditions may forward bias the diode