Figures of Merit:

1) $Q$: usually want this to be maximised in the frequency range of interest. Note that the model is not a simple series or parallel RLC.

How is $Q$ determined?

a) Physical definition: $2\pi \cdot \frac{E_{\text{stored(pink)}}}{E_{\text{loss per cycle}}}$

b) $Q = \frac{\text{Im}(Z_{\text{in}})}{\text{Re}(Z_{\text{in}})} = \frac{\text{Im}(Y_{\text{in}})}{\text{Re}(Y_{\text{in}})}$

$Z_{\text{in}} = \frac{1}{Y_{\text{in}}}$

$Q = f \left( L_s, R_s, C_c, C_{ox}, C_{si}, R_s \right)$

$Q_{\text{ind}} = \frac{1}{\frac{1}{L} - \omega C}$ \{ inductive region \}
* SOI processes show much higher Q than regular CMOS processes

* Substrate losses reduce with distance from substrate — use highest possible metal (these are also usually thicker than lower metals)

* Use Patterned around Shield, if appropriate
  - better Q: a) current loops are broken by slotting — eddy currents
  - also reduces substrate noise coupling
  - more shunt capacitance (shield is now closer than substrate)

2) Self resonant frequency \( f_{sr} \)
   - Frequency at which inductance of spiral resonates with its own capacitive parasitics

* Real inductors have capacitive parasitics
* Real capacitors have inductive parasitics
* Remember — tank circuits have both inductors & capacitors

* Patterned ground shield reduces \( f_{sr} \)
- at $f_{SR}$, inductor impedance is purely resistive, and $Q = 0$
- Beyond $f_{SR}$, the inductor behaves capacitively
- $f_{SR}$ depends on spiral area

3) Total area occupied on chip A

![Graph showing Q versus frequency]

**Transformers:**
* Used in differential circuits (usually)
* Need to be symmetric
* Coupling factor to be maximised (usually)
  - There are cases where you would design for a specific coupling factor

**Planar Transformer - 1**
* Sideways coupling, $n = 2$
* Primary & secondary $S_2$ are symmetric
* Ports $P_1$ & $P_2$ ($S_1, S_2$)
* $S_1$ are not symmetric
Planar Transformer
* $n = 1$
* $P \& S$ symmetric
* $P_1 - P_2 \& S_1 - S_2$ are more symmetric than case 1
  - underpass causes asymmetry

Vertical Transformer
* $n = 1$
* $P \& S$ are completely asymmetric (different metal layers)

Transformer $\pi$-model

* Can cascade coils on multiple metal layers to make a spiral with large $L$ in a given area
  - larger series resistance due to higher $P$ of lower metal layers
  - useful to create “RF chokes” for PAs and wideband RF amplifiers
Other things to remember

* Overall LC tank Q is often limited by inductor Q

* Don't place anything close to a spiral (inductor xfrmr.)

* Use a guard ring around inductor for noise isolation and to provide good EM boundary conditions

* No metal fill inside inductor (what is this?)

* Maintain symmetry - gives higher Q

* Via resistance matters - use lots of vias in parallel if you need to change metal layers

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Note: * Project 1 will involve spiral inductor design using ASITIC

* You will be designing your own inductors using ASITIC for projects 2, 3 & 4 also. The design of the inductor will impact circuit performance, so learn this well.

* HW2 will include an impedance matching problem with a real inductor.