Lecture 83: VCO Design (cont.)

\[ C_{\text{max}} = C \quad (V_{\text{sw}} = \text{ON}) \]
\[ C_{\text{min.}} = C_{\text{series}} \left( C_{gd} + C_{db} \right) \]
\[ C_{\text{max}} \approx C_{gd} + C_{db} \quad (V_{\text{sw}} = \text{OFF}) \]

\( C_{\text{par.}} \propto W \)
\( Q \propto W \)

\( \Rightarrow \) trade-off between \( Q \) & Tuning range

* Varactor may require re-biasing
  e.g. from \( \Delta V = (V_{\text{DD}} - V_c) \) to \( (V_B - V_c) \)

\[ C_{\text{min.}} \]
\[ V_{\text{min.}} \quad V_{c,\text{max.}} \]

\( -\text{ve} \) voltages are undesirable

\[ V_{c,\text{range}} \]

\[ V_{A} \to V_{\text{co}} \quad V_{B} \]
* differential tuning also possible

- Larger linear \( V_c \) range
- \( C_1, C_2 \) slopes are different
  \[ \Rightarrow \text{non-linearities} \]

**DPLL (DCO)**

- No analog tuning
- \( \Delta f \) needs very fine tuning
  \[ \Rightarrow \text{extremely small switchable } C \text{ needed} \]
  
  e.g. 2kHz resolution @ 8kHz

  \[ C_{\text{max}} = 4.5\text{pF}, \quad L = 0.5\text{nH} \quad \Rightarrow \Delta C = 5\text{aF} \quad (5\times10^{-18}\text{F}) \]
Tail current filtering

* popular technique, many variations

\[ \text{Resonate } L_I, C_I @ 2\omega. \]

\[ \Rightarrow \text{high impedance } @ 2\omega. \]

\[ \Rightarrow \text{filters out noise folding down from } 2\omega. \]

\[ \text{and } C_1 = \text{large} \]

\[ \Rightarrow \text{filters out bias noise} \]

\[ \text{extra } L_I \text{ needed} \]
* Ensure regulator does not deteriorate PN (i.e. VCO-regulator co-design)
  * Regulator power consumption must be kept low

Buffers - several configs possible

- Single set of different outputs
- 3 sets of outputs
  * Extra cap loading on VCO
  * Tuning range reduced

Very long routings or many in parallel

⇒ Use 2-stage

* Also reduces feedback from load circuit (e.g., dividers)
* pseudo-differential
* low-noise
* 0-VDD outputs (dividers are often digital)

* inverter is most sensitive to noise during \( \Delta t \)

\[
\text{large } C_L + \text{narrow } \Delta t \Rightarrow \text{large inverters} \Rightarrow \text{high pins.}
\]

Noise floor dominated by buffer noise

e.g. WCDMA (duplex, Rx, Tx or at same time)
high-freq. VCOs: may need "open-drain" buffers

Effect of freq. division on PN

\[ x(t) \rightarrow y(t) \rightarrow x_{PN}(t) \]

+ freq. & phase have a linear relationship

\[ f \rightarrow f/N \Rightarrow \phi = \phi/N \]

\[ x(t) = A \cos (w_0 t + \phi) \]

\[ x_{PN}(t) = A \cos \left( \frac{w_0}{N} t + \frac{\phi}{N} \right) \]

\[ \Rightarrow PN \text{ magnitude at a given offset } \rightarrow \frac{1}{N} \]

\[ \Rightarrow PN \text{ power } \rightarrow \frac{1}{N^2} \{ \text{narrowband FM approx.} \} \]
Bipolar VCOs

- bipolar VEE ~ 0.7V
  - cap. divider allows larger swings @ O/p
- feedback also possible using XfmrS.

VCO Designs

1) Maximize Tank Q (i.e. higher Rp)
2) Maximize output swing, but don't saturate VCO {choose IR carefully}
3) Startup gain of ~ 2-3
4) Use minimum lengths to maximize tuning range (but keep 1/f噪声 in mind)
5) \[ R_p = \frac{1}{w_0LQ} \quad \text{and} \quad V_o = \frac{2}{10} I_T R_p \]

\[ \Rightarrow \text{maximize } L \text{ and } Q \text{ at the same time} \]

for \( \text{min- } P_N \) and \( \text{min- } P_{\text{diss}} \)

6) Choose between

- NMOS-only
- PMOS-only
- Complementary
- Colpitts (differential)
- Hybrid structure