1) Input match \( \{ \text{may require iteration} \)  
2) Output match  

* \( g_m \& C_{gd} \) will cause input \& output matches to depend on each other - Iteration  
* Input matching is quantified by \( S_{11} \) (also called 'return loss')  

\[
S_{11} = 20 \log \left| \frac{Z_{in} - R_s}{Z_{in} + R_s} \right|
\]

* Similarly, output matching is quantified by \( S_{22} \)  

3) Stability: Circuit Techniques to improve stability (i.e. decrease \( C_{gd} \) \& increase \( S_{12} \))  
   
   A) Neutralisation:  
   
   ![Circuit Diagram]

   * \( L_f \) \& \( C_{gd} \) resonate at desired frequency  
   * \( L_f \) \& \( C_{bl} \) parasitics load into node \( \text{area intensive (} L_f \text{)} \)  

   B) Cascade: \* reduces effect of \( C_{gd} \)  
   * reduces interaction between input \& output tuned cols.
\[ Z_1 = \frac{1}{g_m + g_{mb}} + \frac{Z_L}{(g_m + g_{mb}) r_0} \]

Assume \( r_0 \) is large, \( g_m \gg g_{mb} \)

\[ \Rightarrow Z_1 \approx \frac{1}{g_m} \]

* Parasitic cap can cause some loss of signal and degrade NF at high freq.
* Short-channel MOS - \( r_{out} \) is finite, so may want to use \( L \geq L_{min} \).

\[ \Rightarrow \text{This will increase } C_{par} \]

**Cascode LNA**

\[ Av = \frac{V_{out}}{V_{in}} = G_m R_p \]

\[ \Rightarrow [Av = 2 Q_{in} g_m R_p] \]

* Neglect \( r_{ds} \) (we will typically use a cascode)
5) Transducer Power gain $G_T$

$$G_T = \frac{\text{Power delivered to load}}{\text{Power available from source (max)}} = \frac{P_{\text{load}}}{P_{\text{max, source}}}$$

- $P_{\text{max, source}} = \frac{1}{2} \frac{\text{Vin}^2}{2R_s}$ \{ assume $\text{Vin}$, $\text{Vout}$ etc. are peak values \}

Let $Y_L = \frac{1}{Z_L}$ \Rightarrow $G_L = \text{Re}(Y_L) = \text{Re}\left(\frac{1}{Z_L}\right)$

$$P_{\text{load}} = \frac{1}{2} |\text{Vout}|^2 \cdot G_L = \frac{1}{2} |\text{Vout}|^2 \cdot \text{Re}\left(\frac{1}{Z_L}\right)$$

$$= \frac{1}{2} \text{Re}\left(\frac{1}{Z_L}\right) \cdot |G_m (R_p || Z_L)|^2 \cdot |\text{Vin}|^2$$

$$\Rightarrow G_T = \frac{1}{2} |G_m (R_p || Z_L)|^2 \cdot \frac{R_s}{Z_L} \cdot \text{Re}\left(\frac{1}{Z_L}\right)$$

a) LNA drives off-chip component (e.g. filter)

$\Rightarrow$ $Z_L$ is matched to $R_p$ in that case

$$G_T = \frac{1}{2} \cdot \frac{|G_m R_p|^2}{Z_L} \cdot \frac{R_s}{R_p} = \frac{G_m^2 R_s R_p}{4}$$
b) LNA drives mixer (or another amplifier)

Series-parallel transformation:

$$
R_L \approx Q_2^2 V_g 2
$$

$$
L \approx C_g 2
$$

$$
Q_2 = \frac{1}{\omega_0 V_g 2 C_g 2}
$$

* MOSFET with good layout ⇒ $V_g 2$ is very small

* Ideally $V_g 2 \to 0 \Rightarrow Q_2 \to \infty \Rightarrow R_L \to \infty$

* $C_L$ is usually absorbed into $C_p$ (output tuning network of LNA)

$$
G_T = \left(\frac{G_m \left(\frac{R_p}{R_L}\right)}{R_L}\right)^2 \frac{R_s}{R_L}
$$

$G_T \to 0$ as $R_L \to \infty$

What does this mean?

⇒ ideal MOSFET $M_2$ has purely capacitive gate

⇒ no real power consumed at input

⇒ $P_{load} \to 0 \Rightarrow A_T \to 0$
b) Available power gain $A_p$

$$A_p = \frac{\text{Power available from LNA output}}{\text{Power available from source}} = \frac{P_{\text{av,LNA}}}{P_{\text{av,s}}}$$

$P_{\text{av,LNA}}$ = power delivered to load under matched condition (same as $4\omega$)

$$A_p = \frac{G_m^2 \cdot R_s \cdot R_p}{4}$$

How about power dissipation?

**Power-constrained noise optimisation:**

* Minimise $F$ given a specific bound on $P_{\text{av,LNA}}$.

---

* Fix full details, see Thomas Lee pp 380-384

From 2-port noise theory,

$$F = F_{\text{min.}} + \frac{R_n}{G_s} \left[ (h_{s} - h_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 \right]$$

* Define

$$\frac{Q_{\text{opt}}}{\omega G_s} = \alpha \sqrt{\frac{5}{5Y}} = Q_{\text{opt}}.$$ 

$$Q_s = \frac{1}{\omega G_s R_s}$$

* Rewrite $F = F_{\text{min.}} + \left[ \frac{\gamma}{2G_m R_s} \right] \left[ 1 - \frac{Q_{\text{opt}}^2}{Q_s^2} \right]$

* Optimum $Q_{\text{opt}}$ turns out to be $\approx 4.5$
\* \[ W_{opt,p} = \frac{1}{2} \frac{1}{WLCOXRS Qsp} \approx \frac{1}{3WLCOXRS} \]

\* \[ F_{min,p} \approx 1 + 2.4 \frac{x}{\alpha} \left[ \frac{W}{W_T} \right] \]

\* \[ F_{min} \approx 1 + 2.3 \left[ \frac{W}{W_T} \right] \]

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<th>( W_T/W )</th>
<th>( F_{min} )</th>
<th>( F_{min,p} )</th>
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basic design procedure:

1) Determine \( W_{opt,p} \) as above

2) Choose \( I_{bias} \) based on power constraint

3) Determine \( L_s \) (with \( R_{in}, W_T \) known)

4) Calculate \( NF_{min,p} \)

5) Choose \( L_g \) for desired \( f_o \)

6) Choose \( L_D \) to maximize \( R_p \) (highly dependent on process) and \( i_o \) gain

Note: you will probably need to iterate at each step and also between steps

* Noise vs. linearity tradeoff

as \( I_{bias} \uparrow \Rightarrow (V_{as} - V_T) \uparrow \Rightarrow 11P_3 \uparrow \)

but \[ \Rightarrow \alpha \] (i.e. \( g_m \)) \downarrow \Rightarrow \text{F} \uparrow \text{increased short-channel effects} \[ \Rightarrow \]