Phase locked loop frequency synthesizers

SMDP Instructional Enhancement Program

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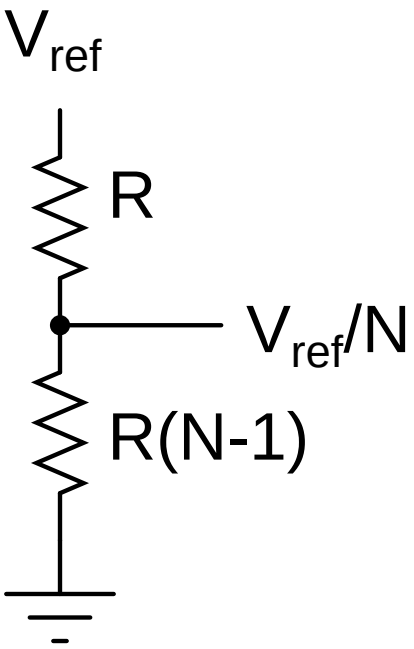
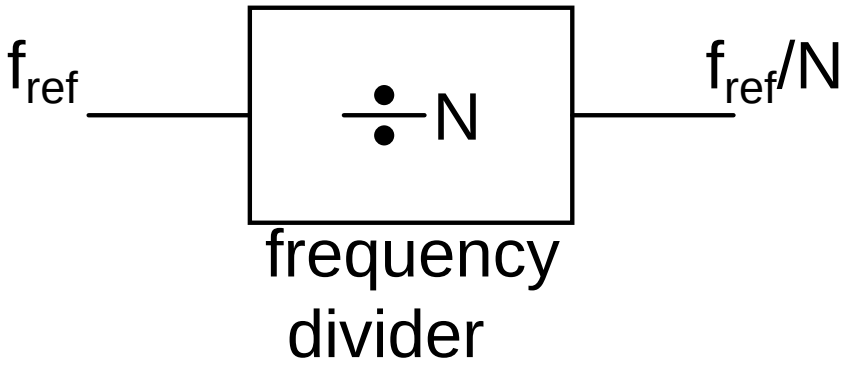
13-24 Nov 2006

Local oscillator requirements

- Generate equally spaced frequencies from an input reference frequency
- Waveform shape not very important
- Spurious output must be sufficiently low
- Noise must be sufficiently low

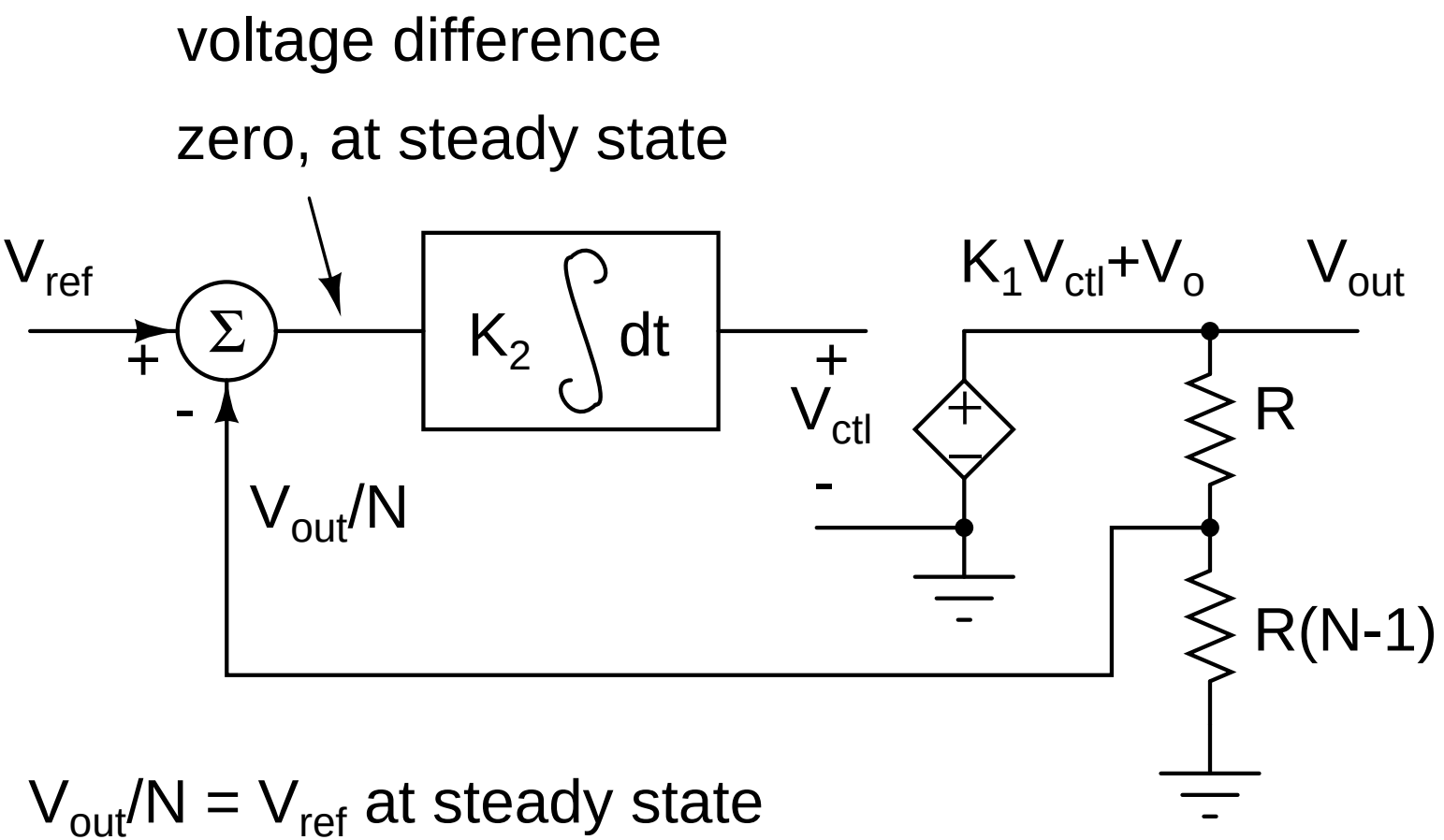
Frequency divider





- Digital frequency divider can generate multiple frequencies
- Frequencies not equally spaced
- Reference frequency higher than output frequencies

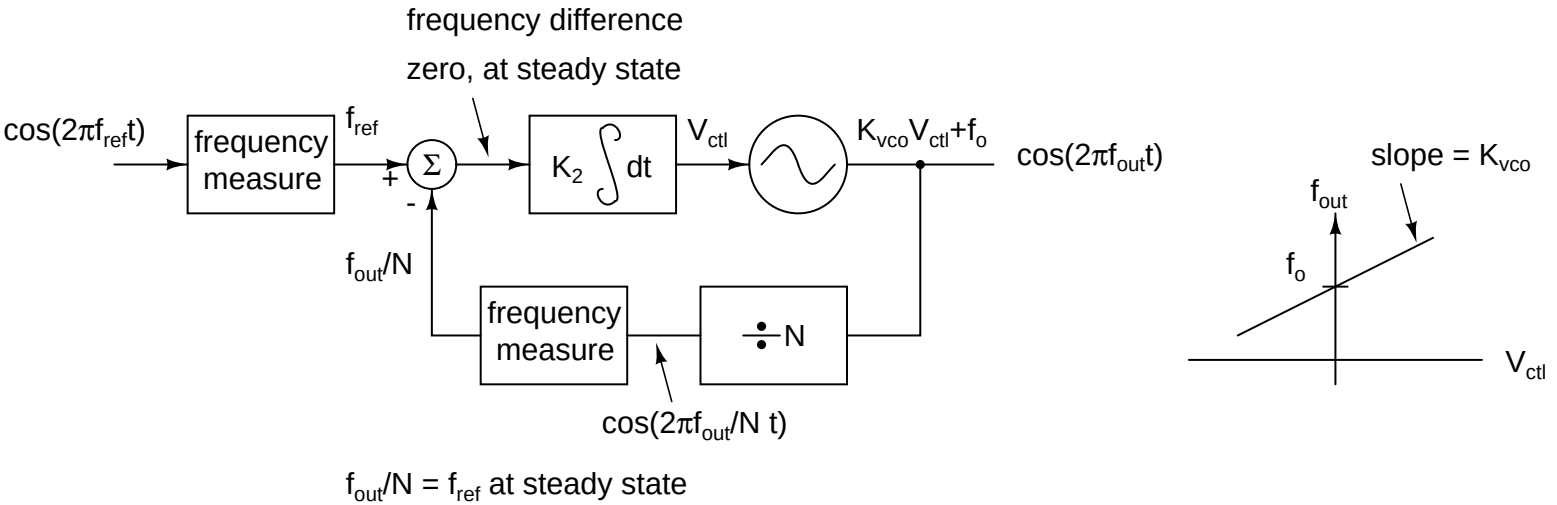
Voltage multiplier



$V_{out}/N = V_{ref}$ at steady state

- A controlled source to generate the output voltage
- Divided output voltage subtracted from the reference to generate error
- Output source controlled by the integral of the error

Frequency multiplier

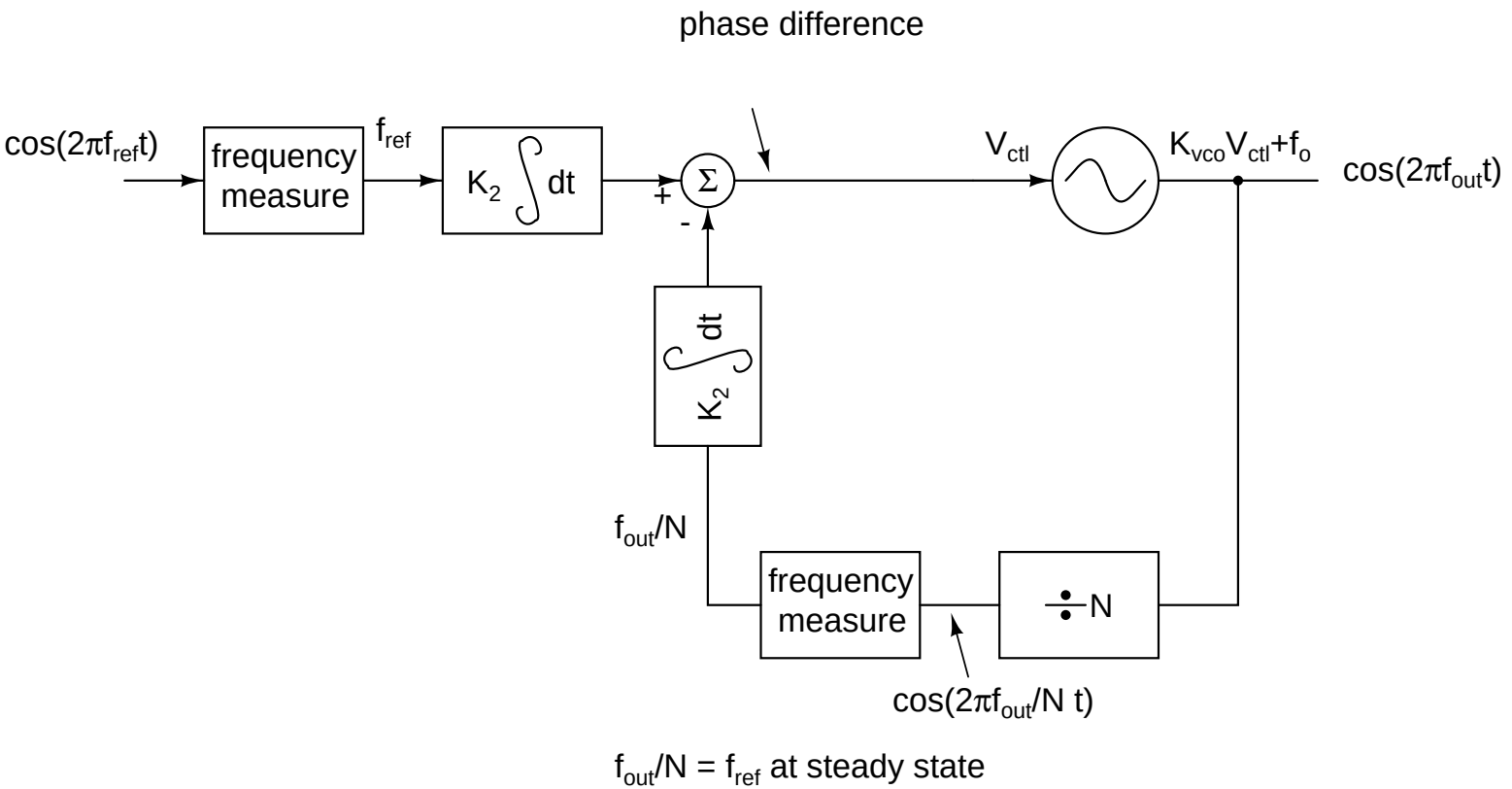


- A controlled source to generate the output frequency
  - A voltage controlled oscillator
- Divided output frequency subtracted from the reference frequency to generate error
- Output source controlled by the integral of the frequency error

Phase and frequency

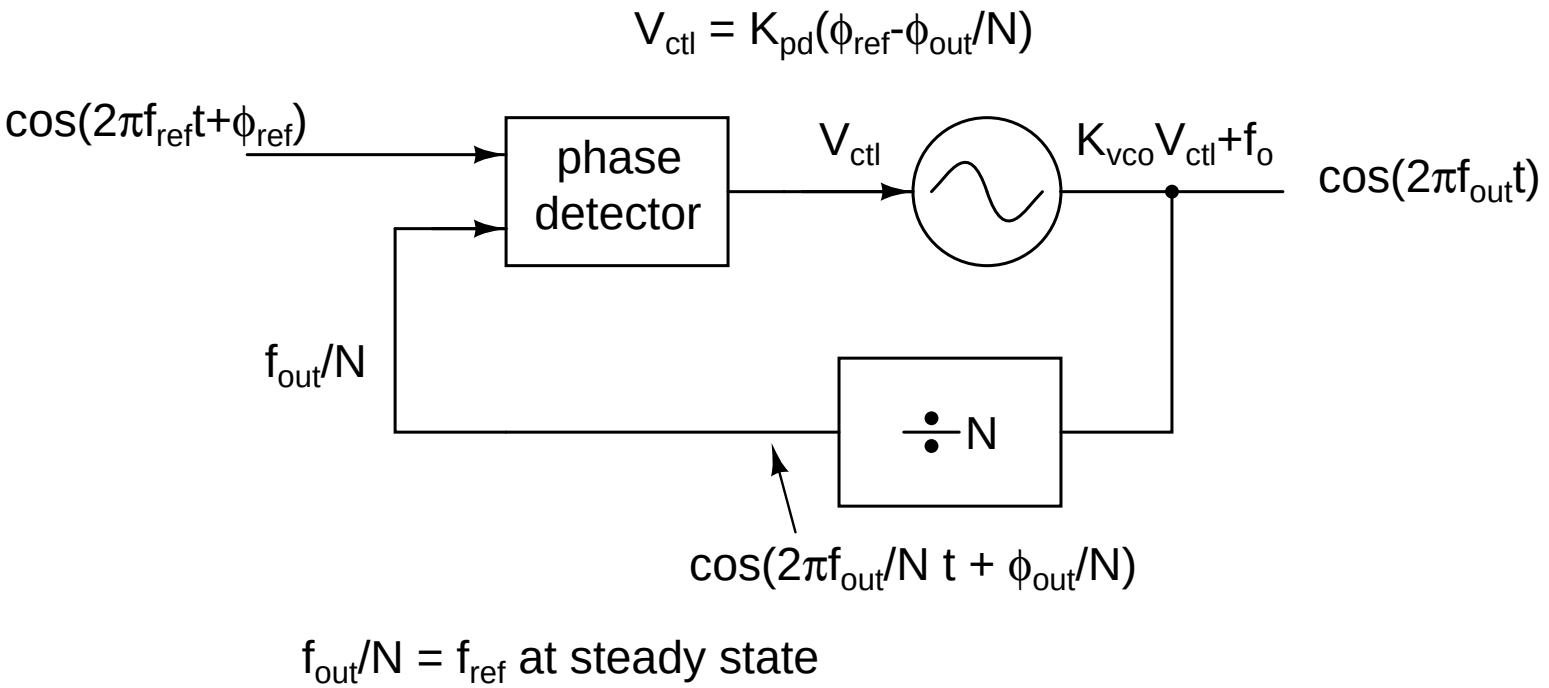
- Sinusoid $\cos(\theta(t))$
- Phase: $\theta(t)$
- Instantaneous frequency $f_i = \frac{1}{2\pi}\frac{d\theta(t)}{dt}$
- Typically expressed as $f_i = f_o + f_e(t)$ where f_o is the average frequency and f_e is the instantaneous frequency error
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + 2\pi \int f_e(t)dt$
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + \phi(t)$
  - Φ_o: phase offset
  - $\phi(t)$: instantaneous phase

Frequency multiplier



- Integration before subtraction
- Integral of the frequency is phase
- Integrator+subtractor measures phase difference between the reference input and the divided output (feedback)

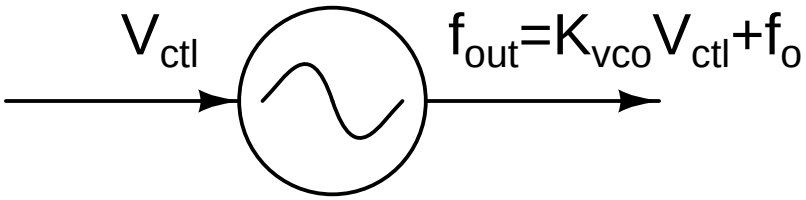
Frequency multiplier—Phase locked loop

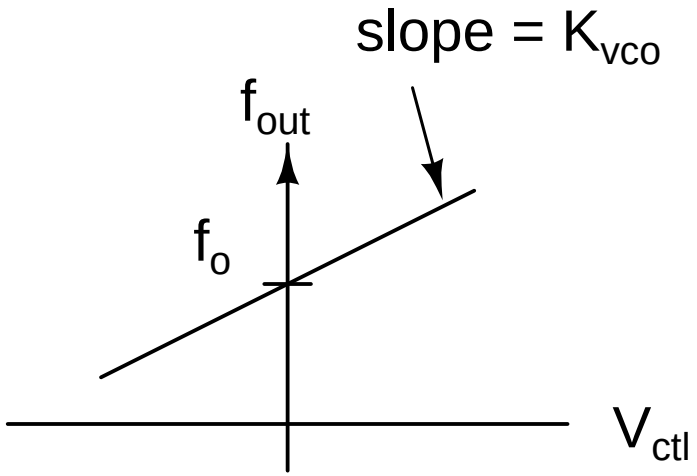


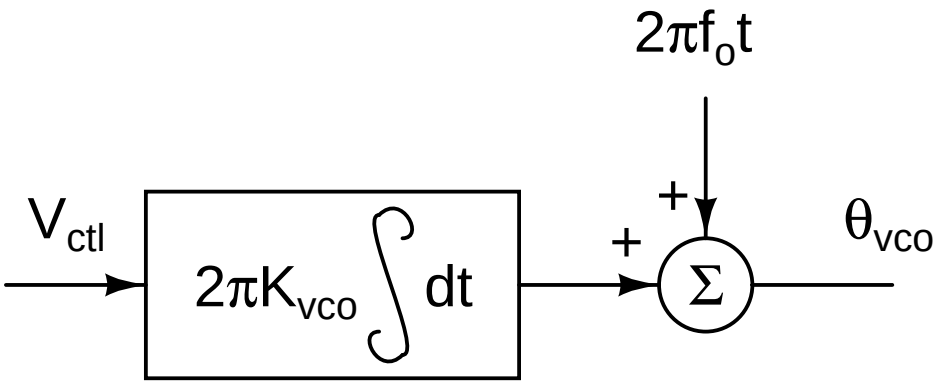
$f_{out}/N = f_{ref}$ at steady state

- Use a phase detector to generate the control voltage

Voltage controlled oscillator

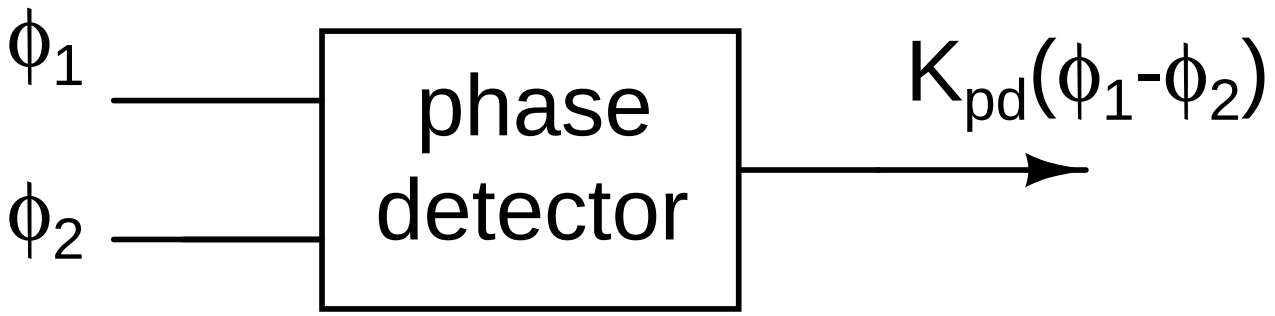






- $f_{vco} = f_o + K_{vco}V_{ctl}$
- $\theta_{vco} = 2\pi f_o t + 2\pi K_{vco}\int V_{ctl}dt$
- K_{vco}: VCO gain in Hz/V

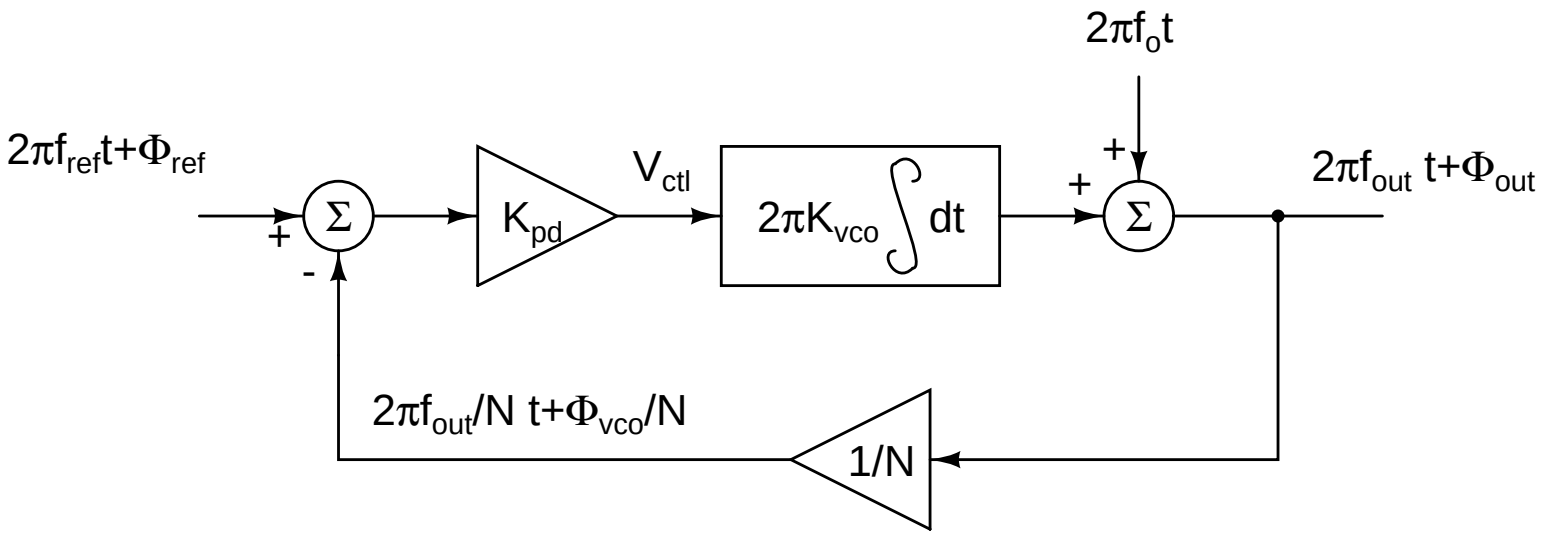
Phase detector



K_{pd}: phase detector gain

- K_{pd}: Phase detector gain in V/radian
- Ideal phase detector: assumed to have an output $V_{pd} = K_{pd}(\phi_1 - \phi_2)$

Phase locked loop model

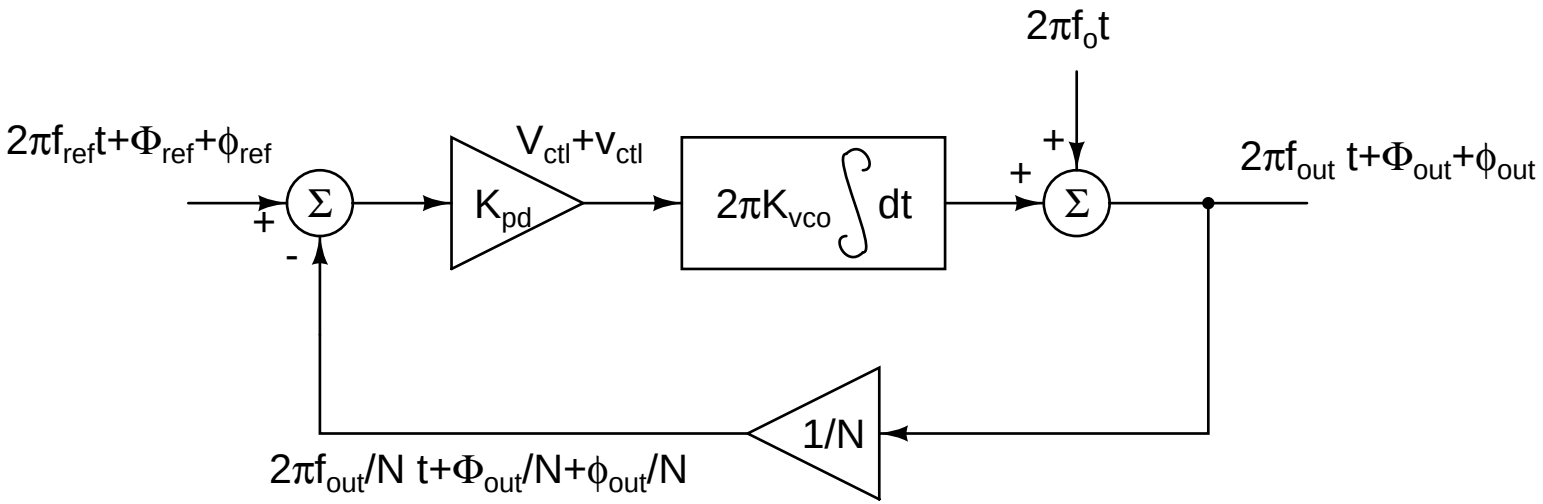


$V_{ctl} = 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $V_{ctl} = \Phi_{ref} - \Phi_{out}/N$

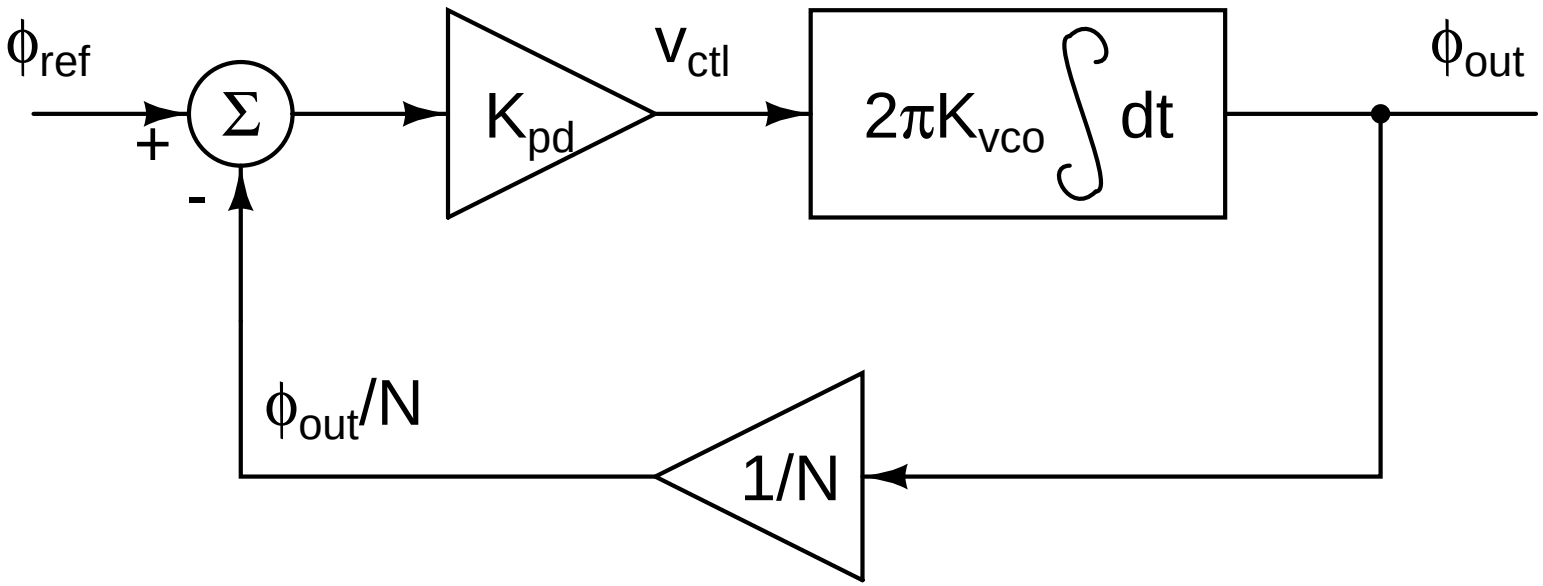
- Modelled in terms of phases of signals
- At steady state (lock), V_{ctl} is a constant $\Rightarrow f_{ref} = f_{out}/N$.
- The loop locks with
  $V_{ctl} = K_{pd}(\Phi_{ref} - \Phi_{out}/N) = (Nf_{ref} - f_o)/K_{vco}$—This is the "operating point" of the circuit

Phase locked loop model



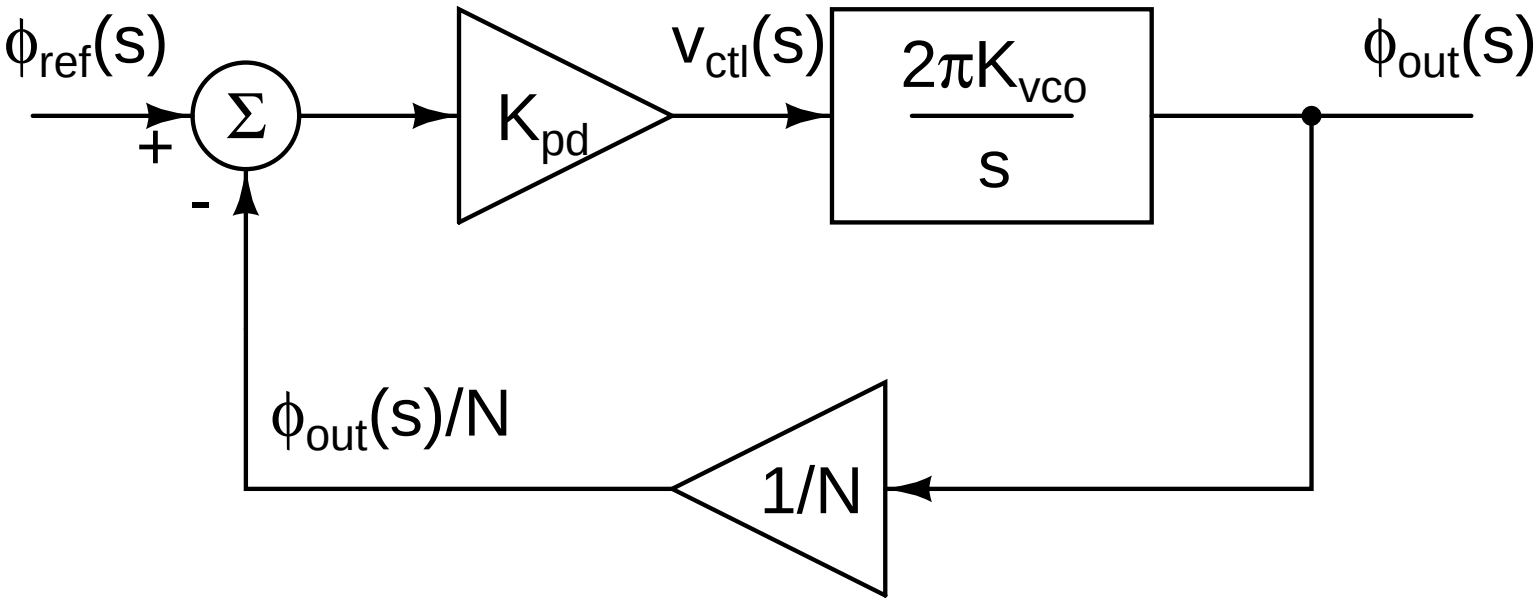
- An increment ϕ_{ref} in the input phase causes increments ϕ_{out}, v_{ctl}

Phase locked loop model—incremental picture



- An increment ϕ_{ref} in the input phase causes increments ϕ_{out}, v_{ctl}
- Type-I loop—One integrator in the loop

Phase locked loop model—frequency domain

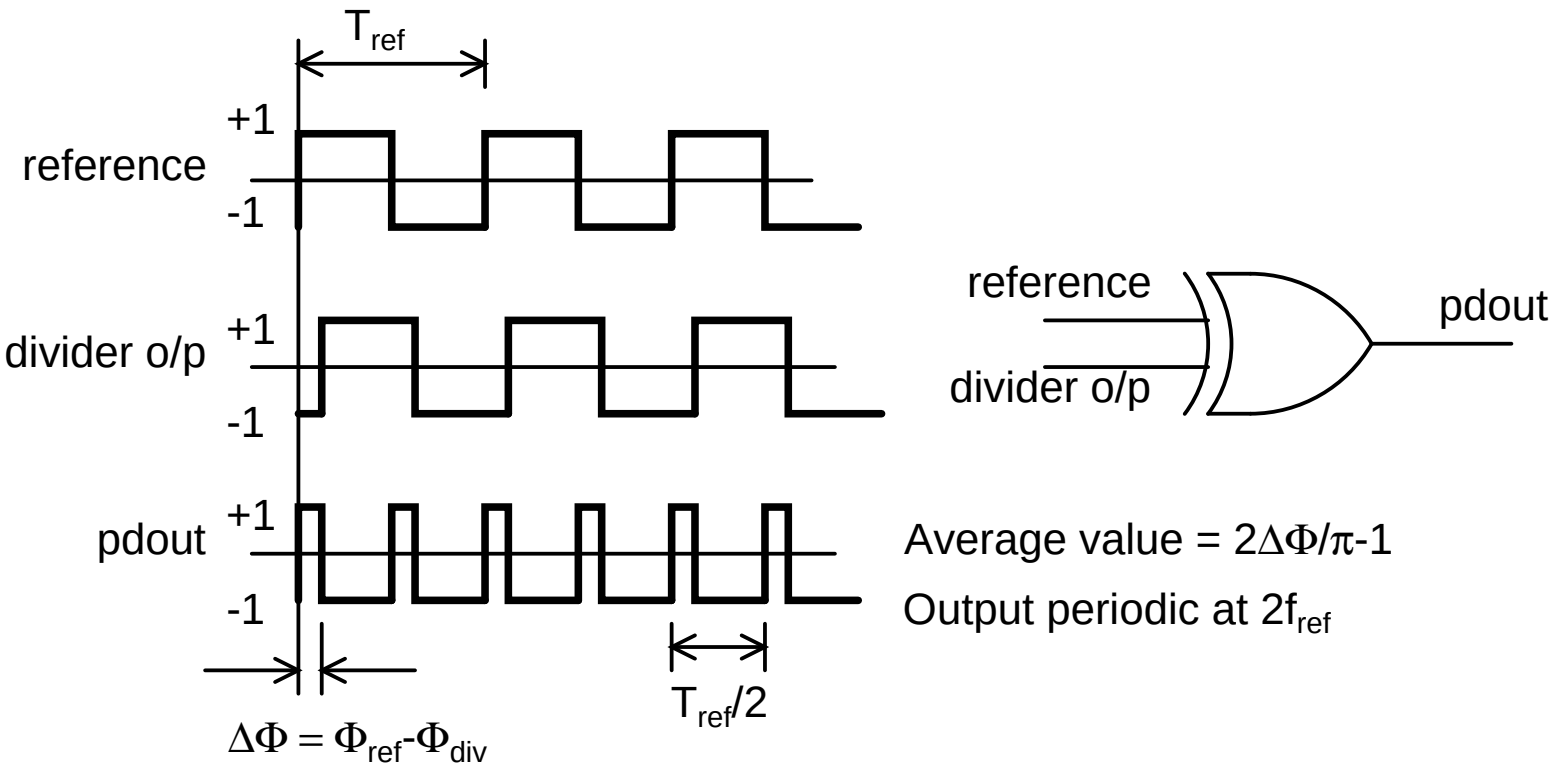


- Loop gain $L(s) = 2\pi K_{pd} K_{vco}/Ns$
- Transfer function $\phi_{out}(s)/\phi_{ref}(s) = N/(1 + Ns/(2\pi K_{pd} K_{vco}))$
- Type-I loop—One integrator in the loop

Type-I PLL—limitations

- Phase error when locked ($f_{out} = Nf_{ref}$):
  $\Phi_{ref} - \Phi_{out}/N = (Nf_{ref} - f_o)/K_{vco}K_{pd}$
- $-\pi < \Phi_{ref} - \Phi_{out}/N < \pi \Rightarrow$
  $f_o - \pi K_{pd}K_{vco} < f_{out} < f_o + \pi K_{pd}K_{vco}$
- Lock range limited by periodicity of phase detector (period of all phase detectors not necessarily $\pm\pi$)
- $K_{pd}K_{vco}$ large for wide lock range

XOR phase detector



Average value = $2\Delta\Phi/\pi$-1

Output periodic at $2f_{ref}$

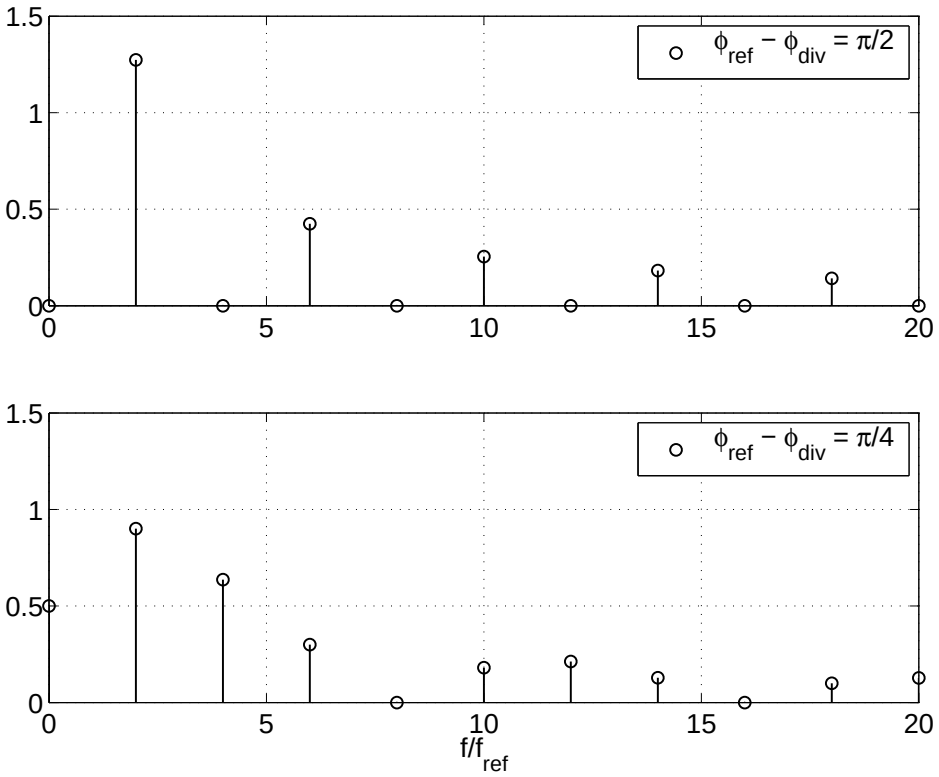
$$V_{out}(f) = \frac{2}{\pi}\left(\Delta\Phi - \frac{\pi}{2}\right)\delta(f) + \frac{4\Delta\Phi}{\pi}\sum_{n=1}^{\infty}\text{sinc}\left(\frac{n\Delta\Phi}{\pi}\right)e^{-jn\Delta\Phi}\delta(f-2nf_{ref})$$

$$V_{out}(t) = \frac{2}{\pi}\left(\Delta\Phi - \frac{\pi}{2}\right) + \frac{4\Delta\Phi}{\pi}\sum_{n=1}^{\infty}\text{sinc}\left(\frac{n\Delta\Phi}{\pi}\right)\cos(4\pi nf_{ref}t - n\Delta\Phi)$$

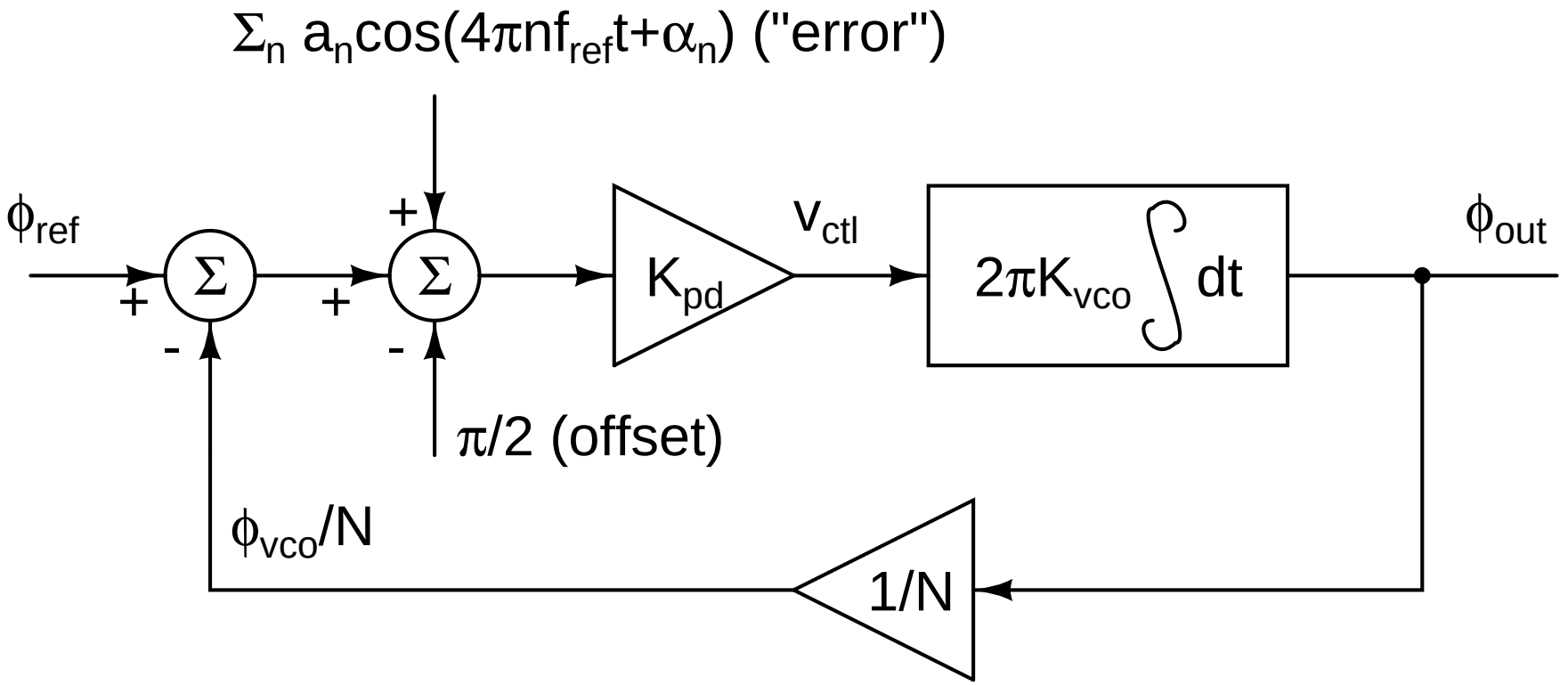
XOR phase detector

- Output average value = $2\Delta\Phi/\pi - 1 = 2/\pi(\Delta\Phi - \pi/2)$
  - $K_{pd} = 2/\pi$
  - Phase detector offset $= \pi/2$
  - Loop locks with $\Phi_{ref} - \Phi_{out}/N = \pi/2$ for $Nf_{ref} = f_o$
  - Output range = $\pm\pi/2$ around an offset of $\pi/2$
  - PLL lock range = $f_o - \pi/2K_{pd}K_{vco} < f_{out} < f_o + \pi/2K_{pd}K_{vco}$
- Output contains $2f_{ref}$ and its harmonics
- Output = $2/\pi(\Delta\Phi - \pi/2) + \sum_n a_n \cos(4\pi n f_{ref} t + \alpha_n))$
- Periodic signal in addition to $K_{pd}\Delta\Phi$
- All real phase detectors have a periodic “error” in addition to the “dc” term proportional to phase error

XOR phase detector-Error spectrum

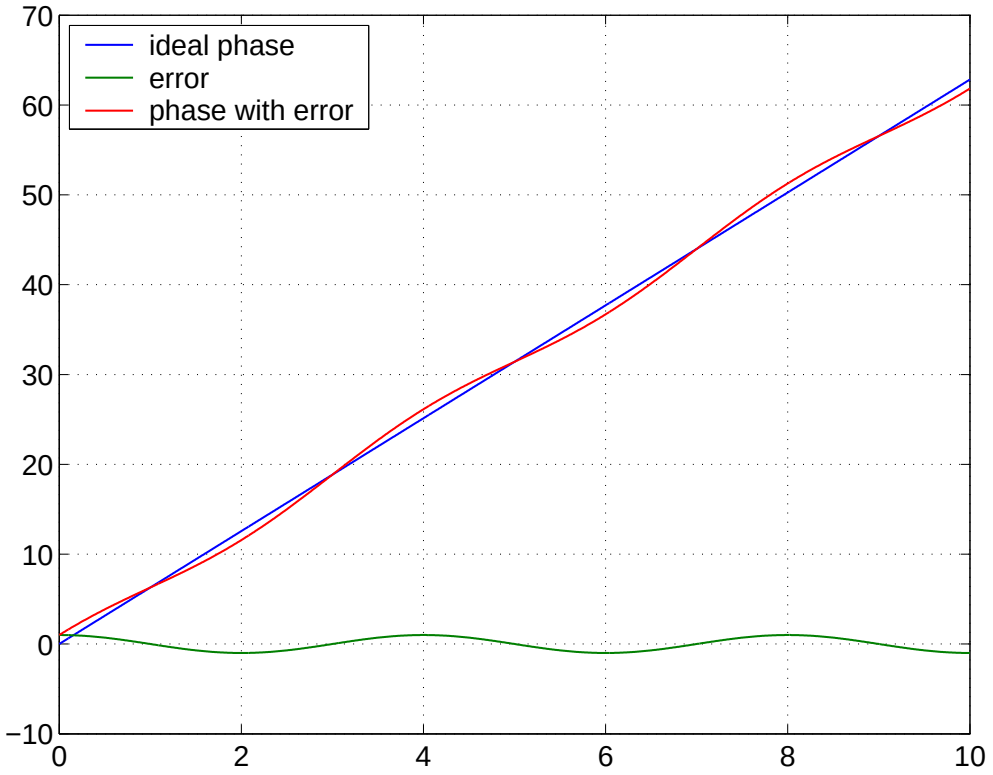


PLL with XOR phase detector

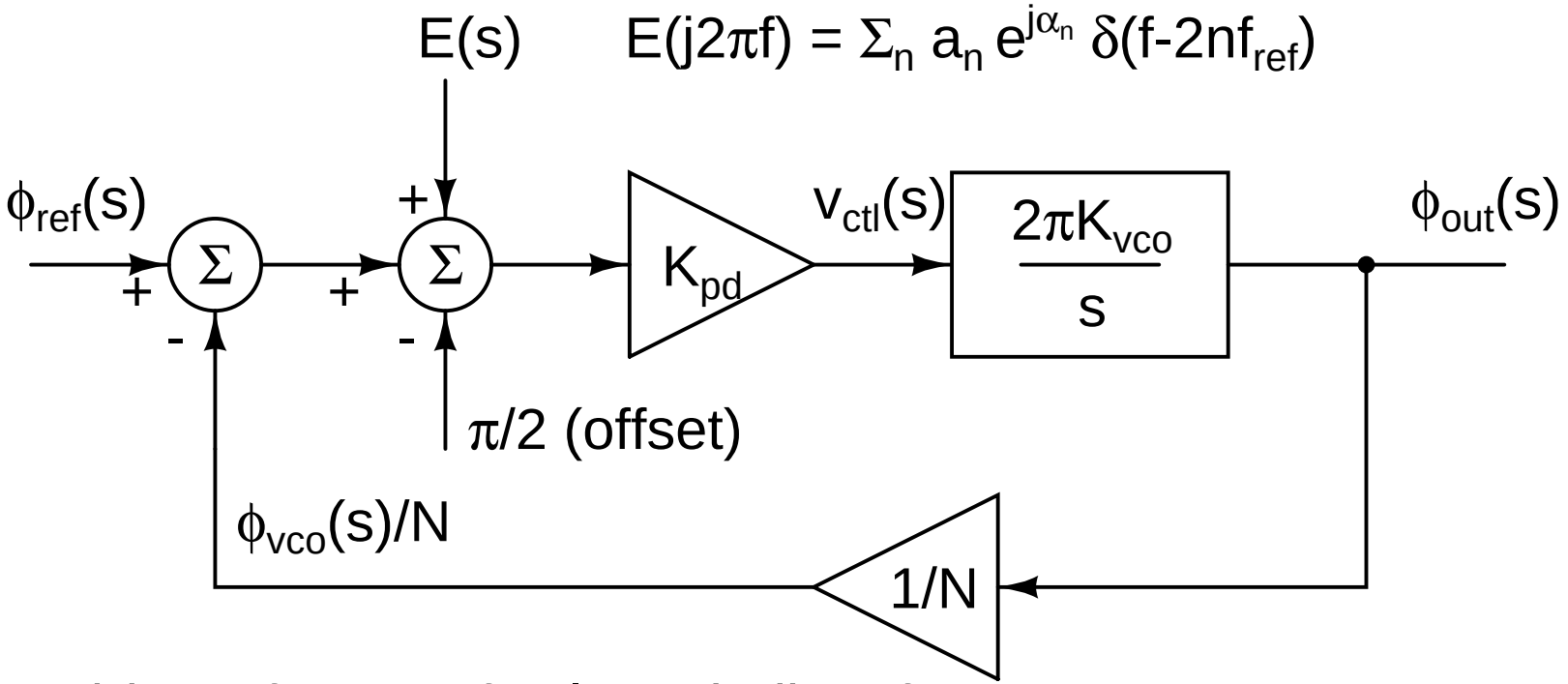


- Error $E(t)$ added to the input of the phase detector
- Disturbances in the vco phase $\phi_{out}(t)$, even with a perfect reference ($\phi_{ref}(t) = 0$)
- VCO output: $\cos(2\pi N f_{ref} t + N\Phi_{ref} - \pi/2 + \phi_{out}(t))$
- VCO output not periodic at Nf_{ref}

PLL with XOR phase detector



PLL with XOR phase detector—frequency domain



$\phi_{ref}(s) = 0$ for a perfectly periodic reference

- Transfer function from the error to the output
  $\phi_{out}(s)/E(s) = \phi_{out}(s)/\phi_{ref}(s) = N/1 + Ns/(2\pi K_{pd}K_{vco})$
- $E(j2\pi f) = \sum_n a_n \exp(j\alpha_n)\delta(f - 2nf_{ref})$

Type-I PLL

$$\frac{\phi_{out}(s)}{E(s)} = \frac{\phi_{out}(s)}{\phi_{ref}(s)} \quad (1)$$

$$= N\frac{2\pi K_{pd}K_{vco}/Ns}{1+2\pi K_{pd}K_{vco}/Ns} \quad (2)$$

$$= N\frac{1}{1+sN/2\pi K_{pd}K_{vco}} \quad (3)$$

$$(4)$$

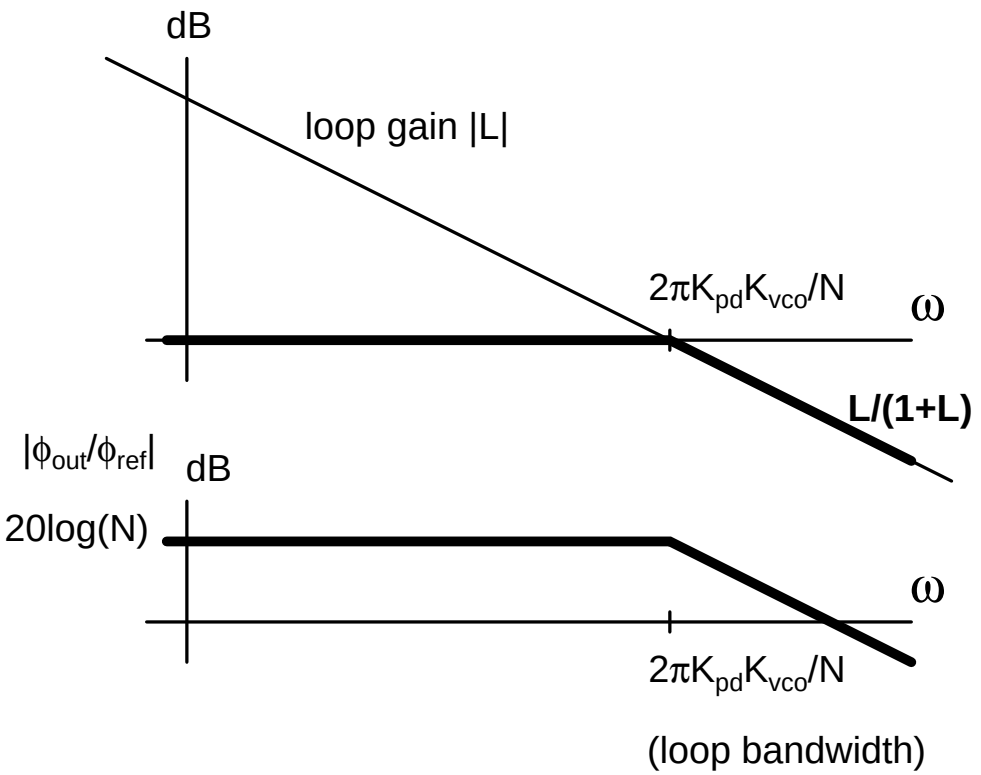
Loop gain

$$L(s) = \frac{2\pi K_{pd}K_{vco}}{Ns} \quad (5)$$

Closed loop bandwidth

$$f_{-3dB} = \frac{K_{pd}K_{vco}}{N} \quad (6)$$

Type I PLL


dB
loop gain |L|
$2\pi K_{pd}K_{vco}/N$
ω
L/(1+L)
$|\phi_{out}/\phi_{ref}|$
dB
20log(N)
ω
$2\pi K_{pd}K_{vco}/N$
(loop bandwidth)

Feedback system

In our system,

$$\frac{\phi_{out}(s)}{E(s)} = N\frac{2\pi K_{pd}K_{vco}/Ns}{1+2\pi K_{pd}K_{vco}/Ns} \quad (7)$$

In general, in a feedback system with a loop gain $L(s)$

$$H_{closedloop}(s) = H_{ideal}(s)\frac{L(s)}{1+L(s)} \quad (8)$$

$$(9)$$

Where $H_{ideal}(s)$ is the ideal closed loop gain (with $L = \infty$). This can be approximated as

$$H_{closedloop}(s) = H_{ideal}(s)L(s) \qquad |L| \ll 1 \quad (10)$$

$$= H_{ideal}(s) \qquad |L| \gg 1 \quad (11)$$

PLL with XOR phase detector—Output signal

Output phase error (constant phase offsets ignored)

$$\phi(j2\pi f) = \sum_n a_n H(j4\pi n f_{ref}) \exp(j\alpha_n)\delta(f - 2nf_{ref}) \quad (12)$$

$$= \sum_{n=1}^{\infty} b_n \exp(j\beta_n)\delta(f - 2nf_{ref}) \quad (13)$$

$$\phi(t) = \sum_{n=1}^{\infty} b_n \cos(4\pi n f_{ref} t + \beta_n) \quad (14)$$

$$V_{out}(t) = \cos(2\pi N f_{ref} t + \sum_{n=1}^{\infty} b_n \cos(4\pi n f_{ref} t + \beta_n)) \quad (15)$$

PLL with XOR phase detector—Output signal

Considering only the term at $2f_{ref}$, and $b_1 \ll 1$

$$
\begin{aligned}
V_{out}(t) &= \cos(2\pi N f_{ref} t + b_1 \cos(4\pi f_{ref} t + \beta_1)) && (16)\\
&= \cos(2\pi N f_{ref} t)\cos(b_1 \cos(4\pi f_{ref} t + \beta_1)) && (17)\\
&\quad - \sin(2\pi N f_{ref} t)\sin(b_1 \cos(4\pi f_{ref} t + \beta_1)) && (18)\\
&\approx \cos(2\pi N f_{ref} t) - b_1 \cos(4\pi f_{ref} t + \beta_1)\sin(2\pi N f_{ref} t) && (19)\\
&= \cos(2\pi N f_{ref} t) - b_1/2 \sin(2\pi(N+2) f_{ref} t + \beta_1) && (20)\\
&\quad - b_1/2 \sin(2\pi(N-2) f_{ref} t + \beta_1) && (21)
\end{aligned}
$$

- Spurious tones in the output at $2f_{ref}$ from the desired frequency
- Reference feedthrough
- In general, spurious tones will be present at nf_{ref} from the desired PLL output

Reference feedthrough

$$b_1 = a_1|H(j4\pi f_{ref})| \quad (22)$$

$$= a_1 N \left| \frac{K_{pd}K_{vco}/j2Nf_{ref}}{1 + K_{pd}K_{vco}/j2Nf_{ref}} \right| \quad (23)$$

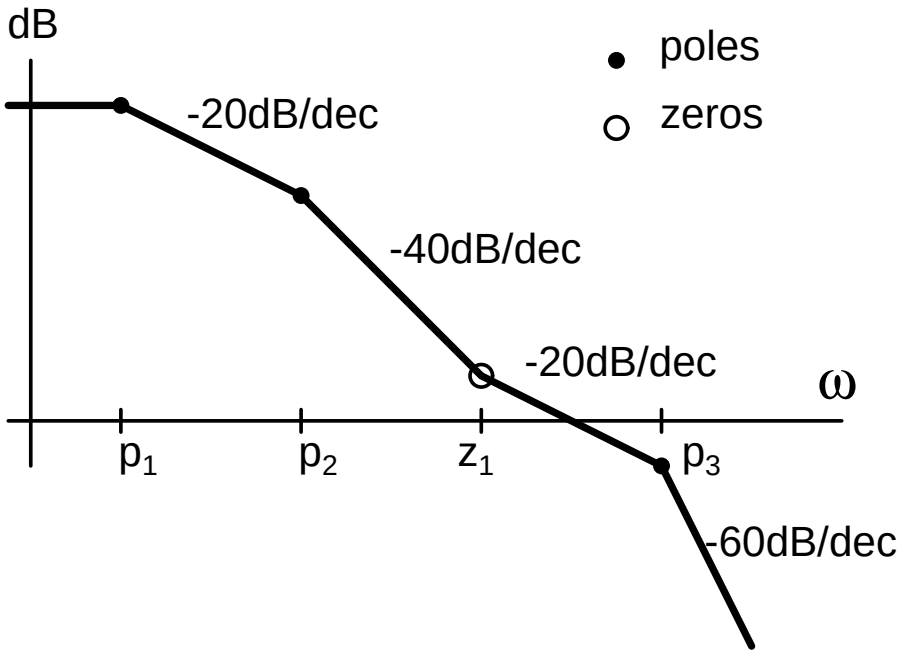
$$\approx a_1 N \left| \frac{K_{pd}K_{vco}}{j2Nf_{ref}} \right| \quad (24)$$

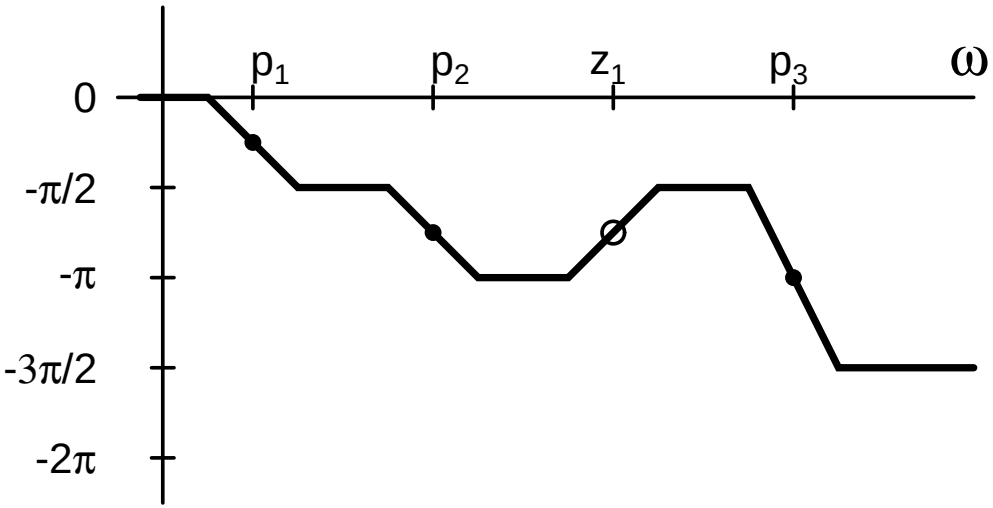
$$\frac{4}{\pi} N \frac{f_{-3dB}}{2f_{ref}} \quad (25)$$

Reference feedthrough—example

- To generate 1 GHz from 1 MHz reference
  - $b_1 = 10^{-2}$ (spurious tones 46 dB below the oscillation level
  - $N = 10^3$
- $f_{-3dB}/f_{ref} = \pi/2 \times 10^{-5} \Rightarrow f_{-3dB} = 5\pi$ Hz
- Lock range $= \pi N f_{-3dB} \approx 50$ kHz
- Lock range is too small; It can't switch to the next channel which is 1 MHz away!

Relationship between magnitude and phase [Bode]



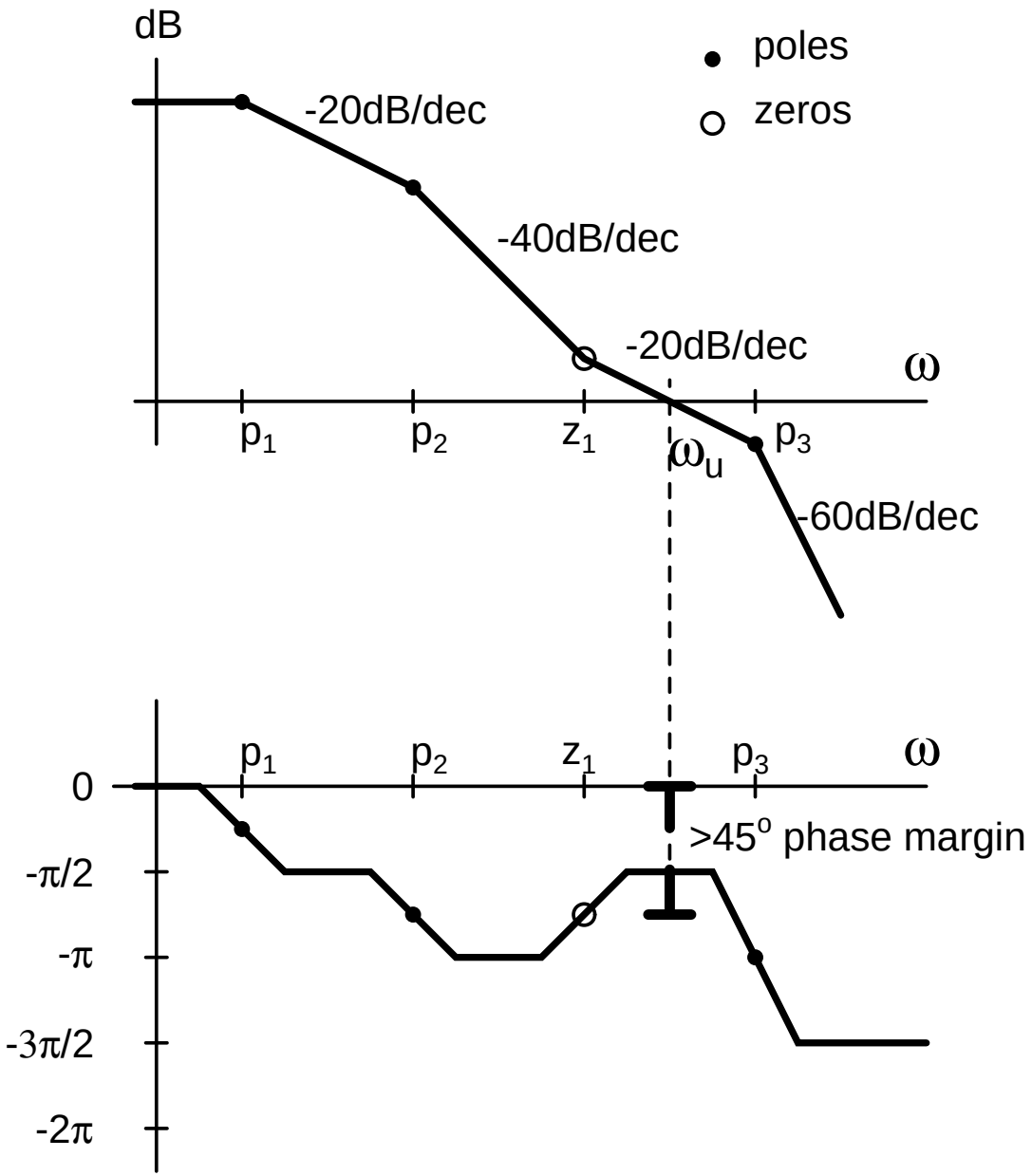


Relationship between magnitude and phase [Bode]

All poles and zeros of the network assumed to be real and in the left half plane.

- The magnitude plot(log-log) consists of segments of slope $20k$ dB/decade
- Poles and zeros form breakpoints between segments
- At each pole the slope increments by -20 dB/decade
- At each zero the slope increments by +20 dB/decade
- Phase at poles/zeros will be $m\pi/4$ radians
- Derivative of phase is positive at a zero and negative at a pole

Stability criteria for negative feedback loops

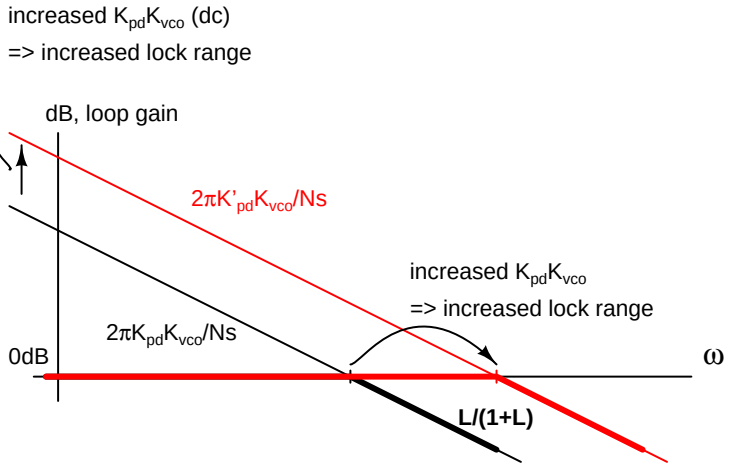


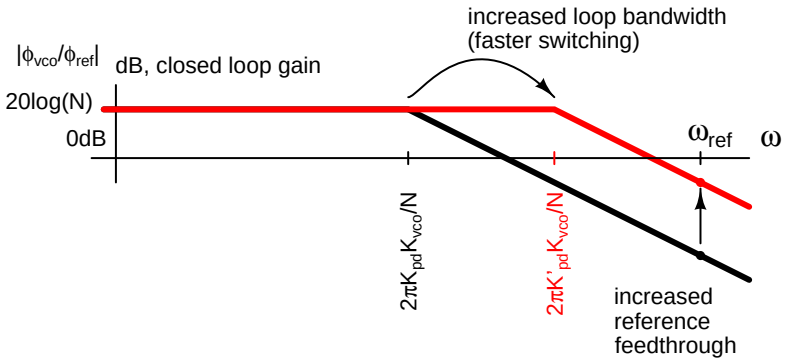
Stability criteria for negative feedback loops

All poles and zeros of the loop gain function assumed to be real and in the left half plane.

- Phase margin should be greater than a specified amount (assume 45°)
- Phase lag at ω_u should be less than 125°
- At ω_u, the Bode plot should have a slope of -20 dB/decade

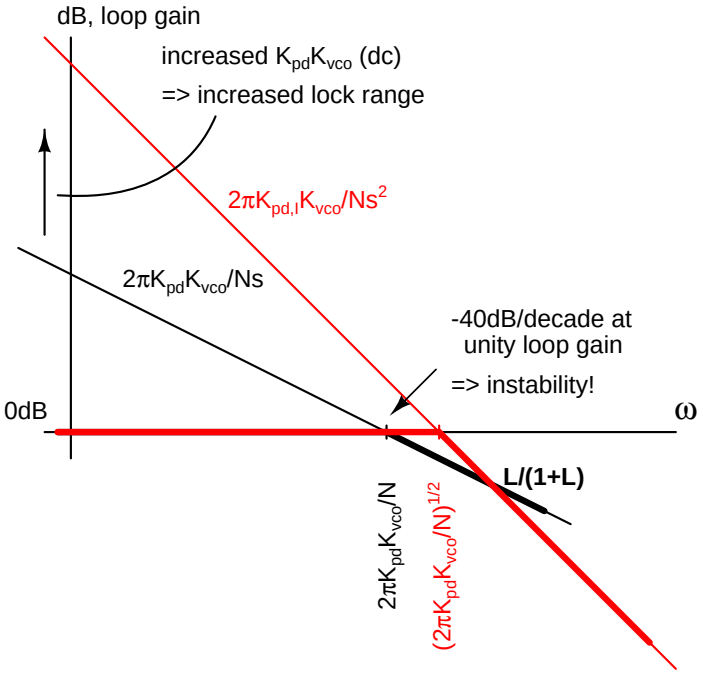
Increasing the lock range of the phase detector-I

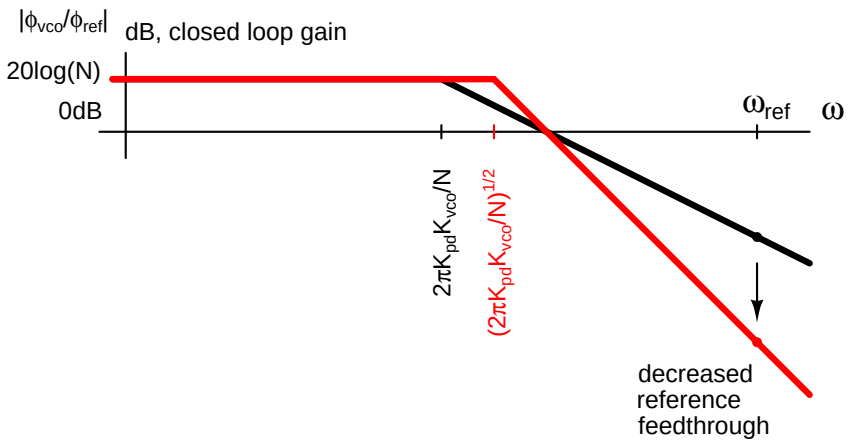




- Increase $K_{pd}K_{vco}$ at all frequencies
- Causes increased reference feedthrough

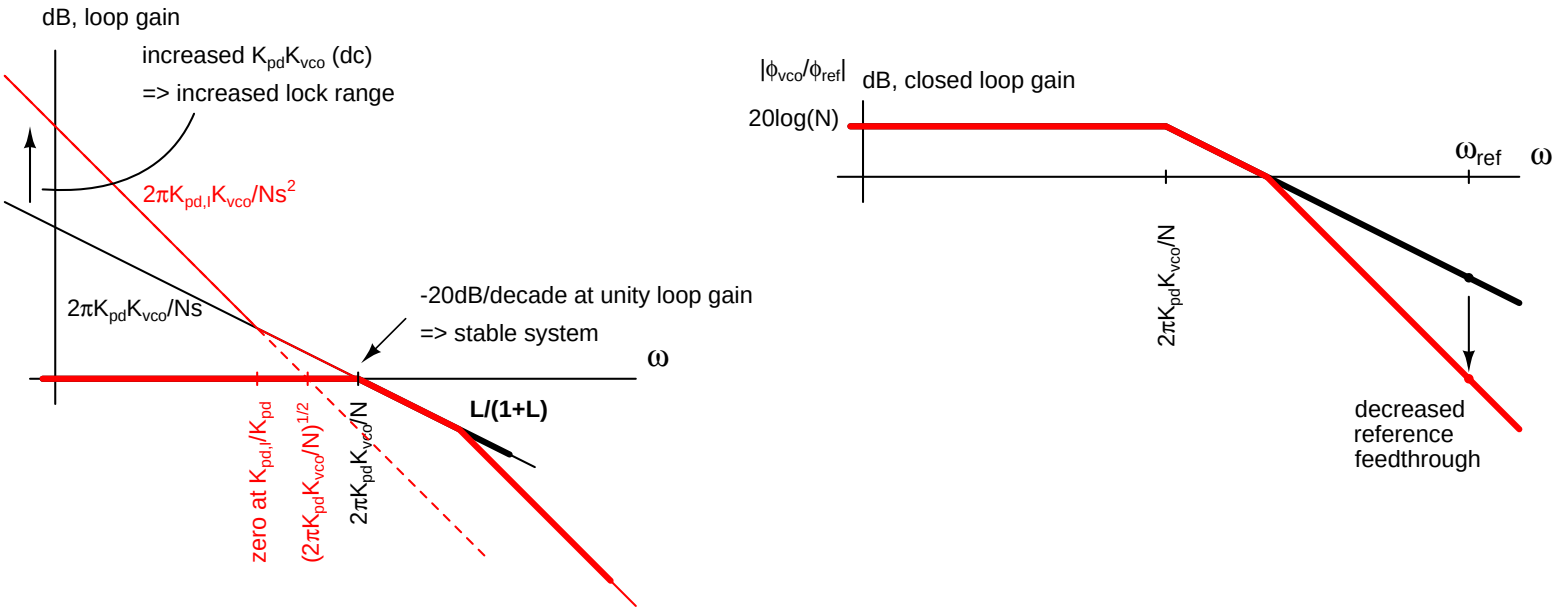
Increasing the lock range of the phase detector-II





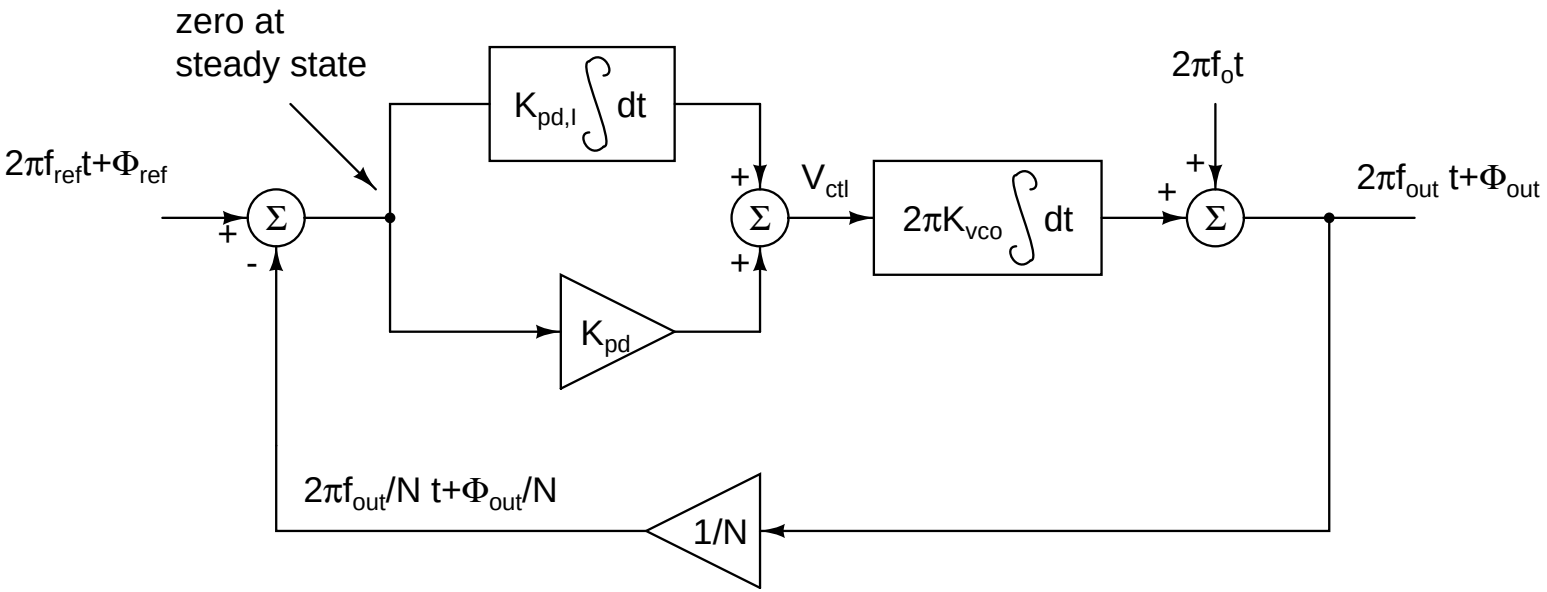
- Increase $K_{pd}K_{vco}$ only at dc (steady state phase error reduces)
- In the limit, use an integrator $K_{pd,I}/s \Rightarrow$ steady state phase error reduces to zero
- Two integrators in a loop $\Rightarrow$ unstable system
- Increased attenuation slope can reduce reference feedthrough

Increasing the lock range of the phase detector-III



- Increase $K_{pd}K_{vco}$ only at dc (steady state phase error reduces)
- In the limit, use an integrator $K_{pd,I}/s \Rightarrow$ steady state phase error reduces to zero
- Maintain -20 dB/decade slope at unity loop gain $\Rightarrow$ introduce a zero before ω_u
- Introduce a pole beyond ω_u to increase attenuation of reference feedthrough

Type II PLL—with two poles and a zero

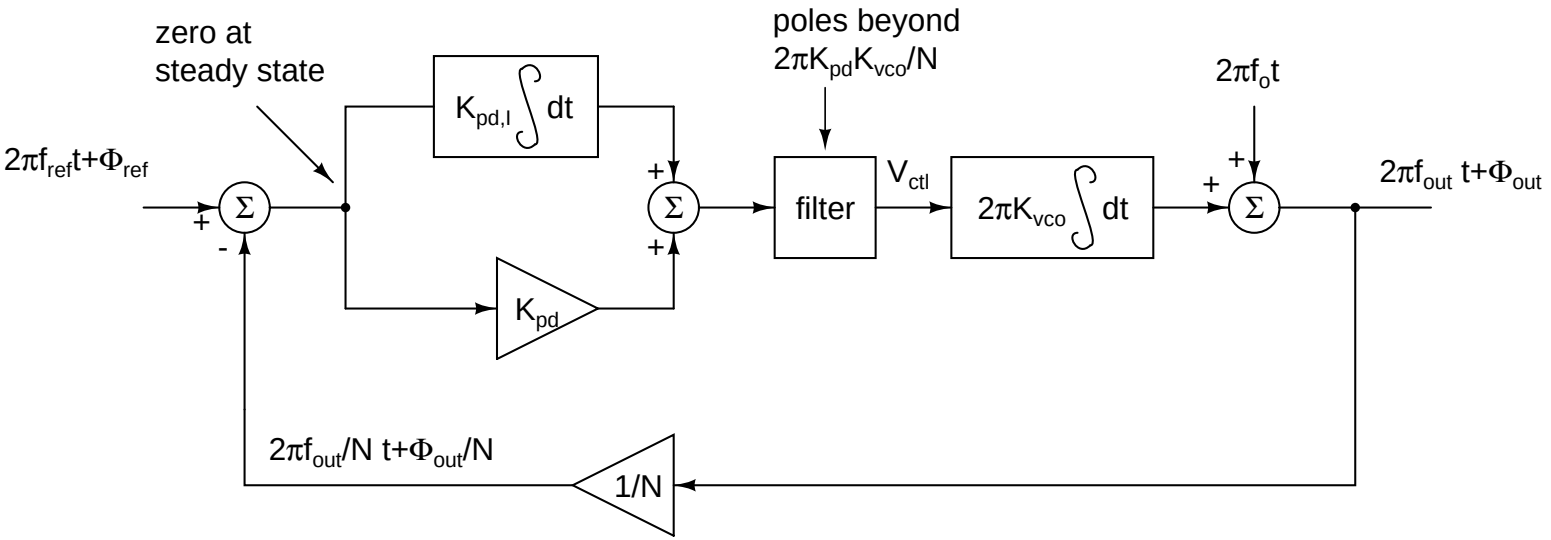


$dV_{ctl}/dt \ \alpha \ 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $\Phi_{ref} - \Phi_{out}/N = 0$;

- At steady state, reference input and divider output have the same frequency and phase
- The integrator's output stabilizes to the value required to make the VCO to oscillate at Nf_{ref}
- At steady state, $V_{ctl} = (Nf_{ref} - f_o)/K_{vco}$

Type II PLL—Additional attenation poles

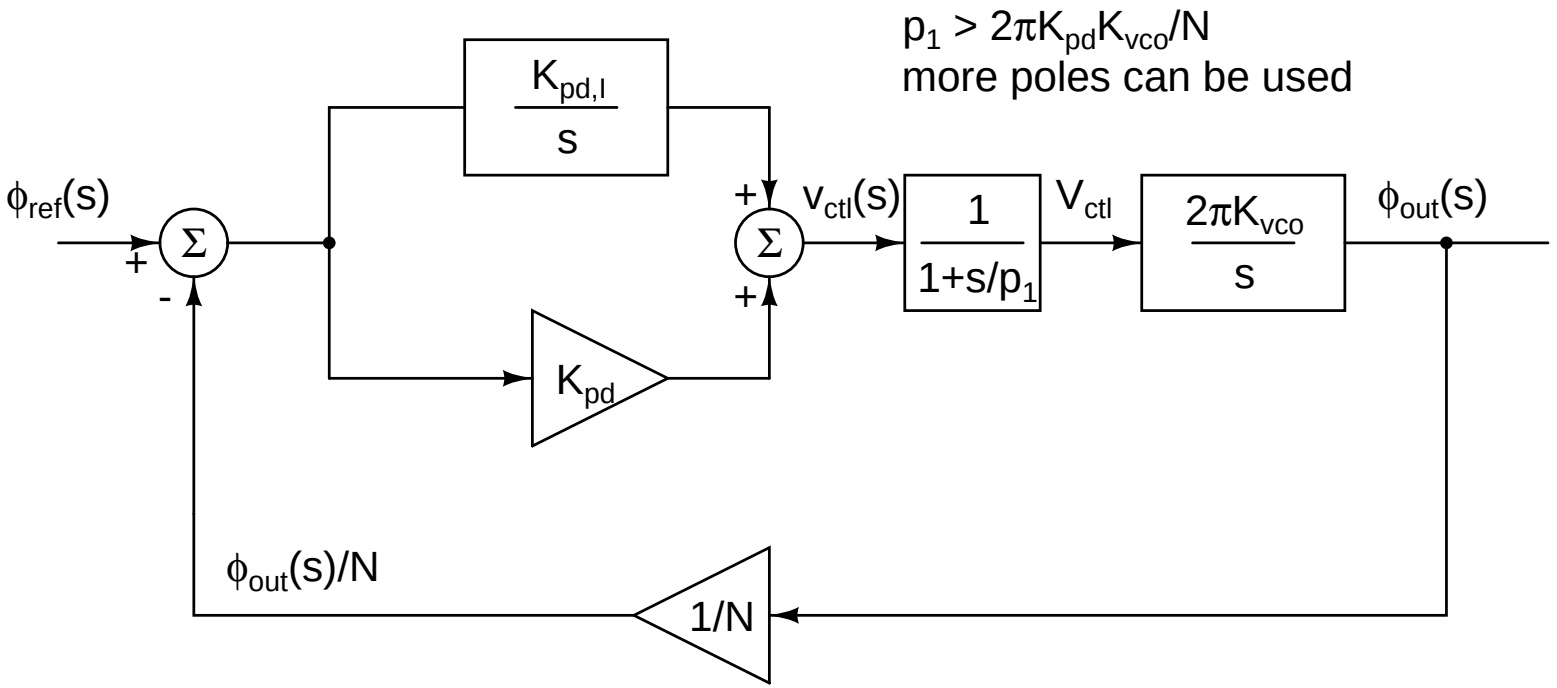


$dV_{ctl}/dt \; \alpha \; 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

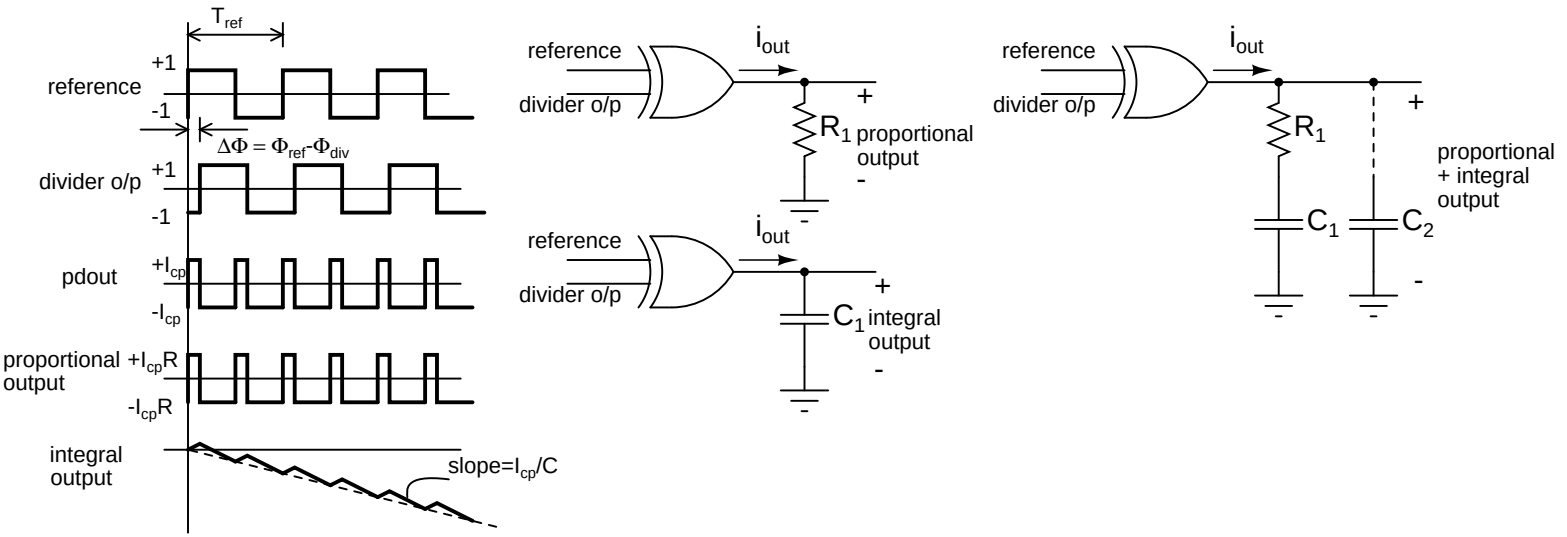
At steady state, $f_{ref}=f_{out}/N$; $\Phi_{ref} - \Phi_{out}/N = 0$;

- Additional poles beyond the unity loop gain frequency to reduce reference feedthrough

Type II PLL—Frequency domain

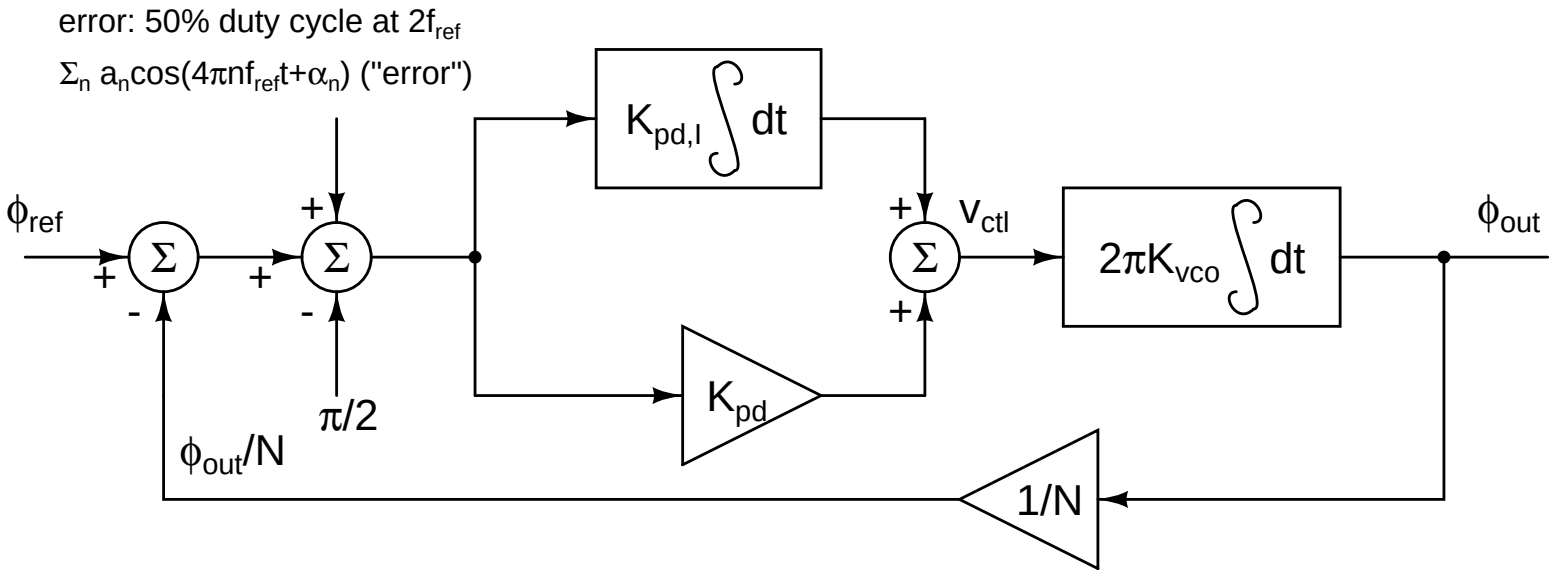


Type II PLL—Implementation



- XOR gate with a current output ($\pm I_{cp}$)
  - Integral term $K_{pd,I}/s$: Current flowing into a capacitor C_1
  - Proportional term K_{pd}: Current flowing into a resistor R_1
  - Series RC to obtain the sum
- Additional capacitor C_2 to introduce the second pole

Type II PLL with an XOR phase detector

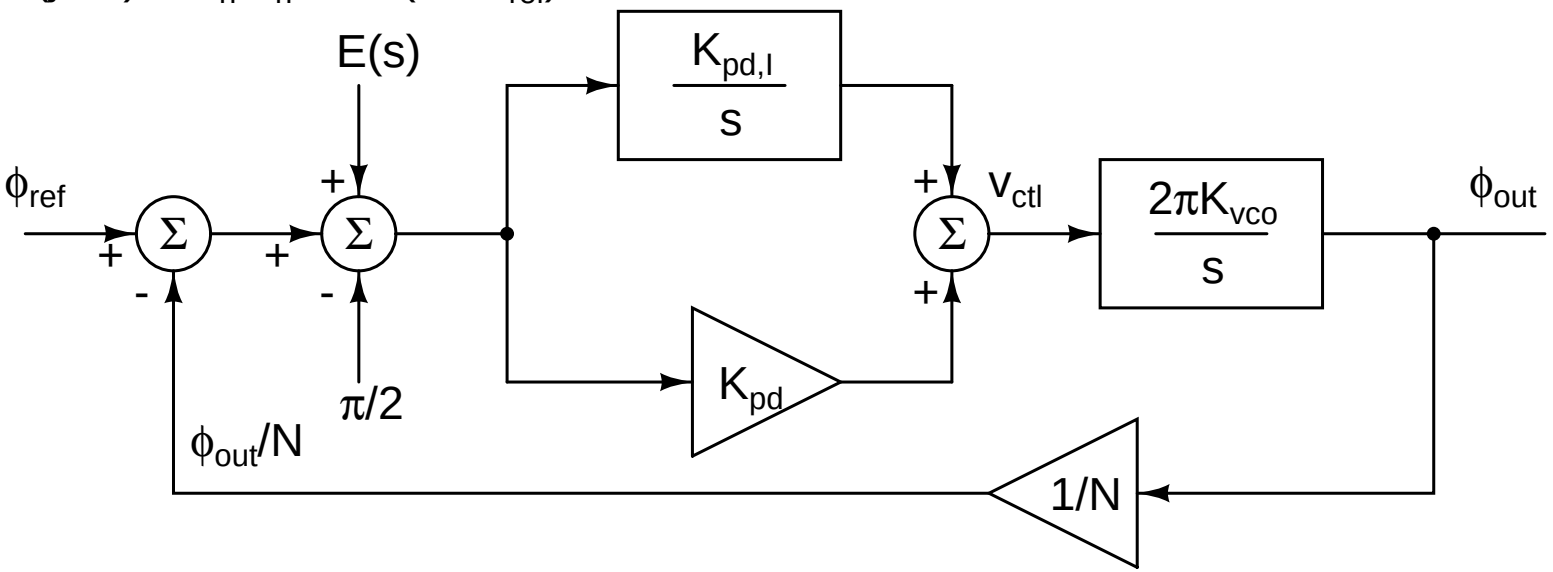


- Loop locks with $\pi/2$ offset between ϕ_{ref} and ϕ_{vco}/N for all frequencies
- Periodic error $E(t)$ is a 50% duty cycle square wave at $2f_{ref}$

$$E(t) = 2\sum_{n=1}^{\infty} \text{sinc}\left(\frac{n}{2}\right) \cos(4\pi n f_{ref} t - n\pi/2)$$

Type II PLL with an XOR phase detector-Frequency domain

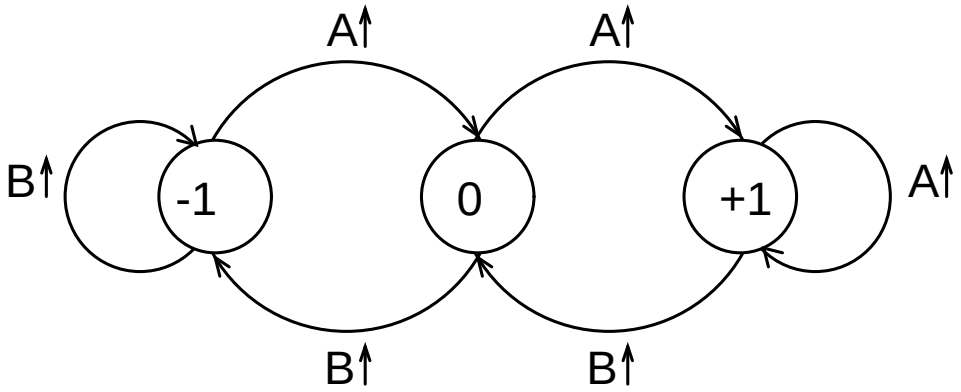
$E(j2\pi f) = \Sigma_n a_n e^{j\alpha_n} \delta(f-2nf_{ref})$

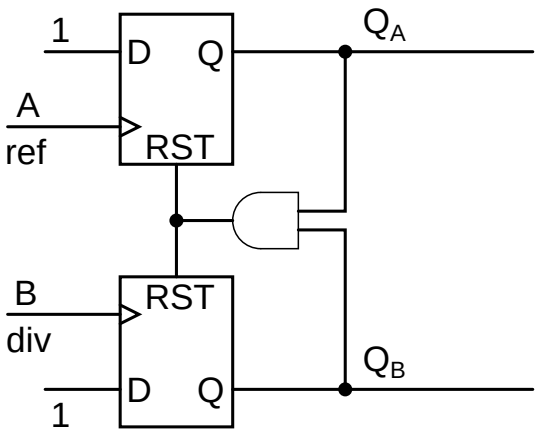


Type II PLL with an XOR phase detector

- Lock range is not limited by phase detector
- Large error signal even under lock $\Rightarrow$ significant reference feedthrough
- XOR output sensitive to duty cycle of inputs
- Better to have a phase detector with zero output for zero phase error
- Better to have a phase detector sensitive only to the edges
- Loop bandwidth can be widened while maintaining low reference feedthrough

Tri state phase detector

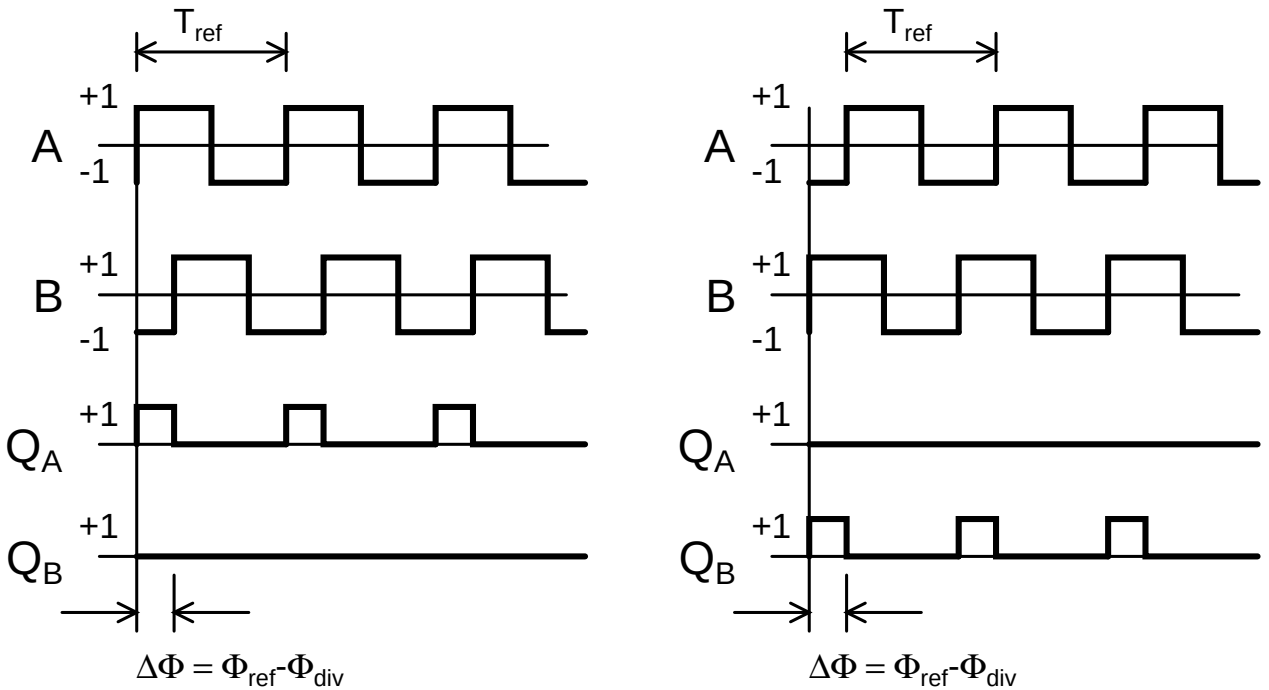




output=Q_A-Q_B

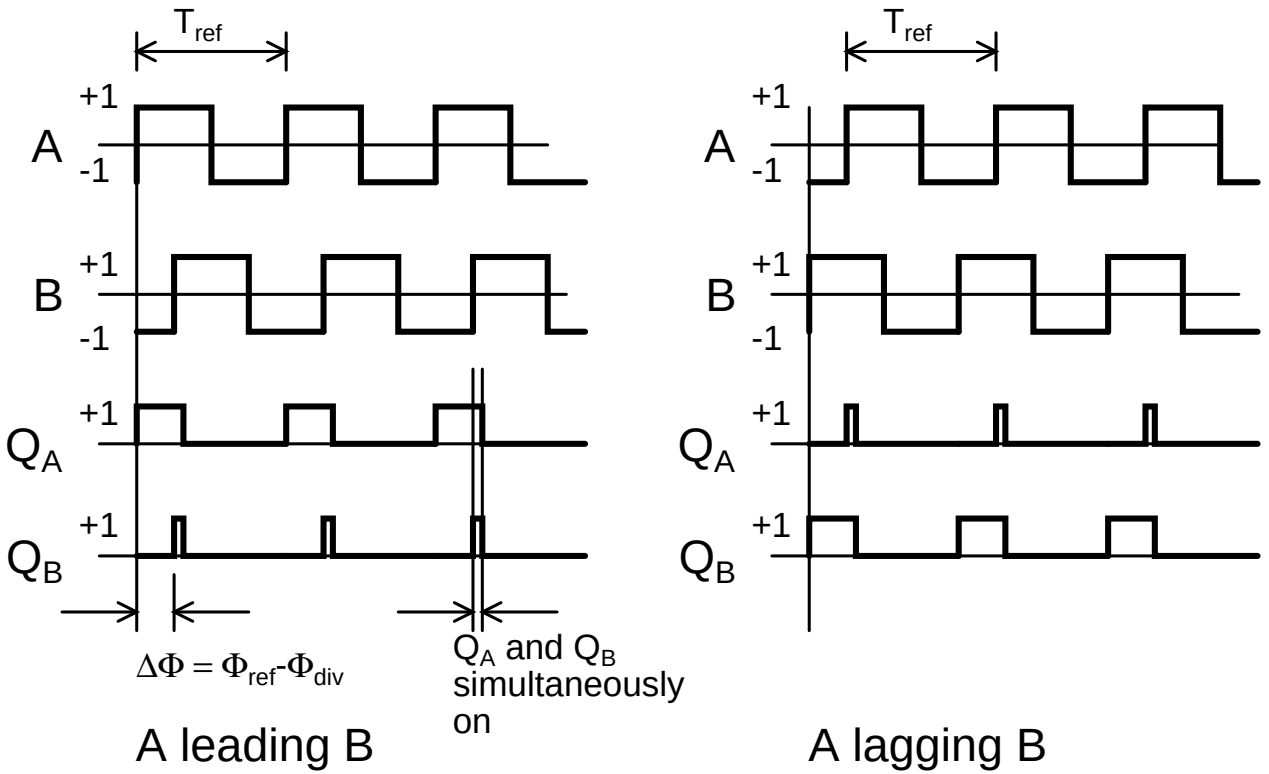
- Output $+1, -1, 0$
  - $+1$ if reference leads divider output
  - -1 if reference lags divider output
  - 0 if reference coincides with divider output

Tri state phase detector-waveforms



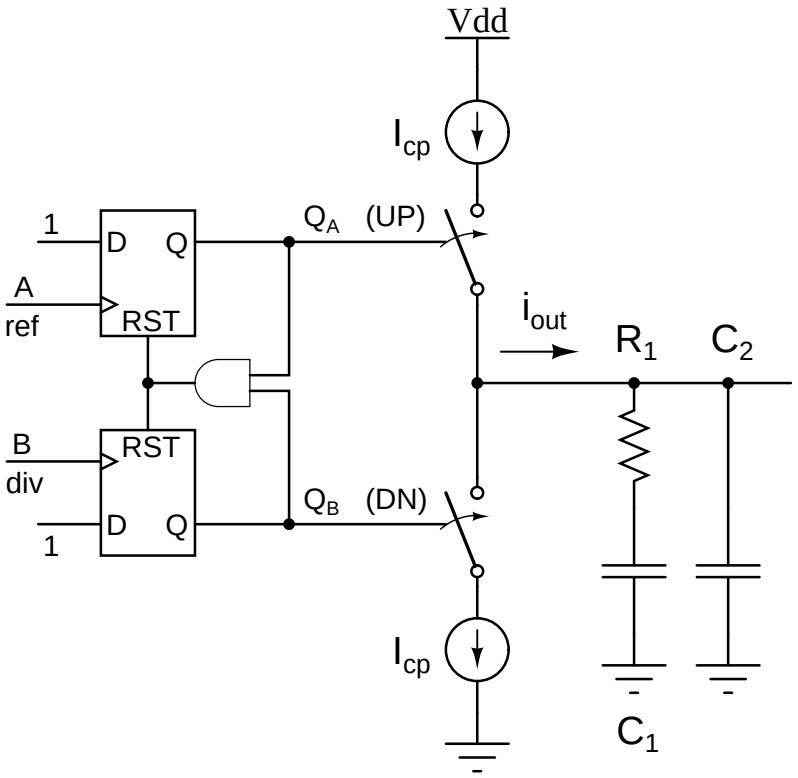
- Flip flops assumed to be reset instantaneously

Tri state phase detector-reset path delay



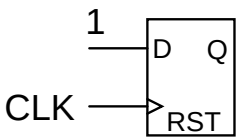
- Q_A and Q_B simultaneously high for a short duration
- $Q_A - Q_B$ proportional to $\Delta\Phi$

Tri state phase detector with charge pump

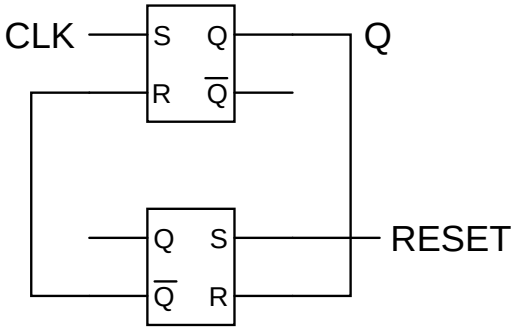


- Q_A and Q_B drive a charge pump
- Average current driven into the loop filter is $I_{cp}\Delta\Phi/2\pi$

Tri state phase detector implementation

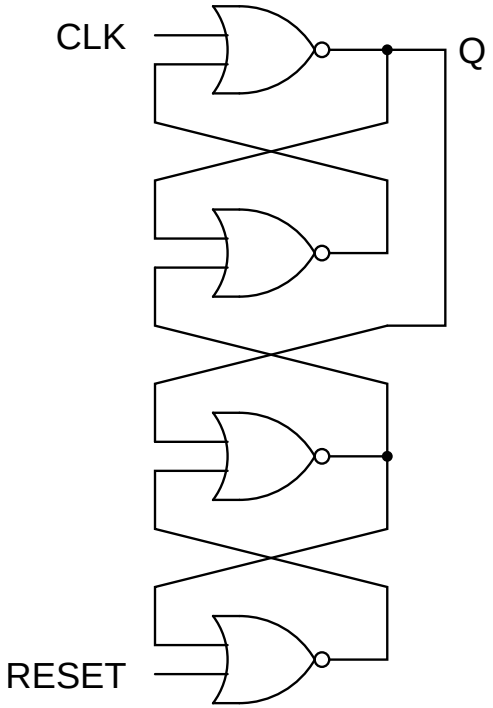


D latch with reset and D="1"



(D input with "1" implicit)

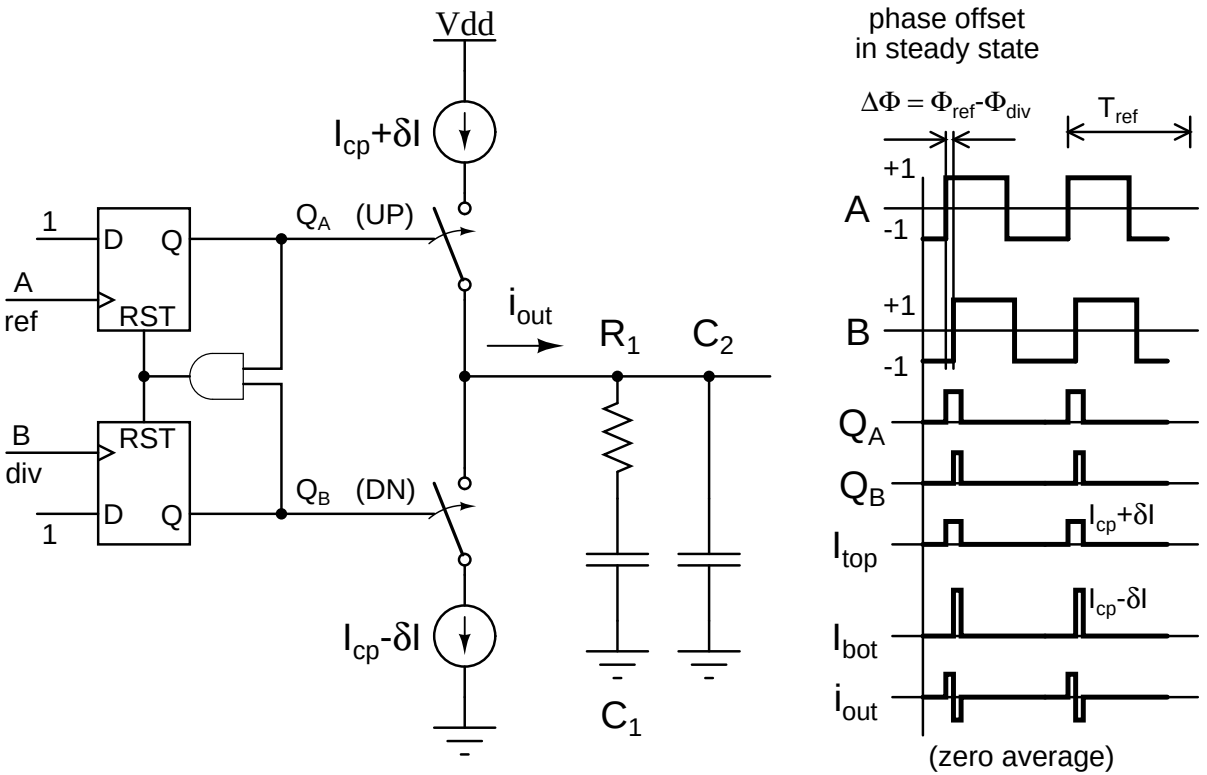
Realization using SR latches



Realization using NOR gates

- D flip flops with reset implemented using SR latches

Tri state phase detector-Current source mismatch



- Ideally $\Delta\Phi = 0$ under lock in a type-II loop $\Rightarrow$ no reference feedthrough (loop filter input $= 0$)
- Mismatch between top and bottom current sources causes a non zero $\Delta\Phi = 0$ and reference feedthrough

Type-II PLL: transfer functions

$$L(s) = \frac{2\pi K_{pd,I} K_{vco}}{N s^2}(1 + s K_{pd}/K_{pd,I}) \tag{26}$$

$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = N \frac{1 + s K_{pd}/K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1} \tag{27}$$

$$\frac{\phi_{out}(s)}{V_{n,ctl}(s)} = \frac{N}{K_{pd}} \frac{s K_{pd}/K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1} \tag{28}$$

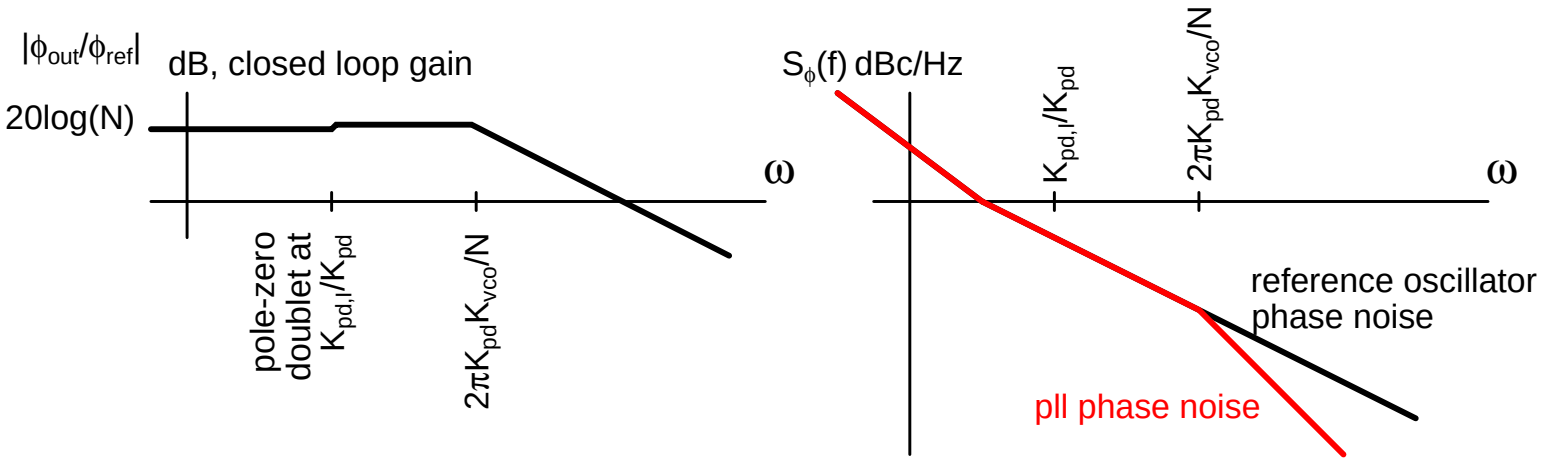
$$\frac{\phi_{out}(s)}{\phi_{vco}(s)} = \frac{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1} \tag{29}$$

Type-II PLL: transfer functions

$$\frac{L(s)}{1+L(s)} = \frac{1 + sK_{pd}/K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s\frac{K_{pd}}{K_{pd,I}} + 1} \tag{30}$$

- 2 poles and a zero
- Zero $z_1 = -K_{pd,I}/kpd$
- Natural frequency $\omega_n = \sqrt{2\pi K_{pd,I} K_{vco}/N}$
- Quality factor $Q = \sqrt{NK_{pd,I}/2\pi K_{vco}}/K_{pd}$, damping factor $\zeta = 1/2Q = K_{pd}/2\sqrt{NK_{pd,I}/2\pi K_{vco}}$
- For well separated (real) poles, $p_1 \approx -K_{pd,I}/kpd$, $p_1 \approx -2\pi K_{pd} K_{vco}/N + K_{pd,I}/kpd$,
- Pole zero doublet p_1, z_1; p_1 at a slightly higher frequency than z_1

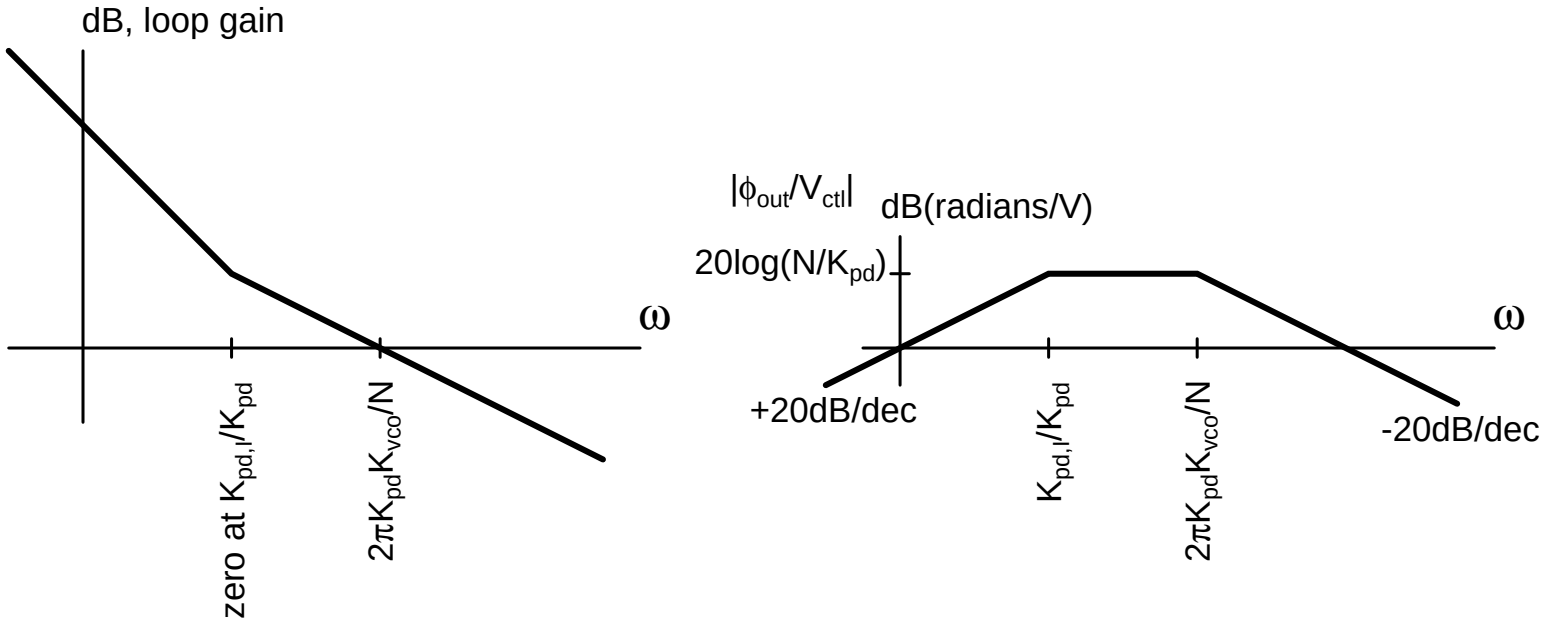
Type-II PLL: Reference input



$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = N\frac{1+sK_{pd}/K_{pd,I}}{s^2\frac{N}{2\pi K_{pd,I}K_{vco}}+s\frac{K_{pd}}{K_{pd,I}}+1} \quad (31)$$

- Low pass response; Reference noise attenuated at high frequencies
- Low frequency gain of N, -3 dB bandwidth of $2\pi K_{pd}K_{vco}/N$
- Pole zero doublet $p_1 \approx z_1 = K_{pd,I}/kpd$; p_1 at a slightly higher frequency than z_1

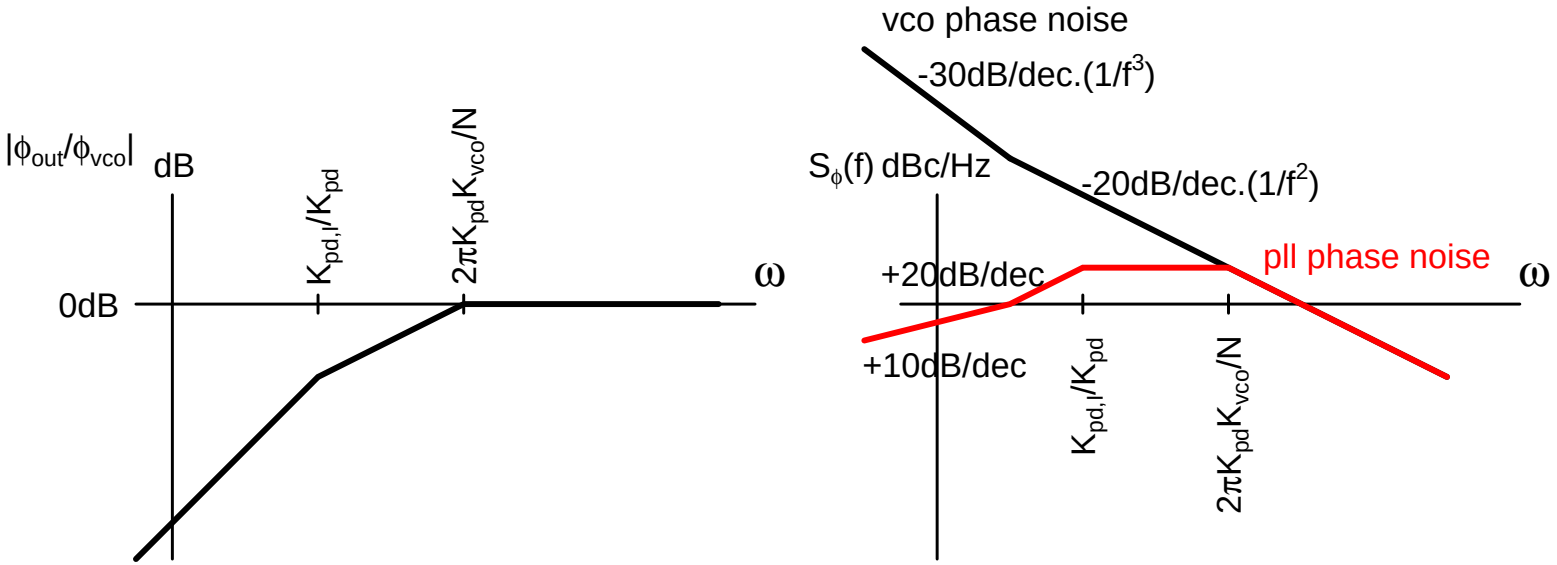
Type-II PLL: Noise added to control node



$$\frac{\phi_{out}(s)}{V_{ctl}(s)} = \frac{N}{K_{pd}} \frac{sK_{pd}/K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s\frac{K_{pd}}{K_{pd,I}} + 1} \quad (32)$$

- radians/Volt
- Bandpass response
- Mid band gain of N/K_{pd}
- Lower cutoff at $K_{pd,I}/kpd$, Upper cutoff at $2\pi K_{pd}K_{vco}/N$

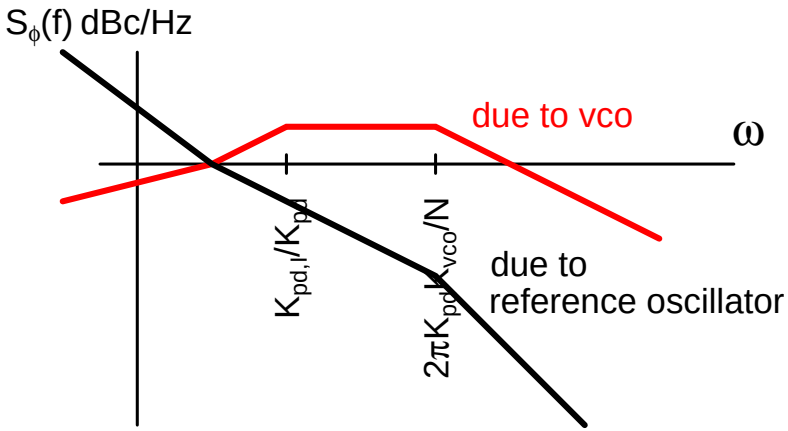
Type-II PLL: VCO noise

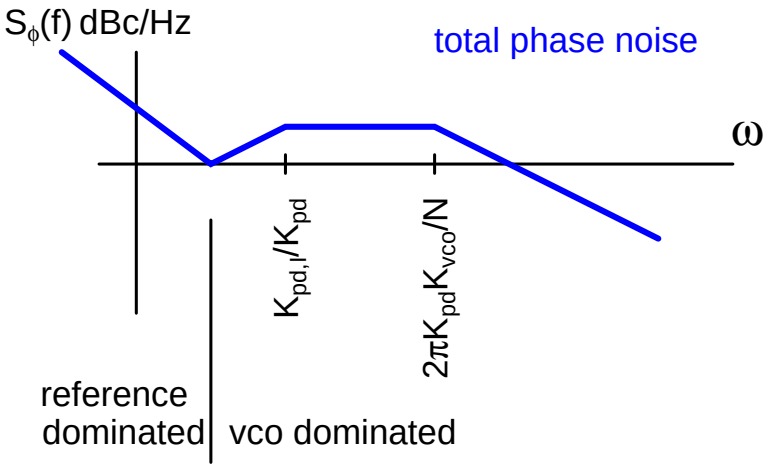


$$\frac{\phi_{out}(s)}{\phi_{vco}(s)} = \frac{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1} \qquad (33)$$

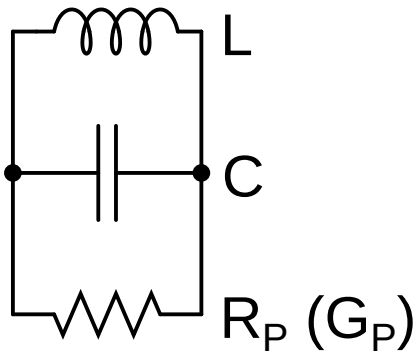
- Second order highpass response
- Feedback loop effectively inactive beyond $2\pi K_{pd} K_{vco} / N$

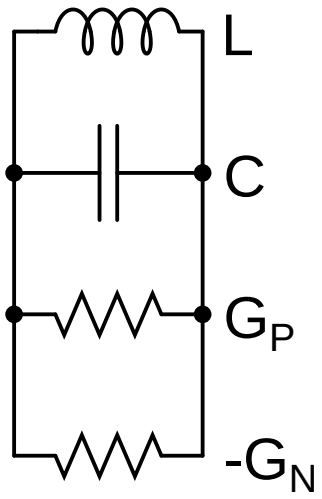
Type-II PLL phase noise example





LC oscillator



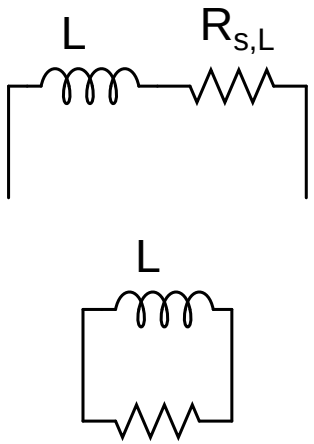


$G_N \geq G_P$

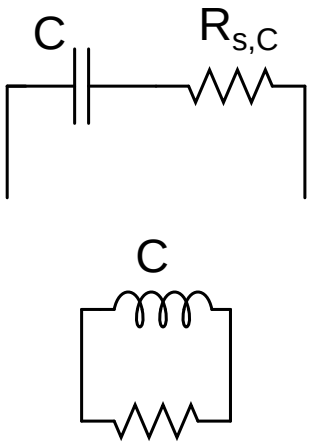
for sustained oscillation

- Lossless LC resonator sustains a sinusoidal voltage indefinitely
- LC resonator loss modeled using a parallel resistance R_p
- Compensate the loss of a lossy LC resonator using a parallel negative resistance
- Oscillation frequency $f_o = 1/2\pi\sqrt{LC}$

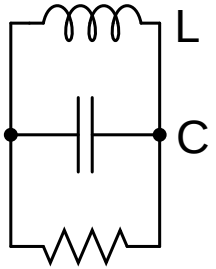
LC resonator losses



$R_{P,L} = (\omega L)^2/R_{s,L} \cong Q_L^2 R_{s,L}$



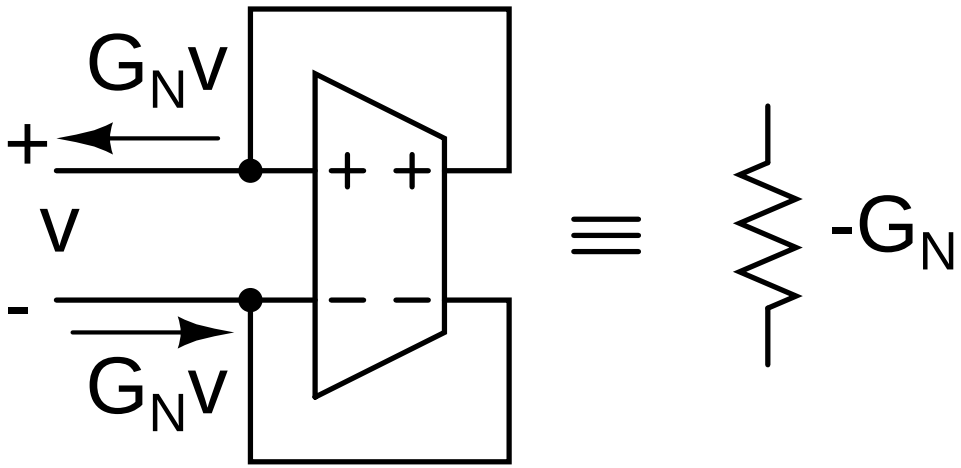
$R_{P,C} = 1/(\omega L)^2 R_{s,C} \cong Q_C^2 R_{s,C}$



$R_P = R_{P,L} || R_{P,C}$

- Capacitor and Inductor series resistances represented by equivalent parallel resistances
- Effective R_p is a parallel combination of losses from all components

Negative resistance-implementation

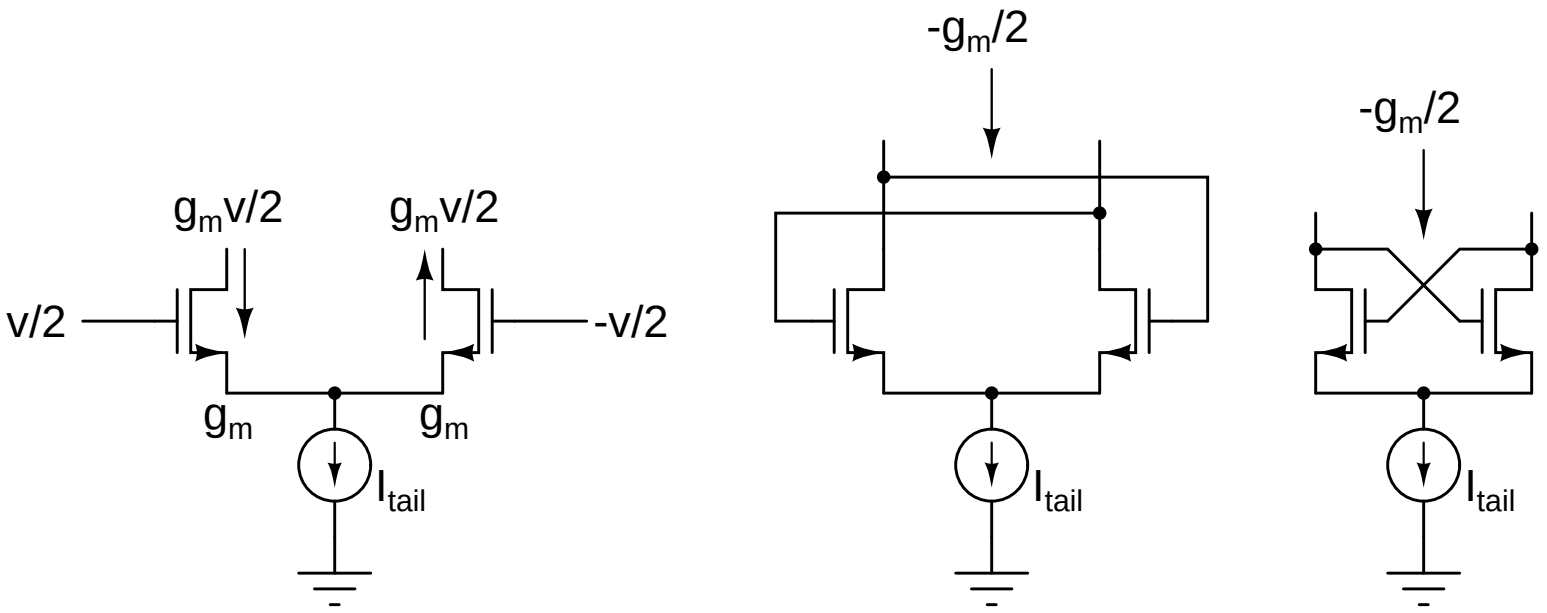


transconductance G_N

in positive feedback

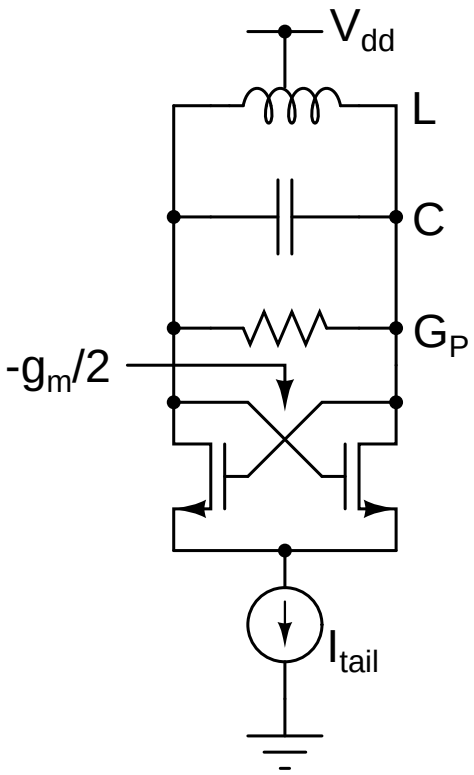
- Transconductor connected in positive feedback

Negative resistance-implementation



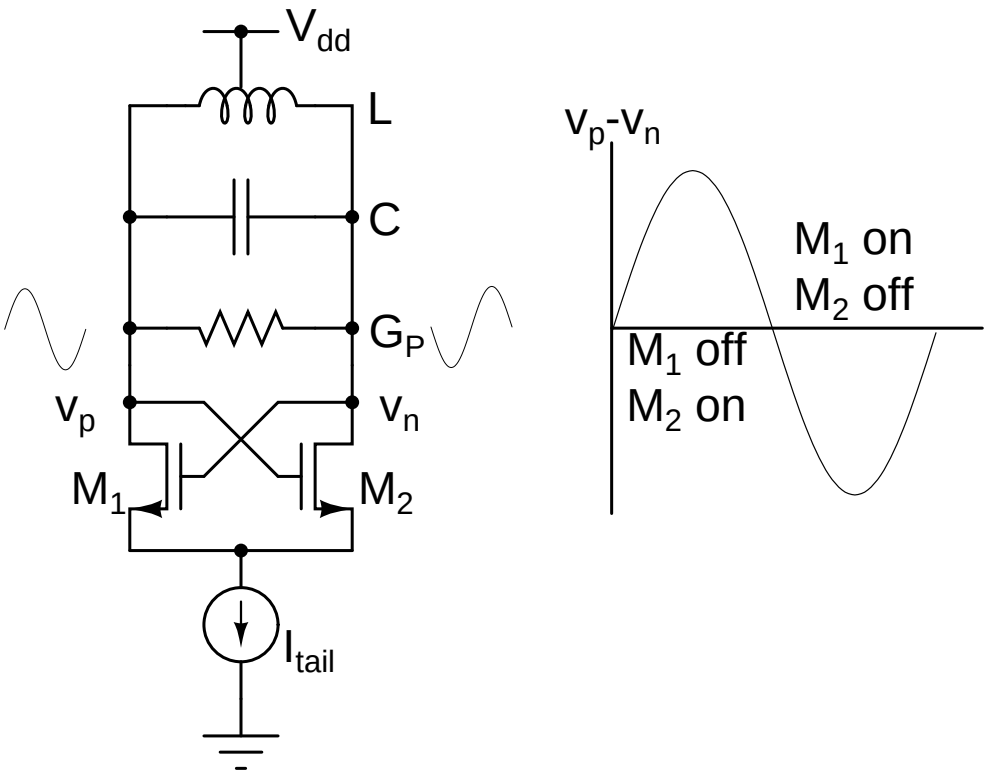
- Cross coupled differential pair
- Negative conductance $= g_m/2$ where g_m is the transconductance of each MOS device

LC oscillator



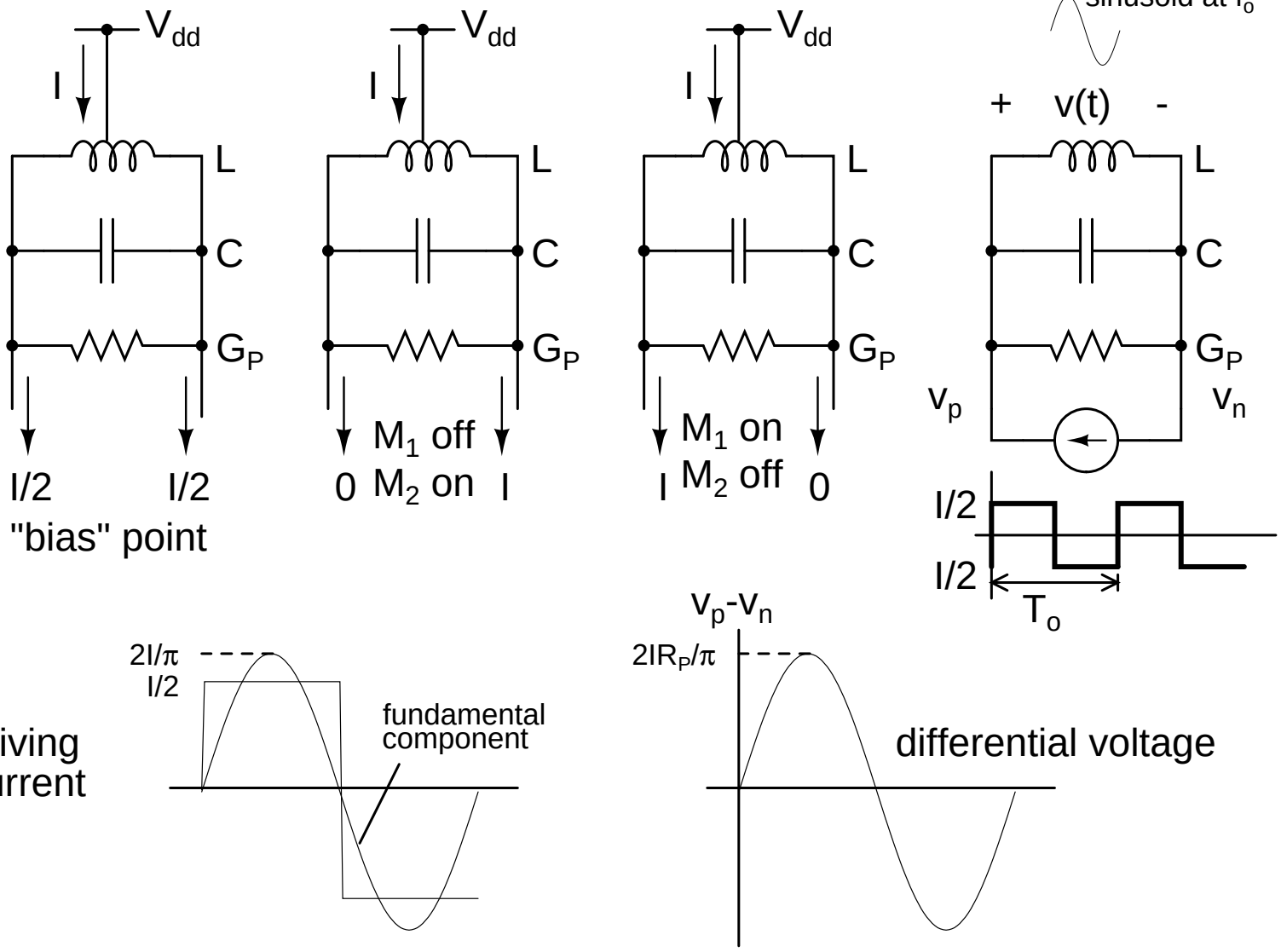
- Parallel LC tank with cross coupled differential pair
- This and its variants are the most commonly used topologies of CMOS integrated oscillators

LC oscillator-amplitude



- Complete switching of MOS devices assumed
- Equivalent to a square wave current of amplitude $I/2$ driving the parallel LC tank

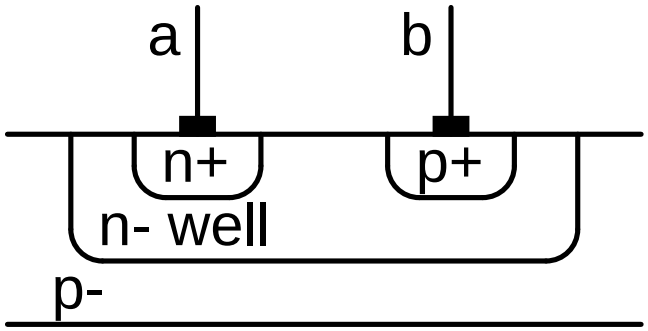
LC oscillator-amplitude

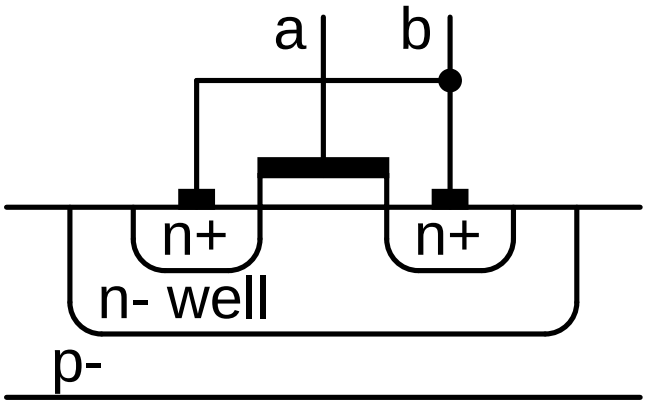


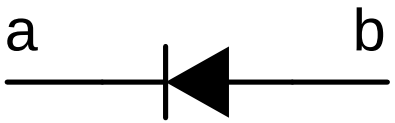
LC oscillator-amplitude

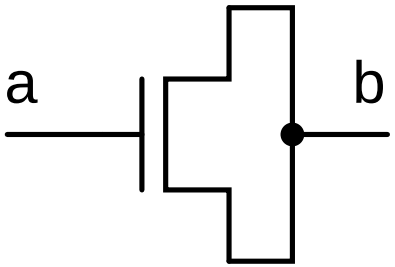
- Equivalent to a square wave current of amplitude $I/2$ driving the parallel LC tank
- All components except the fundamental filtered out
- Amplitude of the differential sinusoidal voltage = $2IR_P/\pi$

LC oscillator-tunability



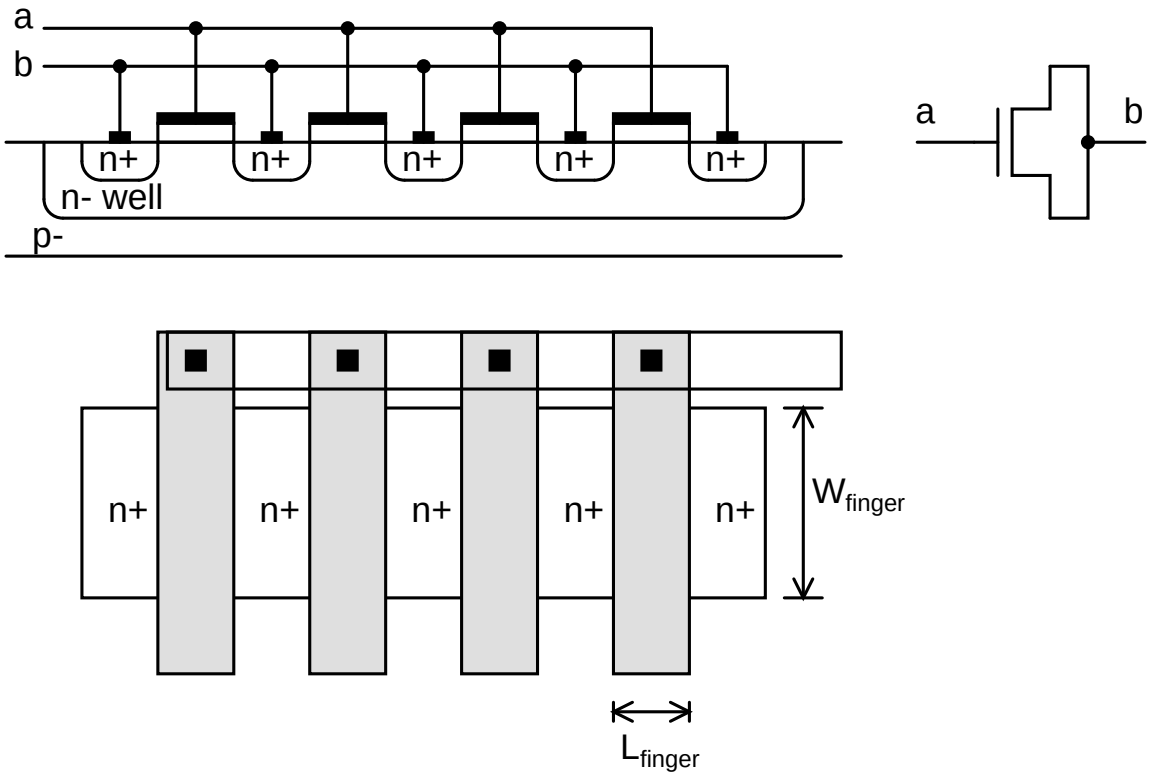






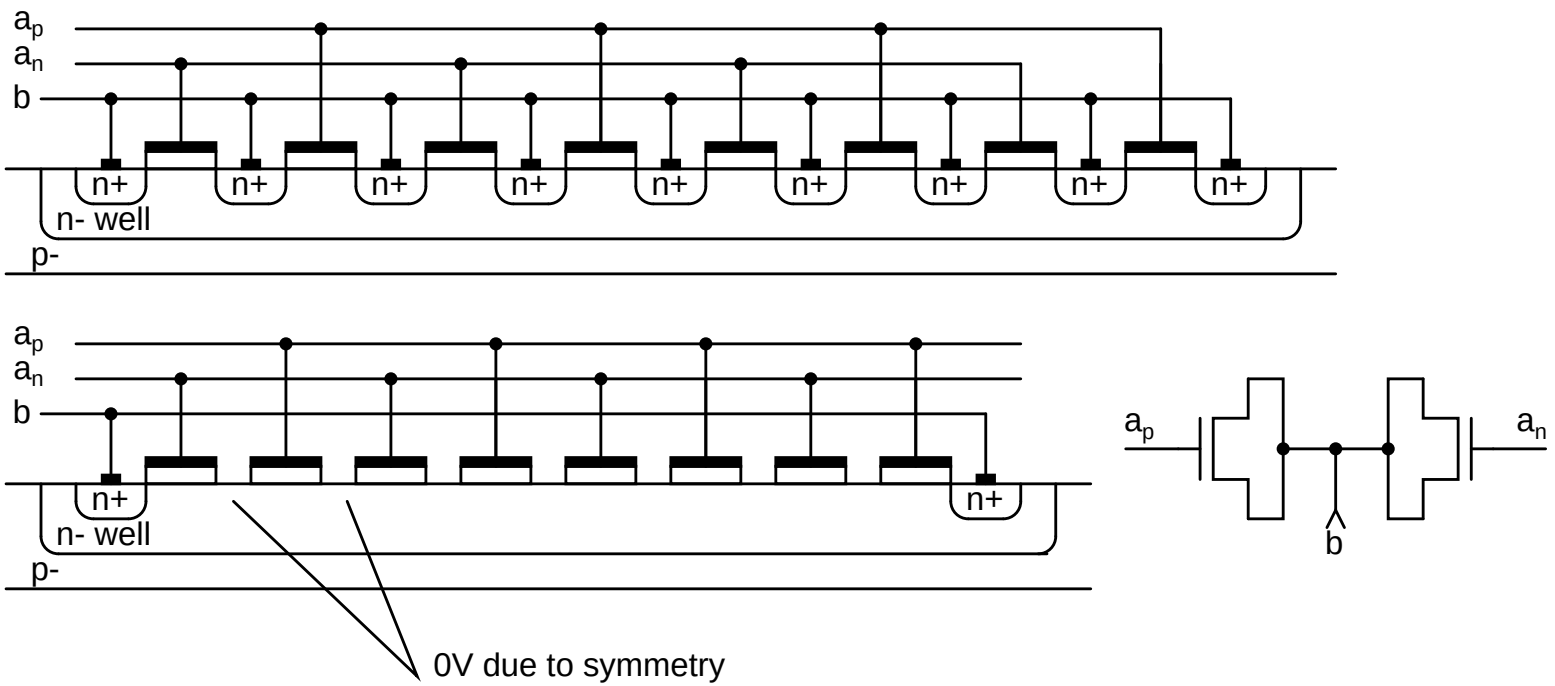
- Tunable using a varactor
- Reverse biased p-n junction
- MOS device in accumulation—larger tuning range; more popular in CMOS ICs

Accumulation MOS varactor



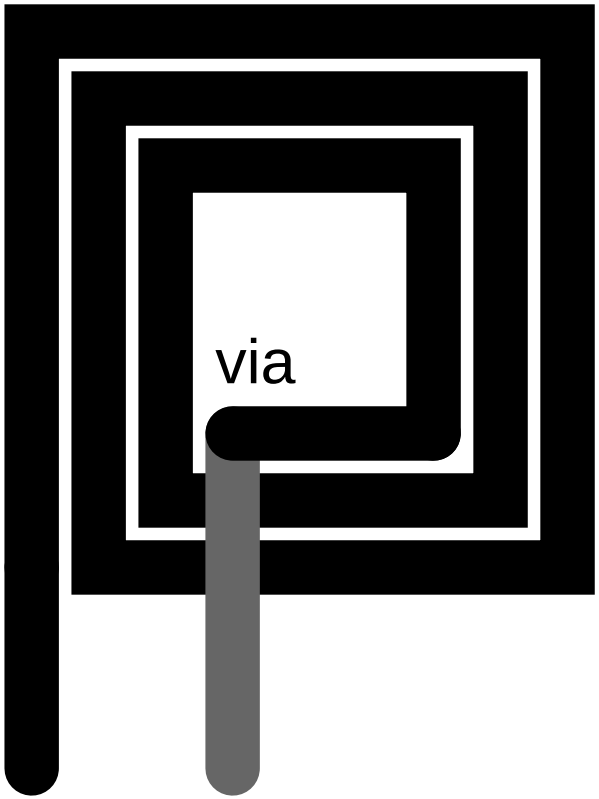
- nMOS in n-well
- Multi fingered structure to reduce gate, “channel” resistance
- $W \sim$ few microns
- $L > L_{min}$ to reduce parasitics
- Gate can be contacted at both ends to further reduce resistance

MOS varactor with differential excitation



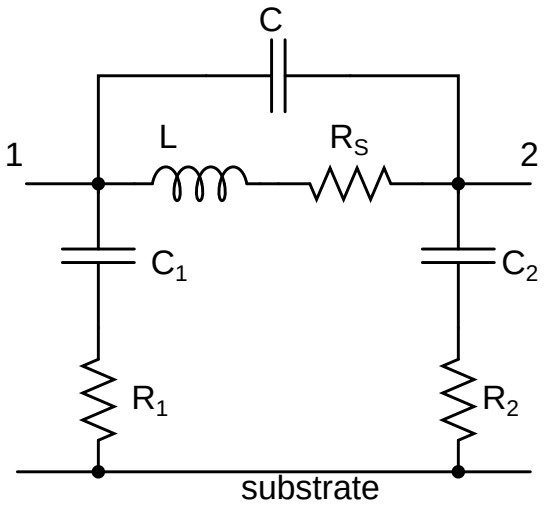
- Interdigitated fingers—alternate ones connected to a_p and a_n
- Region between gates connected to a_p and a_n at 0 V due to symmetry
- All n+ contacts except the ones at the end can be removed [5]
- Smaller structure, lower series resistance, and smaller parasitic capacitances

On chip inductors

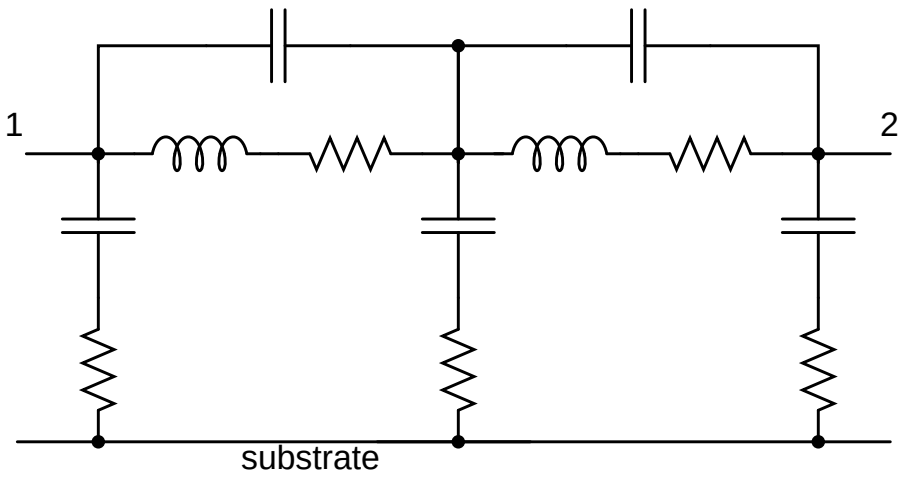


- Planar inductor on one of the metal layers
- Top level metal preferred
  - Farther from the substrate
  - Smaller parasitic capacitance
  - Lesser coupling to substrate, and hence, loss
- Thicker top level metal ($\sim 2\,\mu$m) available in mixed signal processes

Inductor loss mechanisms

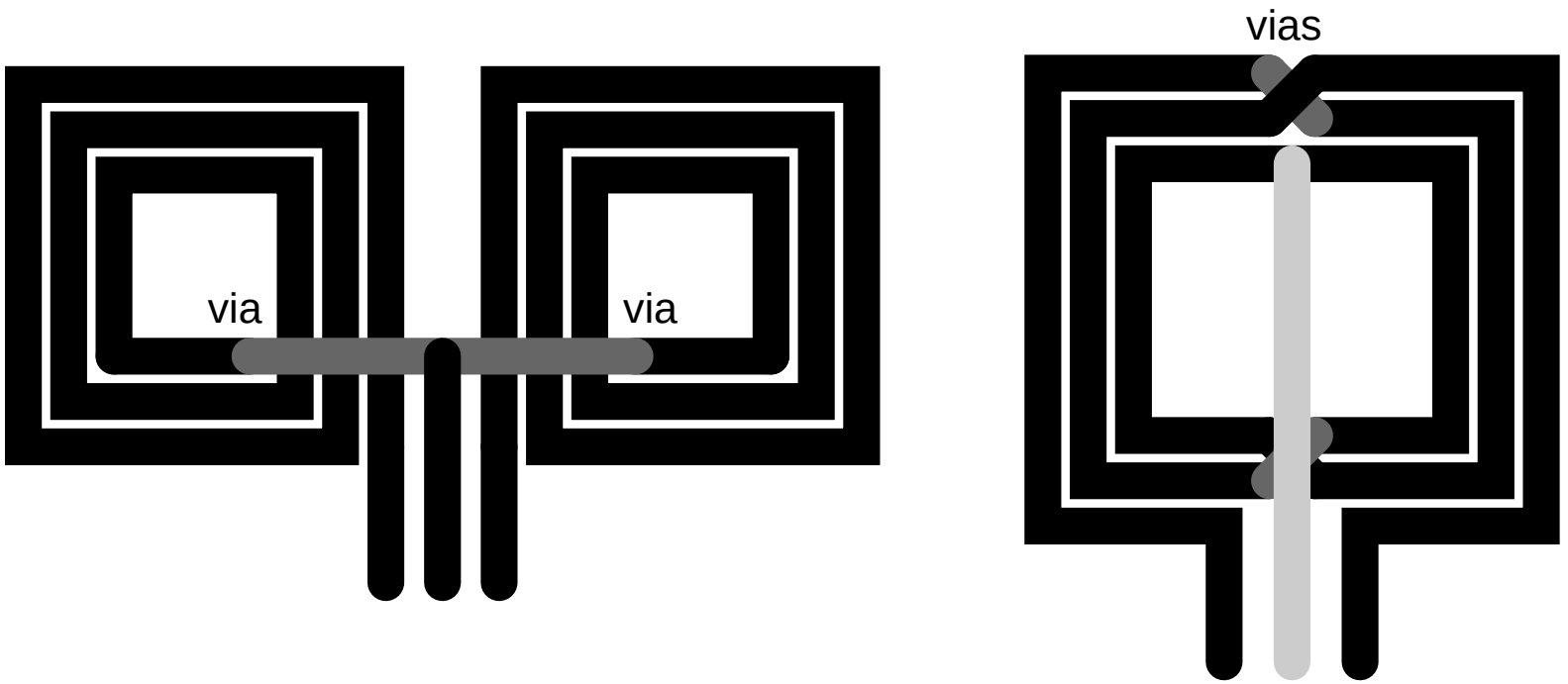


distributed model: more sections can be added



- Winding resistance
  - $R_\square L/W$
  - Effective $R_\square$ larger due to skin effect
  - Copper: $2\,\mu$m skin depth ($\propto 1/\sqrt{f}$) at 1 ghz
- Capacitive coupling to substrate and its resistance
- Inductive coupling to (resistive) substrate
- Quality factors upto 15 possible, typically 8-10
- Use adequate thickness and number of vias during layout

Differential inductor



- Symmetrical differential inductor
  - More compact for a given differential inductance
  - Larger potential difference between turns $\Rightarrow$ larger effect of interwinding parasitics
- Symmetrically laid out single ended inductors
  - Greater area
  - Interwinding parasitic capacitance not very signifi cant

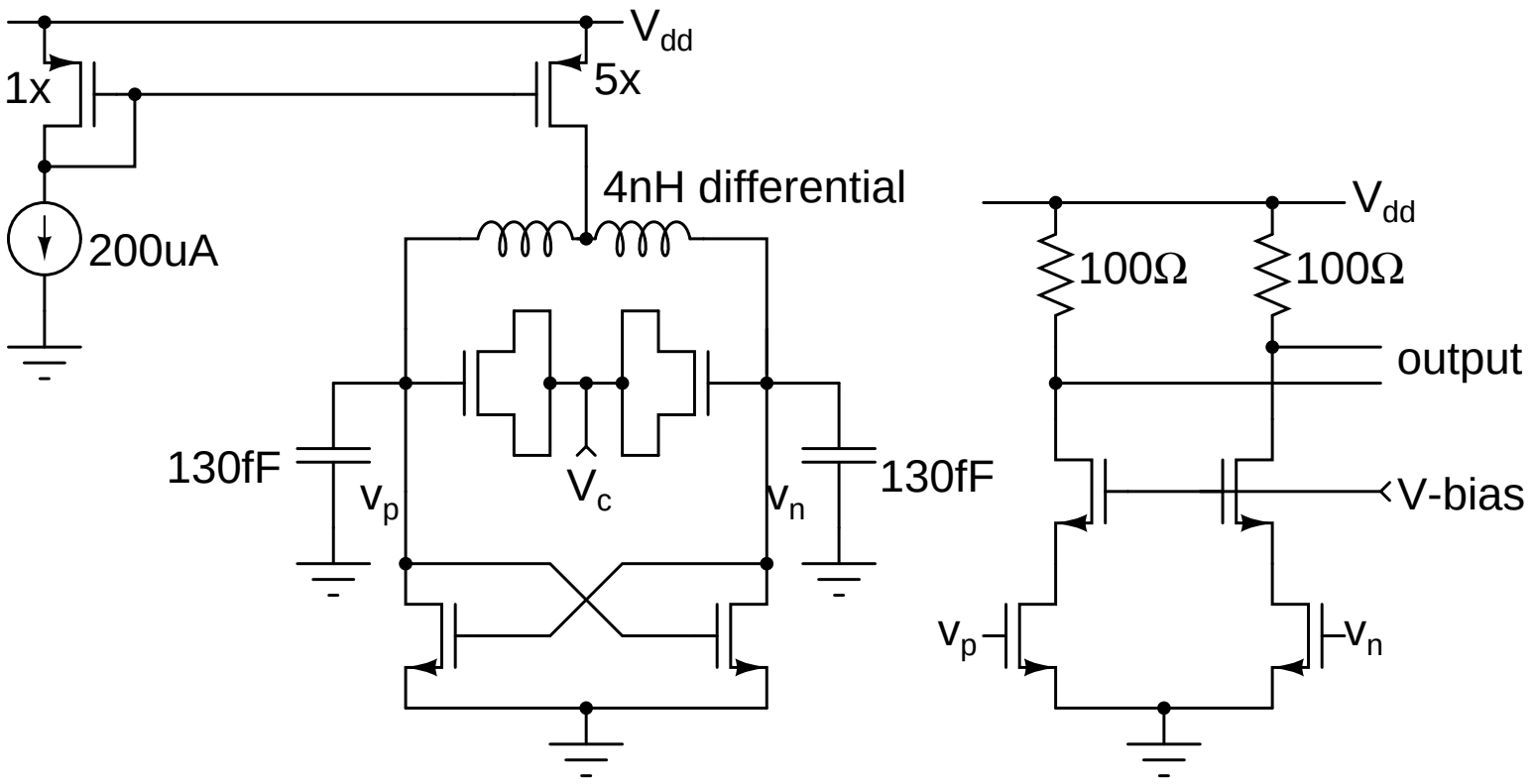
Inductor simulation

- Some processes have scalable inductor library and models
- Typically needs to be simulated from process parameters—metal thickness, resistivity, intermetal spacing etc.
- Inductance value
  - FastHenry, Asitic etc.
  - Accurate estimation possible
- Quality factor
  - FastHenry, Asitic etc.
  - Harder to accurately estimate losses due to substrate coupling
- Parasitic capacitance
  - First order parallel plate estimation—OK for single ended inductors
  - FastCap etc.
  - Use distributed models for accuracy

VCO design: bias current and transistor sizing

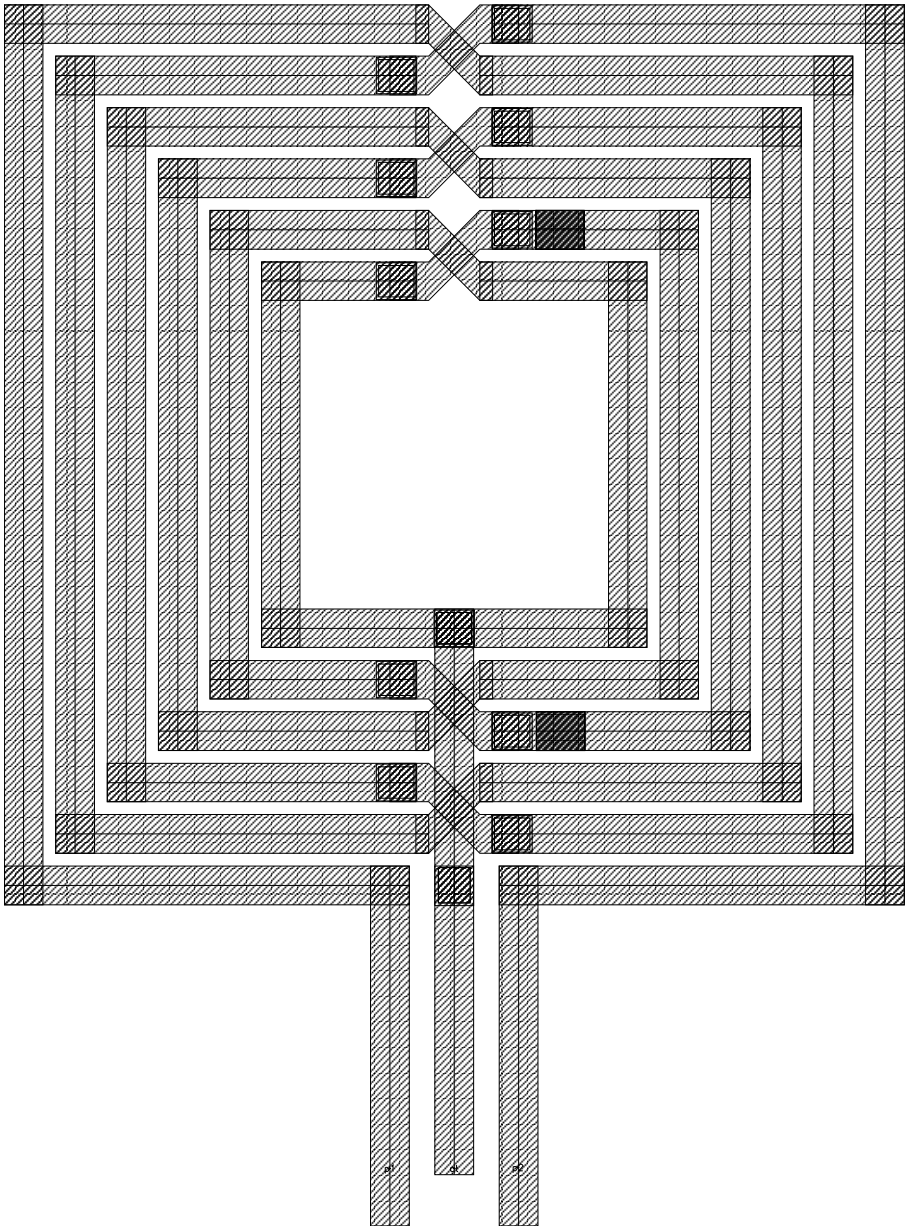
- Bias current is a function of tank losses and desired amplitude
  - Maximize the inductance for a large amplitude from a small current
- Transistors typically minimum length at high frequencies—longer to lower $1/f$ corner
- Bias source: longer than minimum length to lower $1/f$ noise
- Minimize all parasitics to maximize tuning range from the varactor
- Transistor W/L to get the desired g_m for startup in the worst case
  - Large $g_m \Rightarrow$ increased phase noise; So don't go crazy!

5 GHz VCO in 0.18 μm CMOS

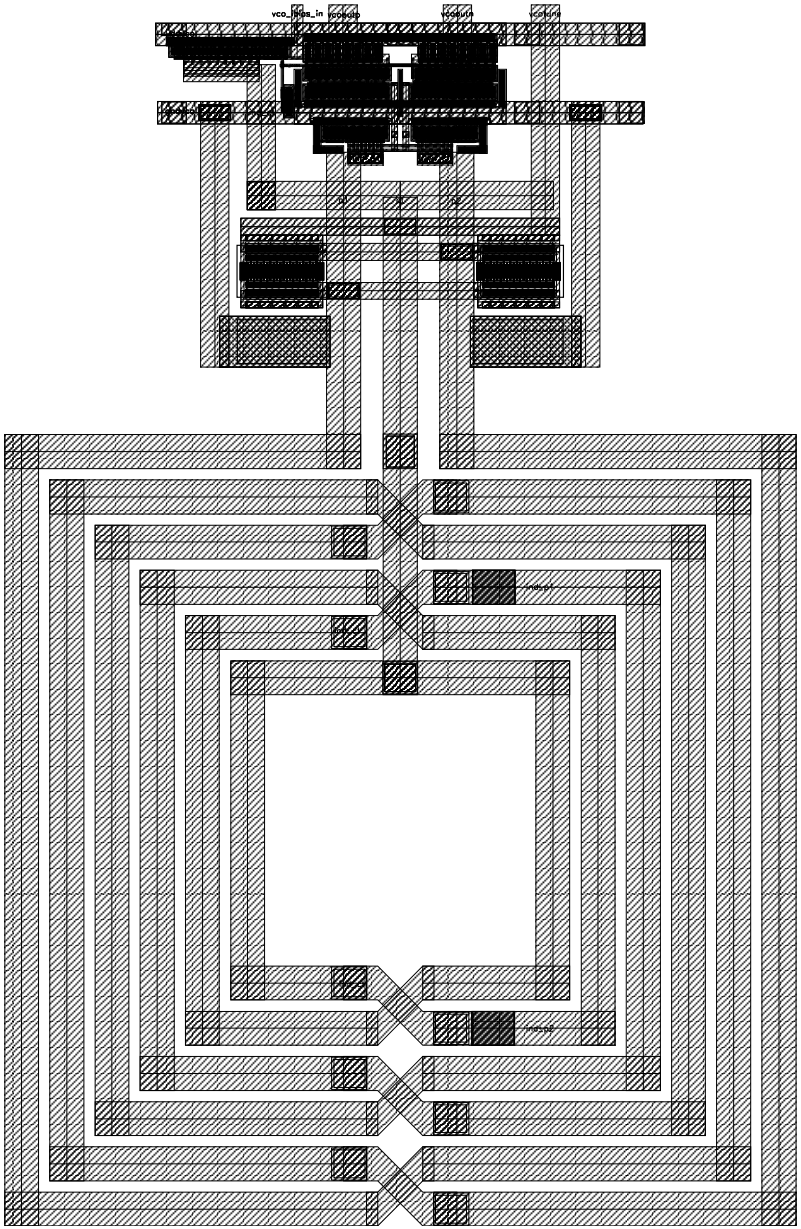


- $L = 4$ nH and $C = 0.25$ pF (differential) chosen
- 6 turn inductor on top metal layer, $\approx 140\,\mu$m square
- From inductor simulations, $Q \approx 6$
- Minimum length transistors

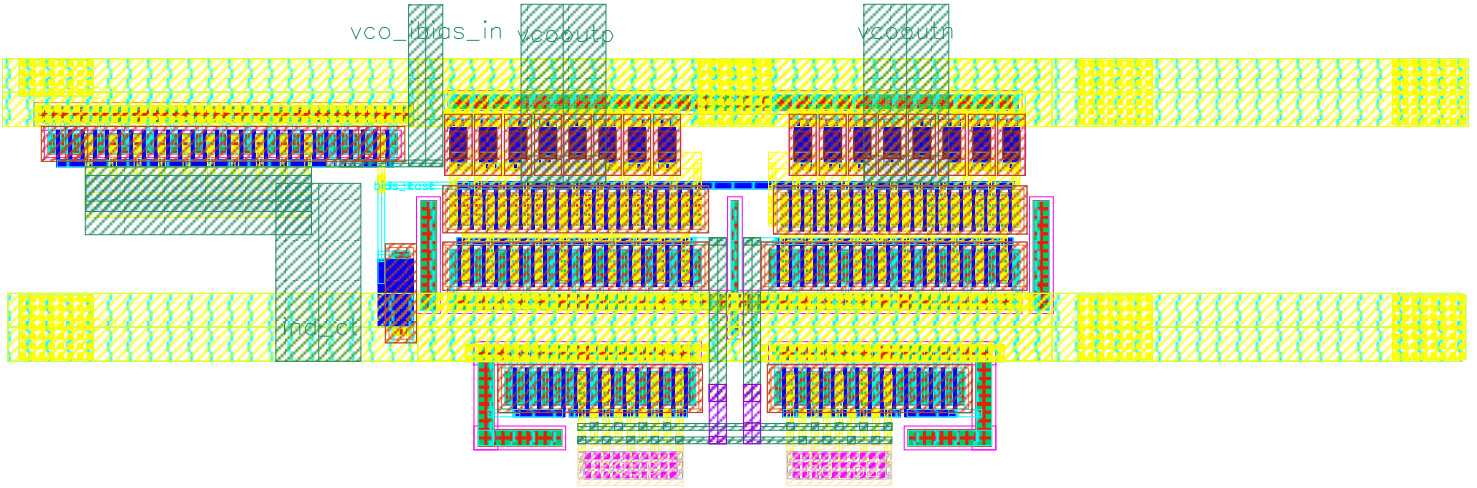
5GHz VCO-inductor



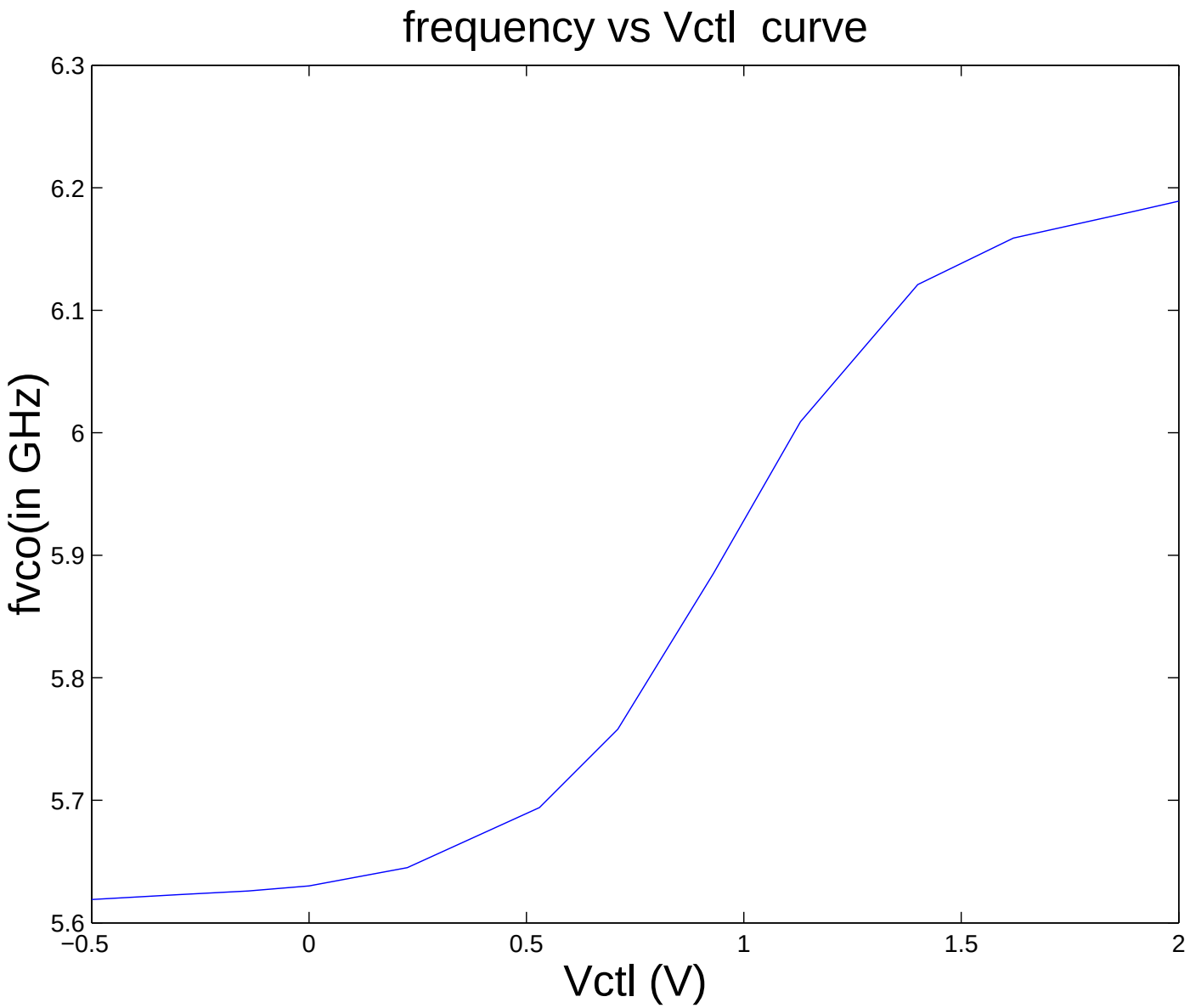
5GHz VCO layout



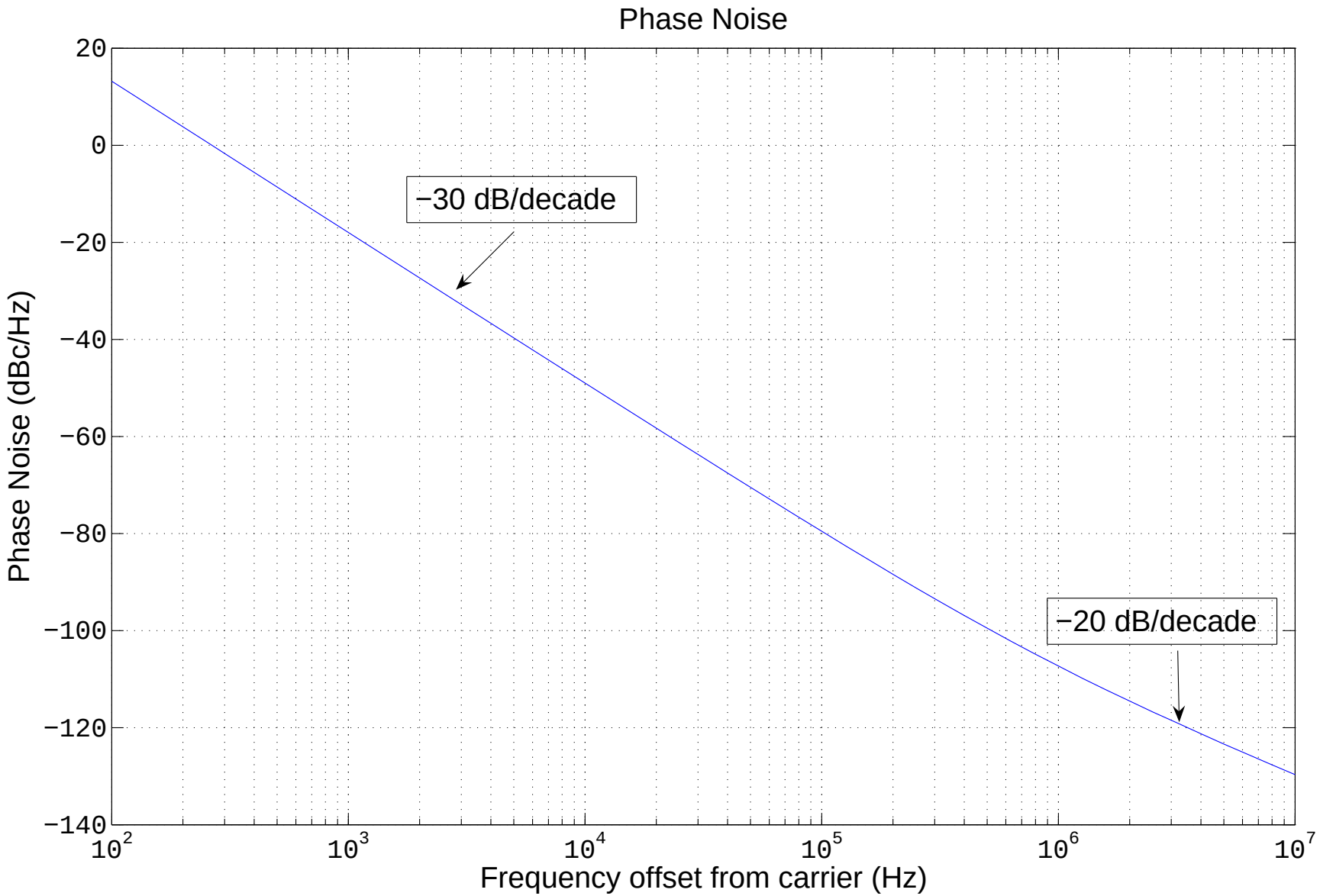
5GHz VCO layout



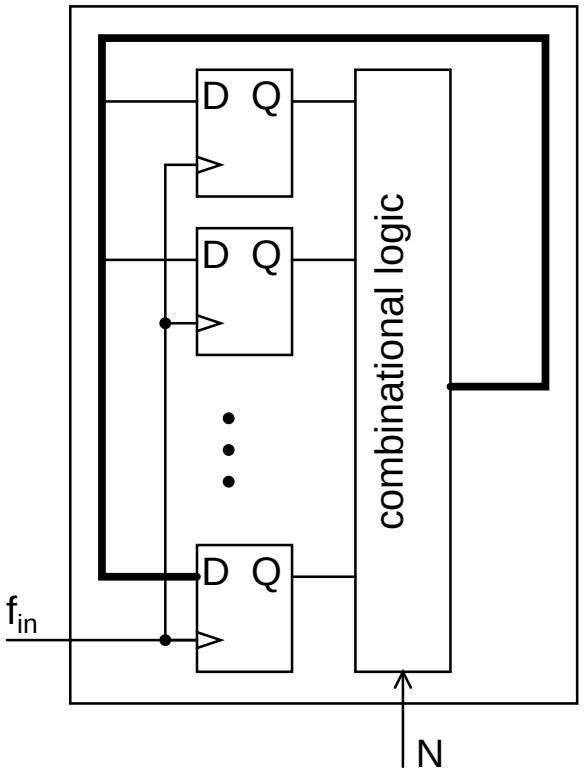
VCO (higher freq. version)-measured f vs. V



VCO-simulated phase noise

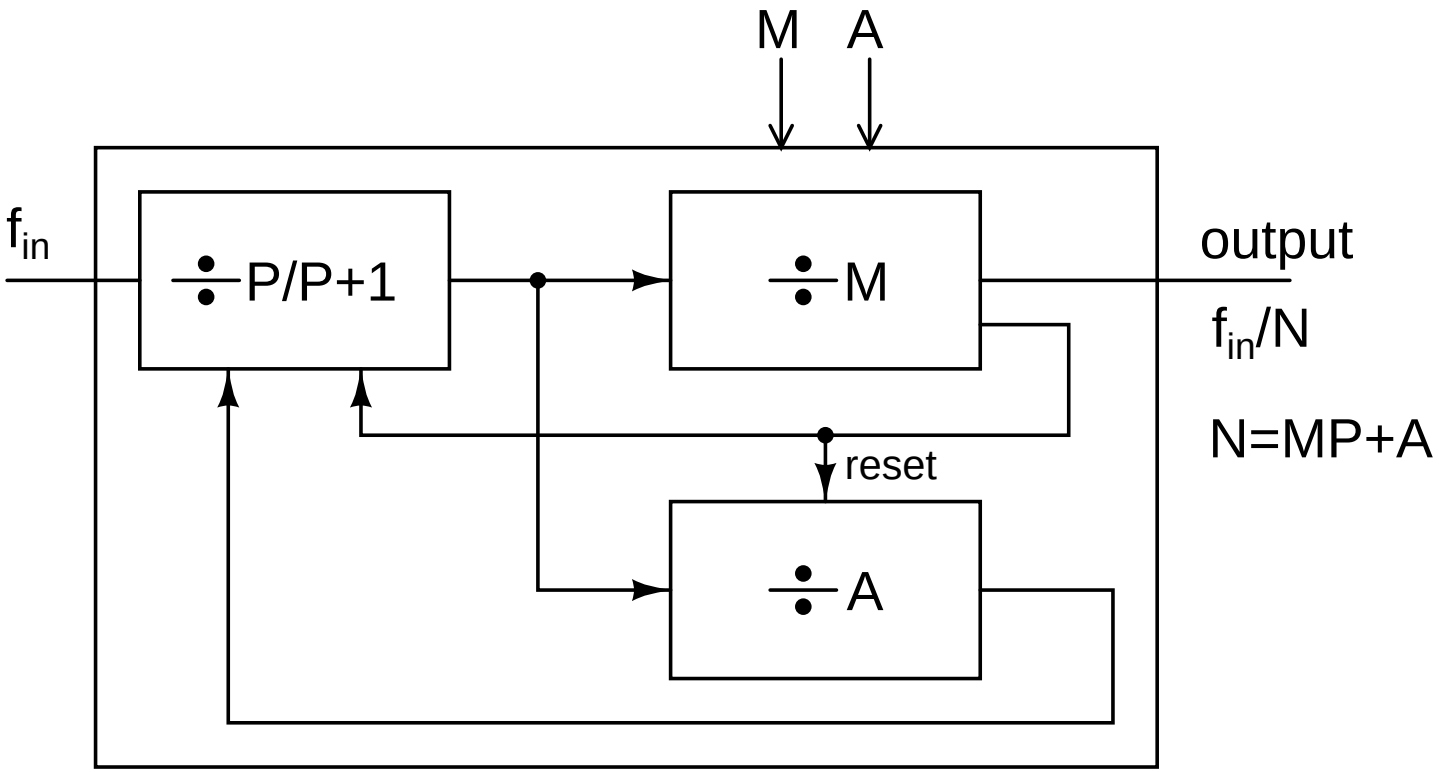


Programmable divider-Synchronous counter



- All of the circuitry running at full speed
- Very high power dissipation
- Asynchronous operation preferred

Programmable divider-Pulse swallow architecture



- Dual modulus prescaler $\div P/P+1$
- Divide by $P+1$ for A cycles
- Divide by P for $M-A$ cycles
- Full cycle = $(P+1)A + P(M-A) = MP + A$
- Only the dual modulus prescaler running at full speed
- Programmability using M and A

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