Titles and abstracts of the lectures to be delivered during the visit

Cognitive Radio and CMOS RF Circuit Challenges and Ideas (1.5 hours)

To better exploit the scarce available radio spectrum, “cognitive radio” devices could monitor the locally available spectrum to detect unused spectrum. Starting with the TV bands, regulators are in the process of allowing such devices to conditionally use “spectrum holes” or "white spaces". In the future similar functionality may be allowed in other bands. This tutorial discusses circuit and system challenges related to cognitive radio, focusing mainly on the analog and mixed-signal radio front-end part. Cognitive radio asks for new functionality, like spectrum sensing and an agile radio transmitter and receiver, posing several circuit and system challenges. Moreover, requirements on radio receiver and transmitter blocks are also quite challenging in terms of for instance flexibility, linearity and spurious emissions.

A cognitive radio ideally adapts itself in a smart way to its radio environment. CMOS IC-technology is the mainstream technology to implement smart signal processing and for reasons of cost and size it is attractive to also integrate the radio frequency (RF) hardware in CMOS. Traditional radio transceiver hardware is highly dedicated, e.g. to a fixed RF band, channel bandwidth and modulation format. In contrast, a cognitive radio asks for a programmable radio, a kind of "software defined radio" (SDR). This lecture reviews recent research aiming at a CMOS SDR, focusing on the challenging RF and analog baseband part of a SDR receiver and transmitter. Traditional radio receiver and transmitter hardware is highly dedicated, e.g. to a fixed RF band, channel bandwidth and modulation format. The challenge is to conceive receiver architectures and circuits that can flexibly support a range of RF-bands, channel-bandwidths, and modulation types at different sensitivity levels. Several resulting challenges and solutions proposed in recent literature will be addressed.

Wideband Receivers exploiting Thermal Noise Cancelling – history and development (1.5 hours)

Wide-band Low Noise Amplifiers suffer from a fundamental trade-off between noise figure NF and source impedance matching, which limits NF to values typically above 3dB. Noise cancelling is a feed-forward circuit technique which can break this trade-off. In this presentation the discovery and development of the noise cancelling technique is discussed. The principle was discovered, when looking for wideband impedance matching circuit topologies. A methodology which systematically generates all the possible topologies with 2 transconductor in the signal path is presented. Next to well-known circuits (e.g. the Common Gate-stage and shunt series-feedback Common Source-stage), two novel topologies have been found, amongst which a noise cancelling circuit.

This presentation will also reviews the noise cancelling principle and its key properties. Furthermore several circuit implementation variants will be discussed, amongst which a Balun-circuit and a Balun-LNA-Mixer.

Advances in Low Jitter CMOS Clock Generation stimulated by Figure-of-Merit Definitions (1.5 hours)

The timing jitter and phase noise of clock generation circuits can usually be improved by admittance scaling at the cost of power consumption. To benchmarks circuits and improve their jitter in a power efficient way, it makes sense to define a Figure of Merit (FoM) that normalizes for this admittance level scaling effect. We will discuss some recent ideas to advance the state-of-the-art in low jitter CMOS circuits, stimulated by the definition of such FoMs, more specifically:

1) A multi-phase clock generator, which can be implemented by a delay locked loop or a shift register. Using a jitter-power FoM, it can be shown that a shift register has fundamental advantages and can achieve a lower jitter for a given power budget.

2) A new relaxation oscillator topology which exploits a noise filtering technique, implemented with a switched-capacitor circuit. Its frequency tuning range is 1-12MHz and its phase noise is £(100kHz)=-109dBc/Hz at fosc=12MHz, while consuming 90μW. A FoM of -161dBc/Hz is achieved, which is only 4dB from the theoretical limit and a 6dB improvement over the best published relaxation oscillator.

3) A new PLL exploiting a phase detector which uses sub-sampling of the VCO output by the reference clock to realize very low phase-noise within the PLL-loop bandwidth. A 2.2GHz CMOS PLL using a 55MHz crystal achieves an rms output jitter of 0.15-ps (10kHz ~ 40MHz) with 7.6mW power consumption, resulting in a power-jitter FoM of -248dB. To our knowledge the best power-jitter FoM achived in prior arts is -238dB.

CMOS Frequency Translation Circuits (1.5 hours)

Radio Frequency (RF) Transceivers make extensive use of frequency translation or frequency conversion, e.g. to convert baseband signals to RF or the other way around. Frequency translation can be implemented in various ways, e.g. via nonlinearity but also via linear but time-variant circuits.

This presentation reviews principles and performance limitations of frequency converters suitable for CMOS implementation. Most circuits rely on CMOS switches, which still improve when scaling CMOS down in the nanometer regime. Fundamental differences between various techniques are highlighted by means of a classification and comparison of mixing and sampling. Especially in receivers for software defined radio, robustness for strong interferers is crucial. To this end, various recently proposed techniques will be reviewed which improve out-of-band linearity and realize Harmonic rejection robust to mismatch.