VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 5

This problem set will cover the design of a continuous-time $\Delta\Sigma$ ADC designed as a part of an FM receiver. The signal bandwidth is 200 kHz, and an inband peak SNR of 90 dB is desired. For some design margin, the in-band SQNR should be atleast 12 dB better than the desired SNR. A single-bit quantizer has to be used, and the sampling rate is 64 MHz (which cannot be changed). The supply voltage is 1.8 V, and the peak input signal swing that needs to be supported is 3 V (peak-to-peak differential). Use an NRZ pulse shape for the DAC.

1. Determine the order - show your reasoning clearly (with plots, if necessary).
2. Determine the coefficients of the NTF, and plot the NTF magnitude response in a dB scale. What is the MSA ?
3. What is the maximum RMS clock jitter (assumed white) you can tolerate, so that the peak SNR degradation due to clock jitter is 94 dB ? Show calculations. How will you verify this using simulation ?
4. Assume that the quantizer path has a delay of 4 ns. Determine the transfer function of the continuous-time loop filter required to achieve the desired NTF, and compare the NTF you obtain with what you wanted to achieve. Do not skip steps.
5. Implement the loop filter using ideal integrators, resistors and capacitors. Use an ideal quantizer. **If your roll number is even, use a CIFF loop filter - otherwise use a CIFB loop filter.** Scale the integrator outputs so that they never go beyond 1.5 V (peak-to-peak differential). Run and show simulation results on the scaled modulator to demonstrate that this is indeed achieved in your design. The inband thermal noise added by the input resistors of the first integrator should limit the inband SNR of the ADC to 94 dB. Limit the opamp outputs to the supply voltage - otherwise your modulators will oscillate.
6. Run time domain simulations with a 40 kHz input tone with an amplitude of 0.9 MSA. Plot the PSD of the ADC output, where the PSD is computed with a 1024 point Hann window. Determine the in-band SQNR and compare with your calculations.
7. Repeat step 5 above with real integrators with finite gain of 40 dB, a unity gain bandwidth of 250 MHz. Assume infinite slew rate. Do not change the RC values from the ideal design. What is the new NTF ? Compare it with the ideal.
8. Repeat step 6 with the nonideal integrators.
9. Verify the anti-aliasing property by using a 1 V(peak-to-peak, differential) tone at (f_s + 40 kHz) for the input. What do you see in the signal band ? How does it compare to calculations ?