EE658: VLSI Data Conversion Circuits; HW6

Nagendra Krishnapura (nagendra@iitm.ac.in), Shanthi Pavan (shanthi@ee.iitm.ac.in)

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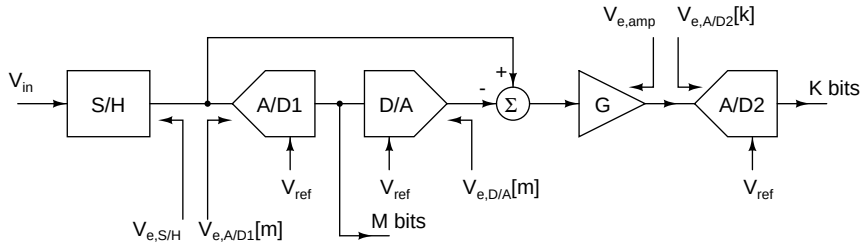

Figure 1:

1. Fig. 1 shows a two step flash converter with error correction. The overall resolution is $N = M + K - 1$ bits. The error in each block is shown as an analog voltage referred to either the input or the output. i.e. The m^{th} transition of A/D1 occurs at $mV_{LSB1} + V_{e,A/D1}[m]$ and the m^{th} output of D/A is $mV_{LSB1} + V_{e,D/A}[m]$. $0 \leq m \leq 2^M - 1$ and $0 \leq k \leq 2^K - 1$. $V_{LSB} = V_{ref}/2^N$ is the LSB voltage of the overall converter.

   (a) Derive the value of the input V_{in} which corresponds to m^{th} transition of A/D1. You should get an expression that combines the errors from different components.

   (b) Derive the value of the input V_{in} which corresponds to k^{th} transition of A/D2. Assume that A/D1 is between m^{th} and $(m+1)^{\text{th}}$ transitions.

   (c) In the result from (a) above, assume that the different terms contribute equally to the total error, which is constrained to $0.5V_{LSB}$. Calculate the individual errors in terms of V_{ref}.

   (d) Calculate the allowable errors in each component for a 8 bit converter, for $M = 5, K = 4$ and $M = 4, K = 5$. Express the accuracy as an effective number of bits (A component with a voltage range V_{ref} has an L bit accuracy if its error magnitude is less than $V_{ref}/2^{L+1}$, i.e. half LSB at L bits).

2. Assume that you have a 2 step flash A/D converter (no digital error correction) with 2 bits in each stage. All components other than the residue amplifier are ideal. Plot INL and DNL for the following cases. Compare it with the ideal characteristics.

   (a) (2 pts.) The amplifier has a gain $G > 4$

   (b) (2 pts.) The amplifier has a gain $G < 4$

   (c) (2 pts.) The amplifier has an input referred offset $V_{os} > 0$

   (d) (2 pts.) The amplifier has an input referred offset $V_{os} < 0$