EE658: VLSI Data Conversion Circuits; HW4

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0.18 μm technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300$ μA/V^2; $K_p = 75$ μA/V^2; $A_{VT} = 3.5\,mV$ μm; $A_\beta = 1\%$ μm; $V_{dd} = 1.8$ V; $L_{min} = 0.18$ μm, $W_{min} = 0.24$ μm; Ignore body effect unless mentioned otherwise.
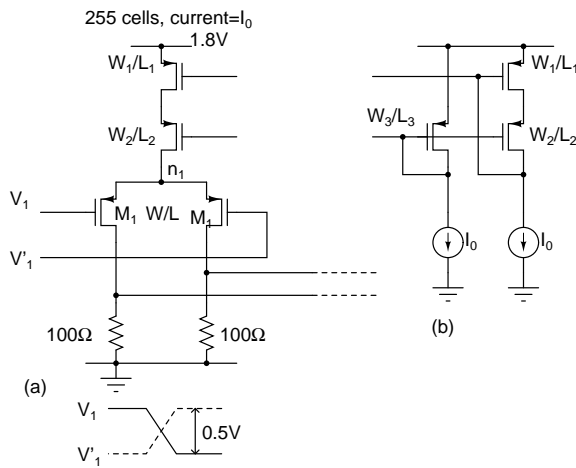

Figure 1:

1. A 8 bit DAC is built using the current steering cells shown in Fig. 1.

   The full scale(differential) output voltage of the DAC needs to be 1.02 V. Calculate the lower limit on the switch voltages V_{bi}, V'_{bi}.

   The switching voltage $V_{bi} - V'_{bi}$ has a peak to peak value of 1 V. Calculate W and L for M_1 and M_2 for complete switching at 0.5 Vpp (to provide for some margin).

   Calculate the minimum and maximum voltages on the tail node n_1.

   Assume that a headroom of 0.8 V is available for the current source. Use 0.2 V for the cascode. Calculate

the dimensions of the current source and the cascode such that the standard deviation in DNL is 0.01 LSB.

Design an appropriate bias circuit as shown in Fig. 1(b)

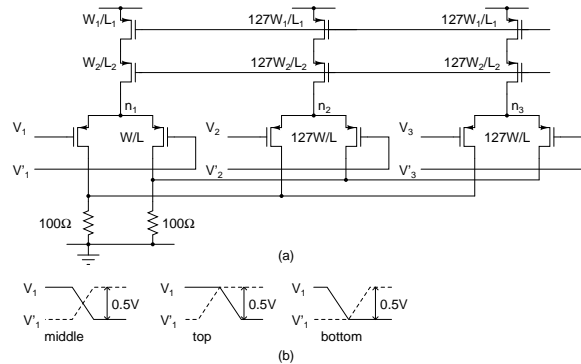In your submission, report all device sizes and key operating points.

Figure 2:

2. Simulate the circuit designed in the previous problem with a power supply of 1.8 V. Use the values of swiching voltages V_i, V'_i calculated earlier. Simulate the configuration shown in Fig. 2(a)[1]

   Simulate the differential DAC output waveform when V_1, V'_1 change from one state to another. V_2, V'_2 and V_3, V'_3 are held constant. Do this for two cases: (a) $V_2 - V'_2$ and $V_3 - V'_3$ are both high, (b) $V_2 - V'_2$ is high and $V_3 - V'_3$ is low. Ideally the output waveforms in the two cases should be identical except for a level shift. Overlap the waveforms with

[1] In Fig. 2(a), the DAC is divided as a parallel combination of a unit cell and two cells that are 127 times the unit cell. Setting up 255 unit cells and simulating them with thermometer coded inputs takes a long time. Combining the cells as shown reduces the time required to setup and run the simulations

an appropriate level shift and compare the two. Plot the waveform on the tail node.

Redo the above simulations when the waveforms cross at the top and the bottom (Fig. 2(b)).

In your submission, report the waveforms in the above cases and your inferences.

3. `Dout.dat` contains the digital output of a Delta Sigma A/D converter with a 4 bit quantizer and an OSR of 64. `Idac.dat` contains the current source values of a 4 bit DAC. The DAC is driven by the digital sequence. Overlay the spectral densities (with a 2048 point FFT) of the digital sequence, the output when the current sources are used as a conventional DAC, and when the current sources are used as a DAC with data weighted averaging. Comment on the results.
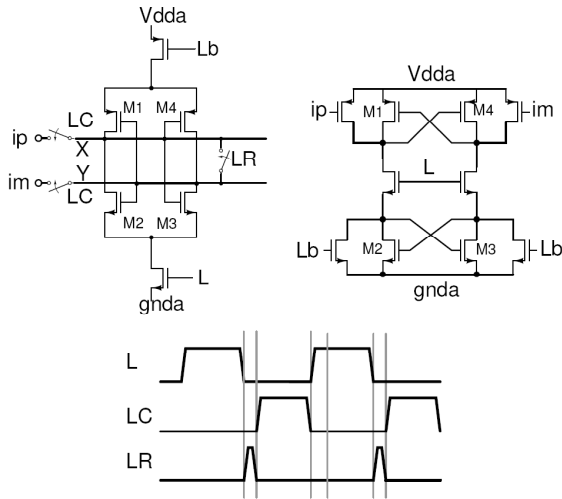

Figure 3: Latches for dynamic offset simulations

4. In this problem, we attempt to understand the issue of dynamic offset. Consider the two latch circuits in Fig. 3. The first latch was discussed in class. Another candidate latch (with the advantage of greatly simplified clocking) is shown towards the right of the figure. In both latches, L is the latch signal, while Lb is its complement. For simplicity, use an ideal clock generator. $V_{dd} = 1.8$ V. The input is fully differential, with a common-mode voltage of 0.9 V. The clock frequency is 10 MHz.

(a) Use minimum sizes for all transistors. Choose appropriate implementations for the switches. Determine dynamic offset using the following procedure - the differential input is to be made a slow ramp, increasing at 2 mV every clock period, starting from $-V_{dd}/5$ and going all the way to $V_{dd}/5$. We hope that the offset will lie within this range. The "threshold" of the latch (ideally to be zero) can be found to within 2 mV by observing when the regenerated output flips sign. Take care of the following during simulation - choose the time step of the simulation to be sufciently small so that the waveforms during regeneration do not change appreciably. Which of the latches has more dynamic offset? Why? In your report, draw the circuit diagrams with all device sizes marked. Also on one graph, plot the waveforms of all latch nodes in that clock period where the latch flips sign.

(b) Deliberately add a capacitance of 0.5 fF at the drain of M1 only, and repeat part (a). What do you notice? Why?
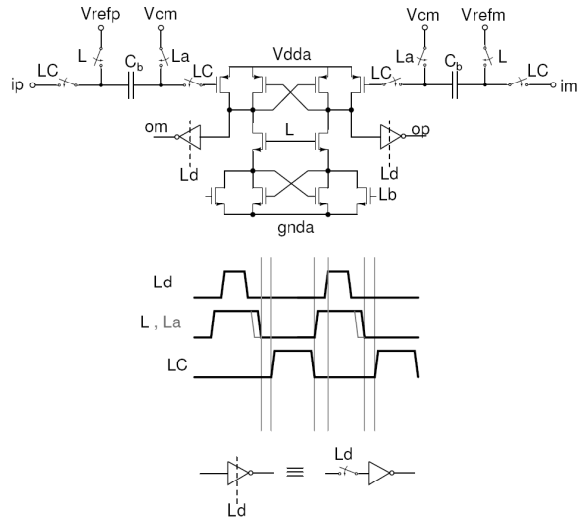

Figure 4: Latch for flash A/D

5. This problem discusses another way of subtracting differential references from the differential input. This is done by the use of coupling capacitors Cb as shown in Fig. 4

(a) Explain clearly how this circuit works.

(b) What is the capacitance looking in from the input when LC is high?

(c) How will you choose Cb ?

(d) Using this as the basic building block, design a 4 bit flash ADC. $V_{dd} = 1.8$ V. The full scale input is to be 3 V (peak to-peak differential), with a common-mode voltage of 0.9 V. Assume you have ideal voltage sources of 1.65 V and 0.15 V from which to operate the ladder. How will you choose the value of the ladder resistors ? Design the digital back-end (transition detect and the 1-of-N to binary converter).

(e) Show the spectrum of the ADC output for a full-scale sinewave at about fs/2. What is the SQNR (in dB) ? One way of doing this is to print the four ADC output bits into a file, read the file into MATLAB, convert from binary to decimal, and do the FFT in MATLAB. Another way of doing this is to use an ideal 4-bit DAC at the output of the ADC and run an FFT on the DAC output in Eldo.

ADC. The circuit diagram of the preamp is shown in the lower part of the figure.

(a) Design an appropriate circuit to generate the bias voltage bp.

(b) What does the input common-mode voltage of the preamp settle to ?

(c) In series with the input terminals of the preamp, insert a 10 mV voltage source as shown in the figure. Simulate the auto-zero action of the preamp-assume that the differential reference is 100 mV, with a common-mode voltage of 900 mV. Show, on the same picture, the waveforms at the input of the preamp during the auto-zero phase.
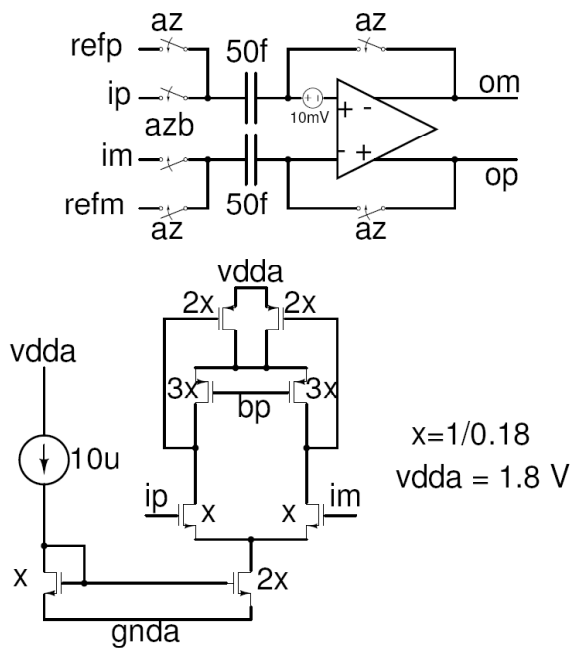

Figure 5: Preamp, autozeroing

6. Fig. 5 shows a preamplifier to be used in a flash