EE658: VLSI Data Conversion Circuits; HW3

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1. Assume that an N bit ideal quantizer with $LSB = 1$ is driven by a full scale sine wave (2^N pp) with a period of M samples, $M \gg 2^N$. If the histogram of the output is plotted what is the number of samples at each output level?

   What happens if the quantizer has DNL? Will you be able to determine the DNL from the histogram of the output samples? Assume that the full scale is exactly the same as before?

2. The output code density of an A/D converter to a low frequency full scale sine wave is given in `a2dcodes.dat`. How many bits does the A/D converter have? Analyze the code density to obtain its INL and DNL. Simulate this A/D converter with a full scale sinewave near half the sampling rate. Compute the SNDR. What is the ENOB of this converter? What is the maximum jitter that can be tolerated so that the SNR due to jitter is 3dB more than the SNDR computed above?

3. An N bit thermometer DAC has unit current sources of value I_0 with a relative error $\delta I_0/I_0$ whose standard deviation is σI_0. A large number of such DACs are manufactured, and DNL and INL are measured versus the input code. What is the standard deviation (over the sample space of DACs) of DNL and INL for each input code? What is the maximum INL standard deviation and for which code does this occur? Assume end point fitting. Use $\delta I_0/I_0 \ll 1$ for suitably approximating your expressions.

4. Come up a macromodel for a fully differential opamp that incorporates the following:

   - The linear small signal transfer function should be $A_0/(1 + sA_0/\omega_u)(1 + s/p_2)$. A_0 is the dc gain, ω_u is the unity gain frequency, and p_2 is the nondominant pole
   - The input resistance in ∞; The input capacitance is C_{in}; The output resistance is zero.
   - The differential output voltage should be limited to be within $\pm V_{max}$
   - The common mode output voltage should be V_{ocm}
   - The output slew rate should be limited to SR

   You can use any components you want. For limiting functions, you can use limits on controlled sources, if your simulator supports it, or use diode limiters like in Fig. 1. In the submission, you need to show the schematic with component values in terms of the parameters above, and specific values for $\omega_u = 2\pi \times 100\,\text{Mrad/s}$, $p_2 = 2\pi \times 200\,\text{Mrad/s}$, $A_0 = 60\,\text{dB}$, $C_{in} = 100\,\text{fF}$, $V_{ocm} = 0.9\,\text{V}$, $V_{max} = 1.5\,\text{V}$, $SR = 20\,\text{MV/s}$.

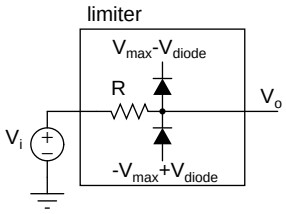

Figure 1: Diode limiter