Project: 5 Gb/s Serial Link

Due Date: Dec. 4, 2016

Design a serial link operating at 5 Gb/s and compensating 15 dB channel loss at Nyquist frequency with minimum power consumption. The link includes a 5 Gb/s transmitter and clock and data recovery circuit to recover the bits error-free at the output of the channel. All the blocks should be designed at schematic level in 45nm CMOS process at 1V supply voltage. The design should make use of following blocks.

1. Ideal 2.5 GHz clock source on the transmitter side.
2. 2:1 serializer on the transmitter side.
3. 7-bit PRBS data for testing.
4. Channel model from Assignment #3.
5. Verification of the recovered bit-pattern in Matlab.

Report Guidelines

1. The report should justify all the design choices made.
2. Use schematic diagram and simulation results to describe block-level operation.
3. Final results should include transmit and received eye-diagrams with and without equalization, transient settling of recovered clock frequency, and recovered clock jitter.
4. Power consumption of each block should be reported and its fraction of the total power with a pie-chart.
5. Include the reference sources used for the design in the report.