EE6322: VLSI Broadband Communication Circuits

Assignment 2

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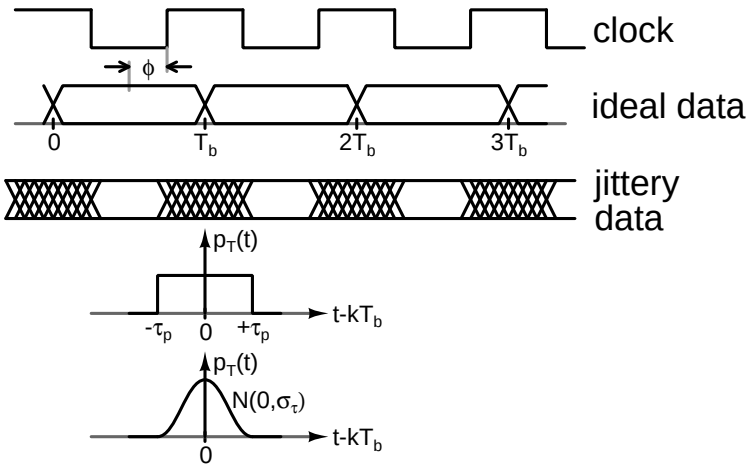

Figure 1: Problem 1

1. A full-rate binary phase detector receives data and clock with an offset of ϕ as shown in Fig. 1. Plot the output (average of $UP-DN$) versus ϕ (the phase by which the rising edge of the clock lags the middle of the data period) for (a) ideal data, and (b) jittery data in which the data transitions move from the ideal bit boundaries (for the two jitter cases shown). The probability density function of the deviation of the data transition points from the ideal transition points are shown. One is a uniformly distributed jitter within $\pm\tau_p$ and the second is a Gaussian distributed jitter with zero mean and standard deviation of σ_τ. In both cases, express the maximum incremental gain of the phase detector in terms of the standard deviation of the data jitter.

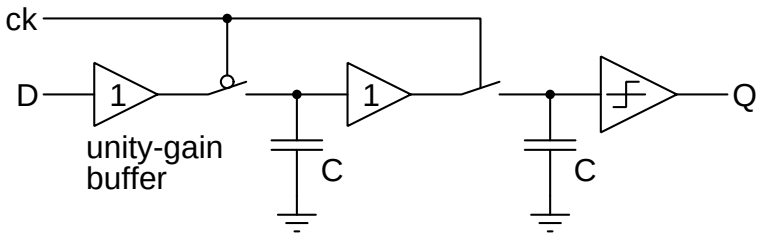

Figure 2: Problem 2

2. Construct the model of a D-flip-flop as shown in Fig. 2. It is a cascade of buffered track-and-hold stages followed

by a comparator. You can use this for macromodeling flip-flops in CDRs and PLLs. Invert the switch controls to trigger on the opposite edge. Add the inverted output $\overline{Q}$ if desired.

Using this D-flip-flop, construct a full-rate linear (Hogge) and a binary (Alexander) phase detector. Use macromodels for XOR gates. Use 1 V for logic "1" and 0 V for logic "0" (Choose appropriate threshold voltages for comparators, switches, and wherever else required).

(a) Obtain the input-output characteristics (average of $UP - DN$ versus ϕ) by simulation.

(b) Plot the phase detector waveforms (for a few cycles) when the rising edge of the clock lags the middle of the data period by $\pi/8$.

3. Add an asynchronous reset switch to the D-flip-flop macromodel above. Using this, construct a 3-state phase detector. Use an ideal AND gate in the reset path.

(a) Obtain the input-output characteristics (average of $UP - DN$ versus ϕ, the phase difference between two waveforms at the same frequency) by simulation.

(b) Plot the phase detector waveforms (for a few cycles) when the rising edge of the clock lags the middle of the data period by $\pi/8$.

(c) Reason out what happens when the 3-state phase detector (Hint: Figure out which states the phase detector will be in) is driven by periodic waveforms of different frequencies and confirm by simulation.

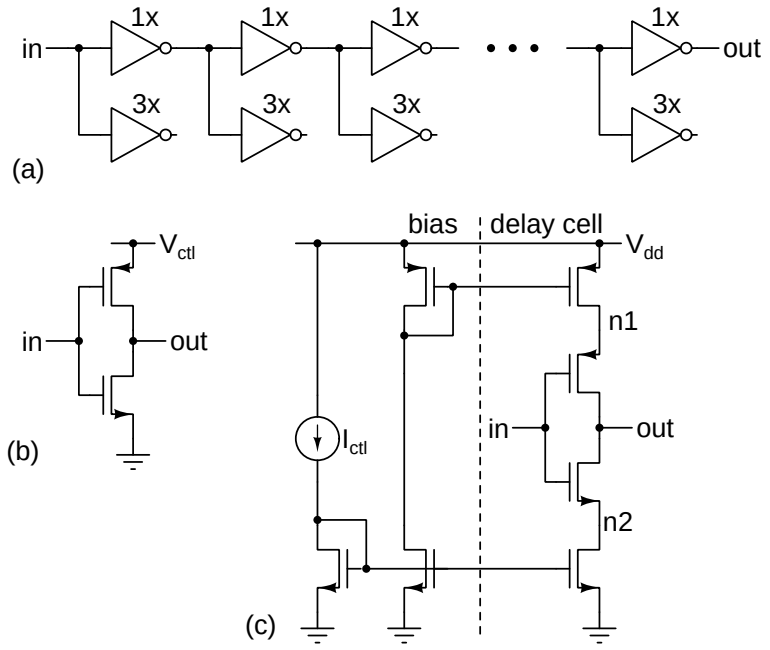

Figure 3: Problem 4 – (a) Delay line, (b) Inverter controlled by supply voltage, and (c) Current starved inverter.

4. Fig. 3(a) shows a delay line. Use the 45 nm CMOS process with a 1 V supply. Add 3 inverters to each node for additional loading (Inverters with a fan-out of 4 are used to estimate the delay of combinatorial logic circuits which use more complex gates. Here it is used to add parasitics which would appear in reality). Use a 1 GHz, 50% duty cycle square wave as the input in the following simulations.

(a) Realize the delay line using the inverter in Fig. 3(b) and determine the inverter delay and its rise and fall times (20 to 80%). Use minimum length transistors and $W/L = 4$ for nMOS. Adjust pMOS width to get nearly equal rise and fall times (It may not be possible to maintain this over the whole delay range. Make sure that it is true at the minimum delay setting). Simulate a chain with many inverters so that the output waveforms converge to the same shape. Compute the delay from that part of the chain whose input/output waveforms are the same.

(b) Plot the inverter delay versus supply voltage with the latter varying from 0.6 V to 1 V.

(c) Realize the delay line using the current starved inverter in Fig. 3(c). Use the same width for the two pMOS transistors and likewise for the two nMOS transistors. Use a common bias circuit for all inverters. As before, size the pMOS devices so that the rise and fall times are nearly the same (It may not be possible to maintain this over the whole delay range. Make sure that it is true at the minimum delay setting). Plot inverter delay and rise/fall times versus I_{ctl}. Choose the range of I_{ctl} such that at its minimum value, the delay is the same as that of Fig. 3(b) with $V_{ctl} = 0.6$ V and at its maximum value, the delay doesn't decrease any further.

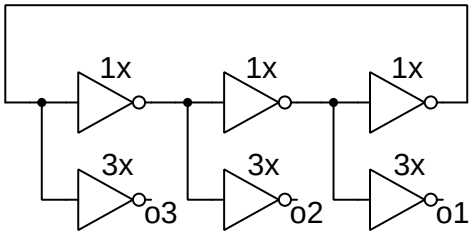

Figure 4: Problem 5 – Three-stage ring oscillator.

5. Use the inverters designed in the previous problem (Fig. 3(b, c)) to design the three-stage ring oscillator in Fig. 4. Use the same ranges for V_{ctl} and I_{ctl} as before and plot the oscillation frequency versus V_{ctl} and I_{ctl}. Also plot the power dissipation of the oscillators versus their oscillation frequency.

   Repeat for five-stage ring oscillators.

   Plot the eye diagram (for two periods) of the oscillation waveform at the highet frequency for the different ring oscillators.