Assignment-2: EE5325 - Power Management Integrated Circuits

Excercise-1

For a sub-1V bandgap voltage reference shown in Figure-1:

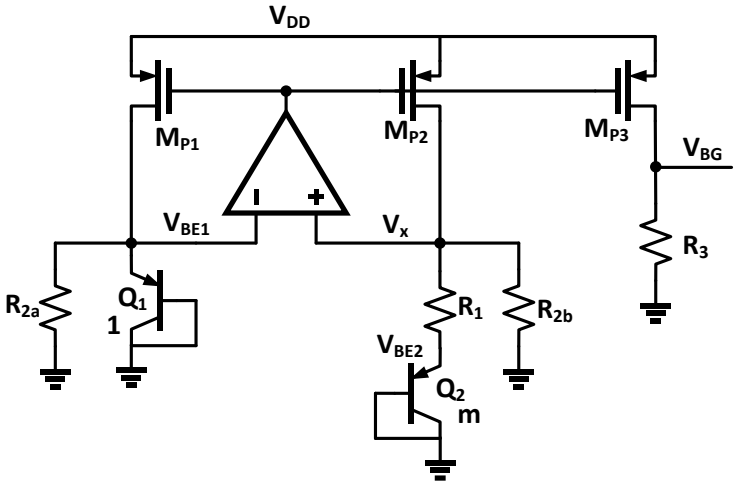

Figure-1

a) Assume m=10, I_{E_Q1}=I_{E_Q2}=5µA at room temperature and identical PMOS transistors, calculate the values of R_1, R_{2a}, R_{2b} and R_3 for V_{BG}=600mV.
b) Analyze the effect of mismatch between M_{P1}, M_{P2} and M_{P3}.
c) Analyze the effect of mismatch between R_{2a} and R_{2b}.
d) Analyze the effect of op-amp offset voltage and compare for m=5 and m=10.

Excercise-2

Consider the transfer function a standard 2nd order system:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Considering $\omega_n = 100\ krad/sec$, fill the values of poles, wp1 and wp2 in following table for the corresponding values of **ζ.**

ζ	Q=1/2 ζ	w_{p1} (rad/s)	w_{p2} (rad/s)
10			
1			
0.7			
0.5			
0.2			
0.1			

Exercise-3

For the non-inverting amplifier shown in Figure-A and considering the op-amp model shown in Figure-B where *A(s)=Vo(s)/Vi(s)*

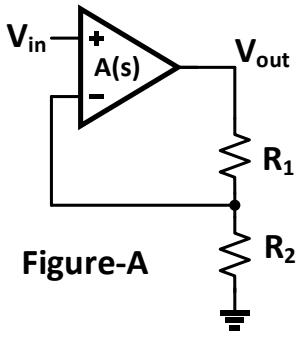

Figure-A

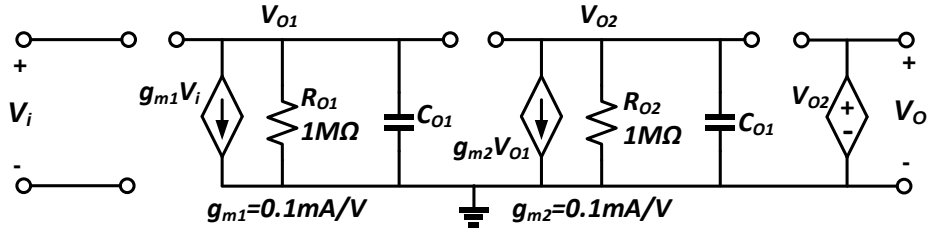

Figure-B

a) Find the loop gain transfer function, LG(s), DC gain A_o, poles p_{1_lg}, p_{2_lg} (roots of s) and their respective frequencies, w_{p1_lg} and w_{p2_lg} in terms of g_{m1}, R_{o1}, C_{o1}, g_{m2}, R_{o2} and C_{o2}.
b) Find the closed loop transfer function, $H(s)=V_{out}(s)/V_{in}(s)$, poles p_{1_cl}, p_{2_cl} (roots of s) and their respective frequencies, w_{p1_cl} and w_{p2_cl} in terms of g_{m1}, R_{o1}, C_{o1}, g_{m2}, R_{o2} and C_{o2}.
c) Prove that, the circuit in Figure-A behaves same as the 2nd order transfer function in exercise-2 for feedback factor, β=1 (i.e. R_1=0 or R_2=∞) and find the expressions for damping factor (ζ), quality factor (Q), natural frequency (w_n) in terms of loop gain pole frequencies, w_{p1_lg} and w_{p2_lg} and DC gain, A_o.
d) Considering g_{m1}=g_{m2}=0.1mA/V and R_{o1}=R_{o2}=1MΩ, fill the values in following table for the corresponding values of C_{o1} and C_{o2}

C_{o1} (F)	C_{o2} (F)	Loop Gain				Closed Loop			
		w_{p1_lg} (rad/s)	w_{p2_lg} (rad/s)	w_{ugf} (rad/s)	PM (deg.)	ζ	Q=1/2 ζ	w_{p1_cl} (rad/s)	w_{p2_cl} (rad/s)
1e-9	1e-9								
10e-9	1e-10								
4e-8	2.5e-11								
1e-7	1e-11								
1.41e-7	7.07e-12								
2e-7	5e-12								
5e-7	2e-12								
1e-6	1e-12								
2e-6	5e-13								
1e-5	1e-13								

e) Analyze the effect of increasing the frequency spacing between loop gain poles, w_{p1_lg} and w_{p2_lg} on damping factor.

f) Plot phase margin (PM) vs. ζ and find the range of ζ for which phase margin can be calculated as 90-100 times of ζ.

g) Enter the circuit in LTSpice and perform following simulations for all the values of w_{p1_lg}, w_{p2_lg}:
   i. Plot the bode magnitude phase and phase response of the loop gain transfer function for all values of w_{p1_lg}, w_{p2_lg} and corresponding AC magnitude and phase response of the closed loop transfer function. Comment on effect of increasing and decreasing phase margin on the closed loop AC magnitude and phase response.
   ii. Plot the step response of the closed loop circuit by applying a unit step (0 to 1V with initial delay of 10us and Trise = 1ns) for the time span of 10ms. Comment on the effect of increasing and decreasing phase margin as well as ζ. Find the phase margin and corresponding value of ζ for the fastest settling (when output settles within 95% of the final value).

h) Change the value of feedback factor, β=1/10 (i.e. R_1=10R_2) and comment about the effect on phase margin, damping factor and unity gain frequency (w_{ugf})