Time-Based Voltage Regulators

EE5325 Power Management Integrated Circuits

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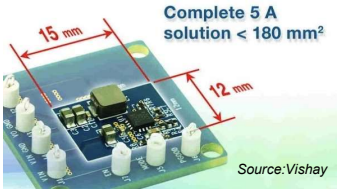
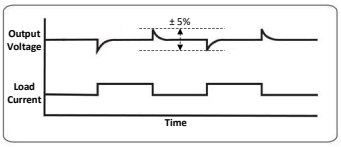
DC-DC Converter Wish List

- **High Power Density**
  - Higher efficiency to reduce heat dissipation
  - Smaller passive components to reduce board space
  - Shrinking die size by innovative controller and integrating more features on single PMIC

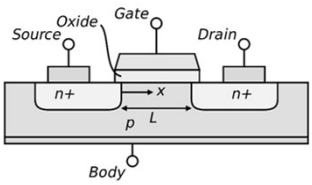


- **Stable Supply**
  - High performance controller design



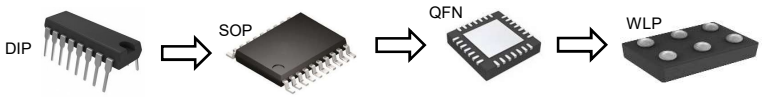
Technology Trends in PMIC

- **Scaling semiconductor process technology**
  - Higher speed Power FETs
  - Smaller Size

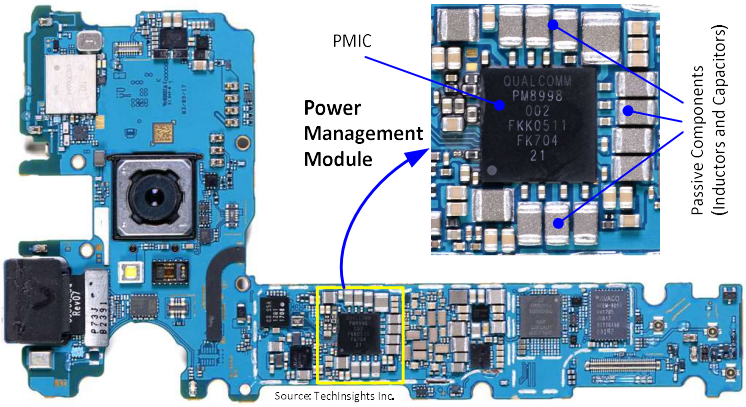


0.5µm → 0.35µm → 0.18µm

- **Low parasitic packaging technologies (WLP, BGA)**
  - Smaller Parasitic



PMIC vs Passive Size



Samsung Galaxy S8

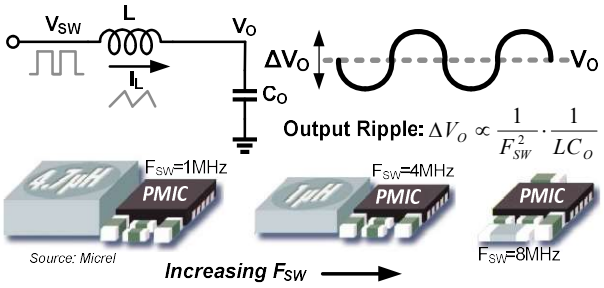
External Passive components (L and C) occupy 2/3rd of the total power module size

Passive Size Reduction

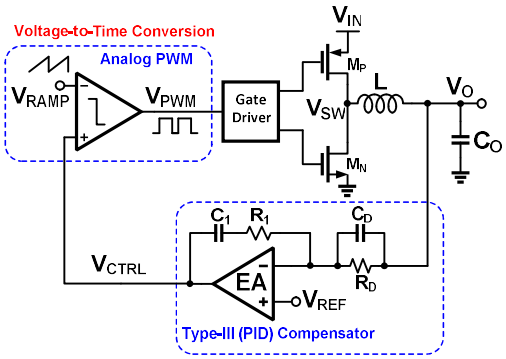
- Output ripple is a function of inductor (L), capacitor (C) and switching frequency (F_{SW})

$$\Delta V_O = \frac{V_{IN} D(1-D)}{8 F_{SW}^2 L C_O}$$

- Doubling switching frequency reduces passive components by 4x for the same output ripple



Limitations of Analog Controller



- PID Compensator
  - Area/power inefficient
- Error Amplifier (EA)
  - Bandwidth limits transient response
- Ramp Generator
  - Limits switching frequency
- PWM Comparator
  - Delay limits output range

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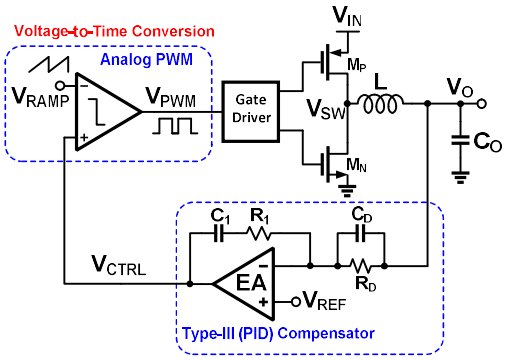

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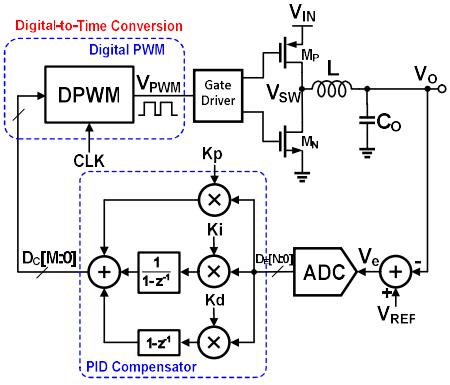
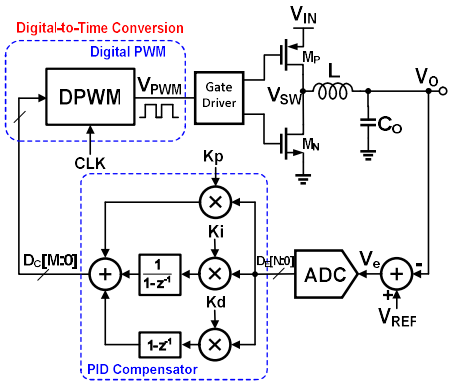
Significant power penalty at high F_{SW}

Digital Controller Design Challenges



- Small controller area at low Fsw
- Non-linear loop dynamics
  - Steady state is a bounded limit cycle → large ripple
- ADC res. > reg. accuracy
  - 0.1% accuracy → 10bit
- DPWM res. ≈ inverter delay
  - Large area and power
- $F_{CLK} >> F_{SW}$

Digital Controller Design Challenges



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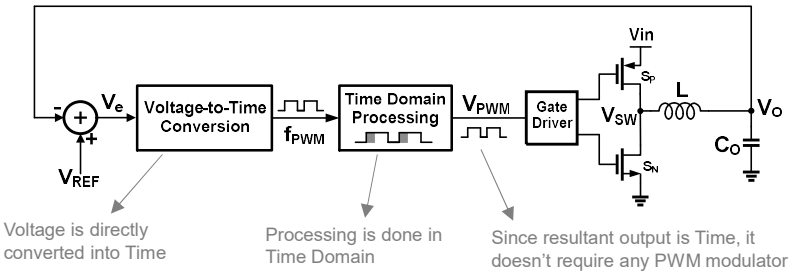
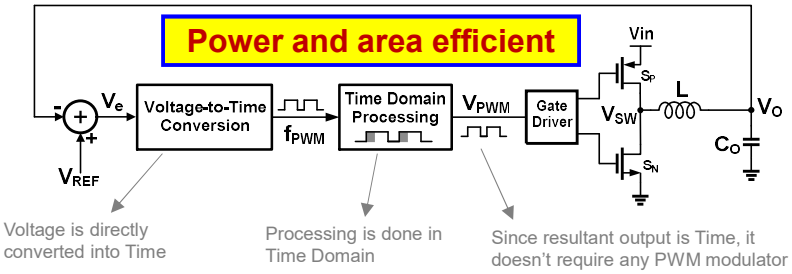
Significant power & area penalty at high F_{SW}

Time Based Controlled DC-DC Converter



- Preserves benefits of both analog (low power, high accuracy) and digital (process scaling, low voltage operation, area efficient) without using any A/D or error amplifier
- Implicit PWM generation → Eliminates PWM modulator hence minimum delay

Time Based Controlled DC-DC Converter



- **Preserves benefits of both analog (low power, high accuracy) and digital (process scaling, low voltage operation, area efficient) without using any A/D or error amplifier**
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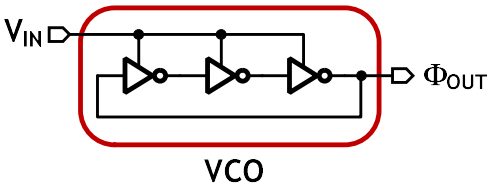
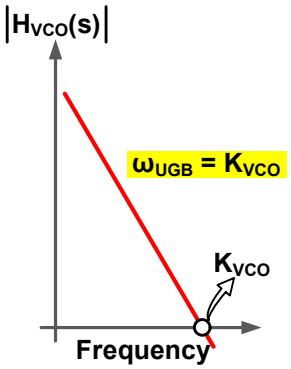
VCO as Time-based Integrator



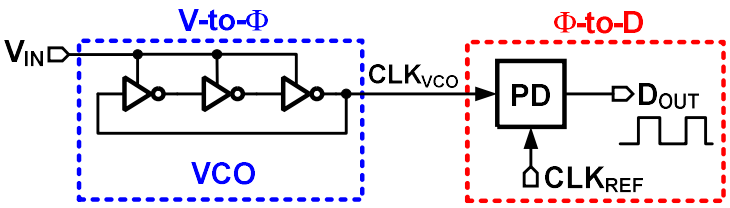


$$\omega_{OUT} = V_{IN} K_{VCO} \qquad \omega_{OUT} = \frac{d\Phi_{OUT}}{dt}$$

$$H_{VCO}(s) = \frac{\Phi_{OUT}(s)}{V_{IN}(s)} = \frac{K_{VCO}}{s}$$

VCO acts as an ideal V-to-Φ integrator

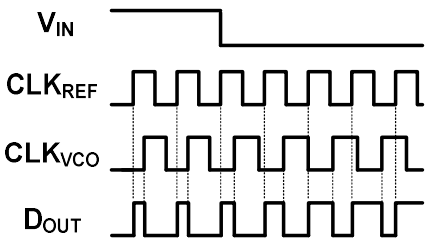
VCO Behavior in Time Domain



$$\Phi_{D_{OUT}} - \Phi_{CLK_{REF}} = K_{VCO} \int_0^t V_{IN}(\tau)\, d\tau$$

$$D_{OUT} = \frac{\Phi_{D_{OUT}} - \Phi_{CLK_{REF}}}{2\pi}$$

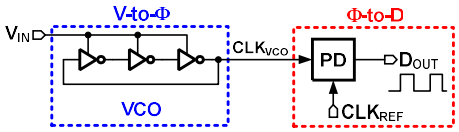
$$\boxed{D_{OUT} = \frac{K_{VCO}}{2\pi} \int_0^t V_{IN}(\tau)\, d\tau}$$

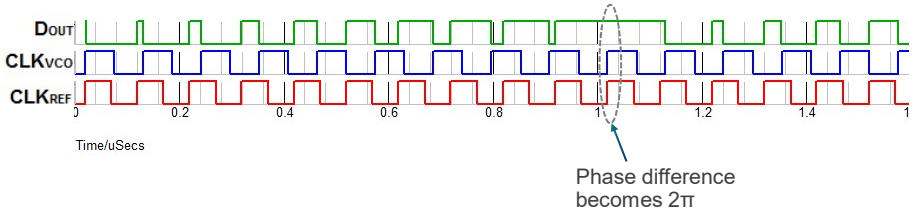


Example of Phase Accumulation

f_o =10MHz (free running frequency of VCO)
Or $\omega_o = 2\pi \cdot 10$MHz
K_{VCO}=2πMrad/s/V

Then phase difference will become 2π every 10th cycle of the clock

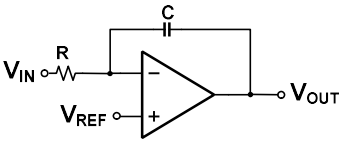


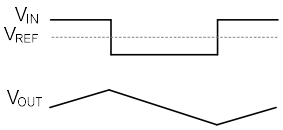


Opamp-RC vs Time Based Integrator

Voltage Based Integrator

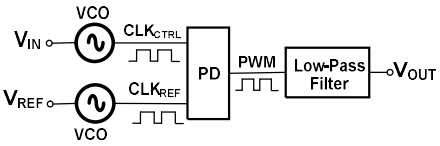
- Input voltage is integrated as voltage
- Integral Gain = 1/RC

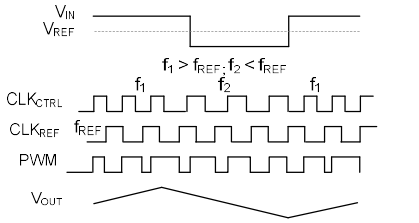




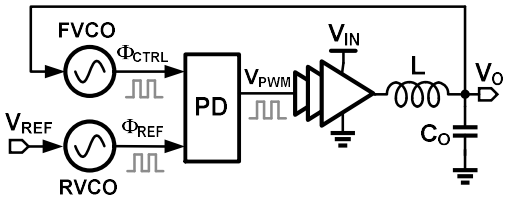
Time Based Integrator

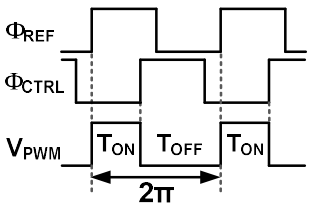
- Input voltage is integrated as phase (time) by VCO
- Integral Gain = K_{VCO}





Buck w/ Time-based Type-I Controller





- Acts as a Frequency Locked Loop, FLL
- In steady state : $f_{FVCO} = f_{RVCO} \Rightarrow V_O = V_{REF} = D \cdot V_{IN}$

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{(\Phi_{CTRL} - \Phi_{REF})}{2 \cdot \pi} = \frac{V_O}{V_{IN}}$$

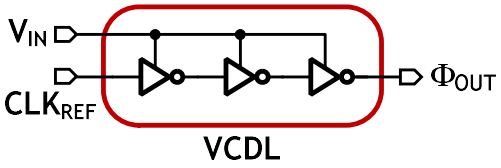
Time Based PID Controller

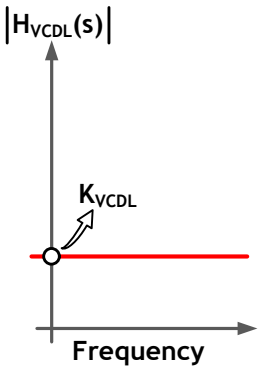
$$H_{PID}(s) = K_P + \frac{K_I}{s} + K_D s$$

Need 3 functions to realize time based PID compensator:

1. **Time based Integrator → VCO**
2. **Time based Proportional (Gain) → ?**
3. **Time based Differentiator → ?**

Time-based Proportional Control



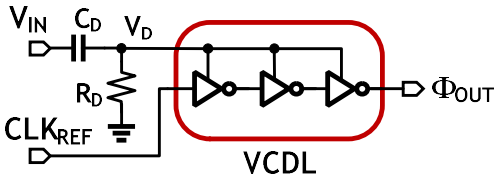


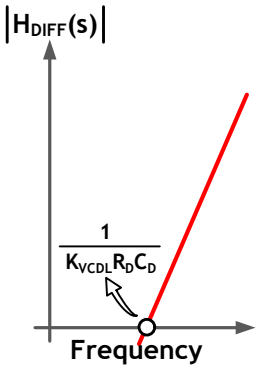
$$\Phi_{OUT} = \Phi_{CLK_{REF}} + K_{VCDL} \cdot V_{IN}$$

$$H_{VCDL}(s) = \frac{\Phi_{OUT}(s)}{V_{IN}(s)} = K_{VCDL}$$

VCDL acts as an ideal V-to-Φ converter

Time-based Differentiator



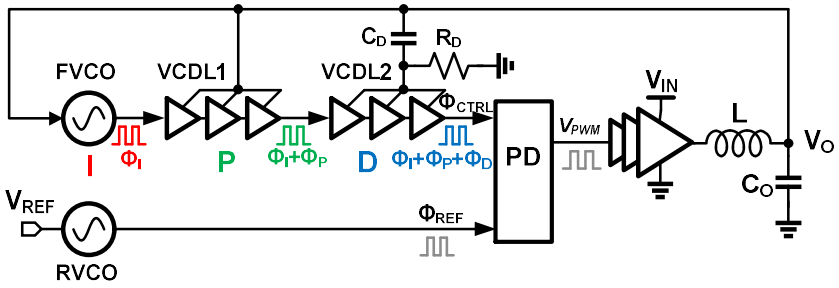


$$\Phi_{OUT} \approx \Phi_{CLK_{REF}} + K_{VCDL} R_D C_D \cdot \frac{dV_{IN}}{dt}$$

$$H_{DIFF}(s) = \frac{\Phi_{OUT}(s)}{V_{IN}(s)} = K_{VCDL} R_D C_D s$$

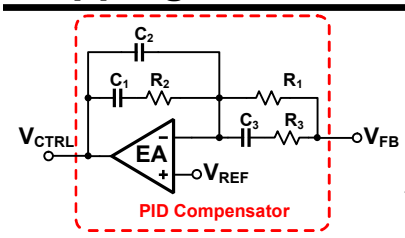
H.P. filter + VCDL acts as an ideal V-to-Φ differentiator

Buck Converter with T-PID Controller



- Integral gain → K_{VCO} of FVCO
- Proportional gain → K_{VCDL} of $VCDL_1$
- Derivative gain → R_DC_D and K_{VCDL} of $VCDL_2$

Mapping V-PID to T-PID (1)



$$where, G = \frac{R_2}{R_1}$$

$$H^V{}_{PID}(s) = G \cdot w_{z1} \frac{(1+\frac{s}{w_{z1}})(1+\frac{s}{w_{z2}})}{s(1+\frac{s}{w_p})}$$

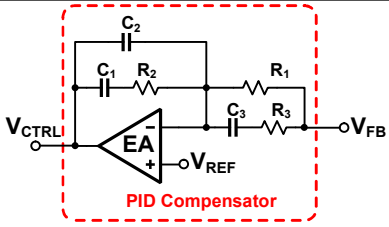
Ignoring w_p and simplifying

$$H^V{}_{PID}(s) = G \cdot \left\{ \left(1 + \frac{w_{z1}}{w_{z2}}\right) + w_{z1}\frac{1}{s} + \frac{1}{w_{z2}}s \right\}$$

Comparing with standard $H_{PID}(s) = K_P + \frac{K_I}{s} + K_D s$

$$K^V{}_P = G \cdot \left(1 + \frac{w_{z1}}{w_{z2}}\right) \qquad K^V{}_I = G \cdot w_{z1} \qquad K^V{}_D = \frac{G}{w_{z2}}$$

Mapping V-PID to T-PID (1)



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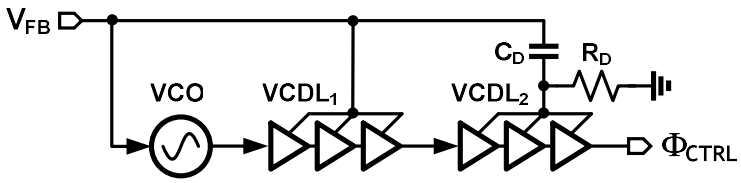
Proportional Integral Derivative

Mapping V-PID to T-PID (2)

$$H^V{}_{PID}(s) = G \cdot \left\{ \left(1 + \frac{w_{z1}}{w_{z2}}\right) + w_{z1}\frac{1}{s} + \frac{1}{w_{z2}}s \right\}$$



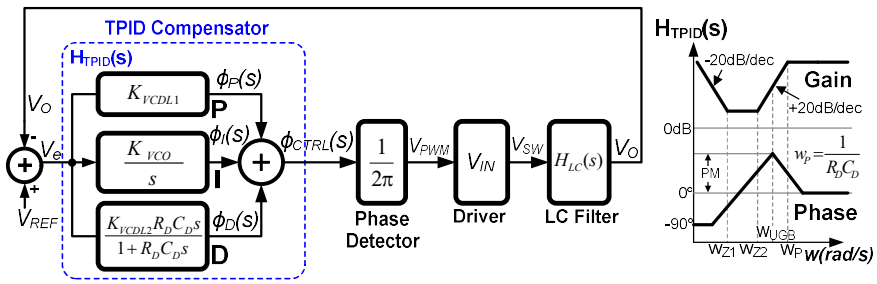
$$H^T{}_{PID}(s) = K_{VCDL1} + K_{VCO}\frac{1}{s} + K_{VCDL2}R_D C_D s$$

$K^T{}_P = K_{VCDL_1}$ $\quad K^V{}_P = G \cdot \left(1 + \frac{\omega_{z1}}{\omega_{z2}}\right)$

$K^T{}_I = K_{VCO}$ $\quad K^V{}_I = G \cdot \omega_{z1}$

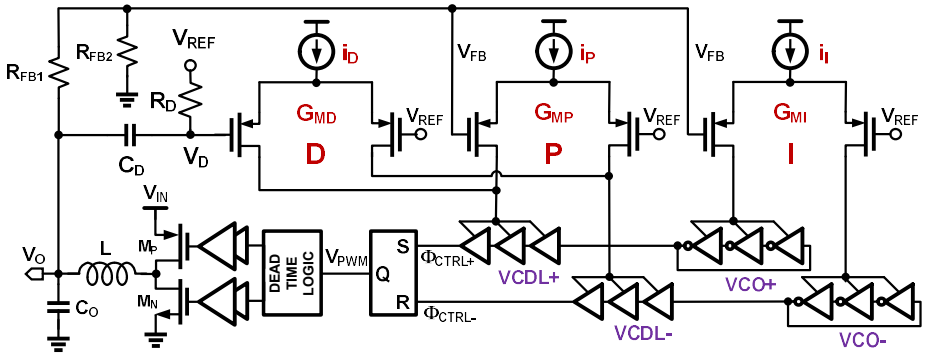
$K^T{}_D = K_{VCDL_2}R_D C_D$ $\quad K^V{}_D = \frac{G}{\omega_{z2}}$

T-PID Transfer Function



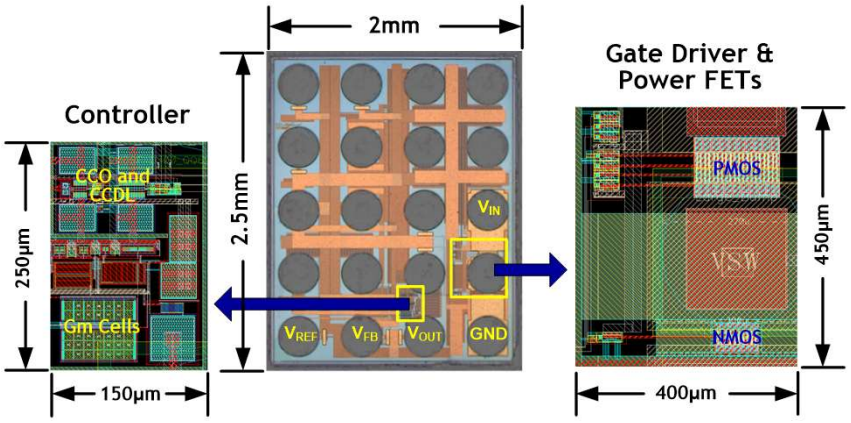
$$K_{VCO} = K_I \qquad K_{VCDL1} = K_I\left(\frac{1}{w_{z1}} + \frac{1}{w_{z2}}\right) \qquad K_{VCDL2} = \frac{1}{R_D C_D}\cdot\frac{1}{w_{z1}\cdot w_{z2}}$$

Circuit Implementation



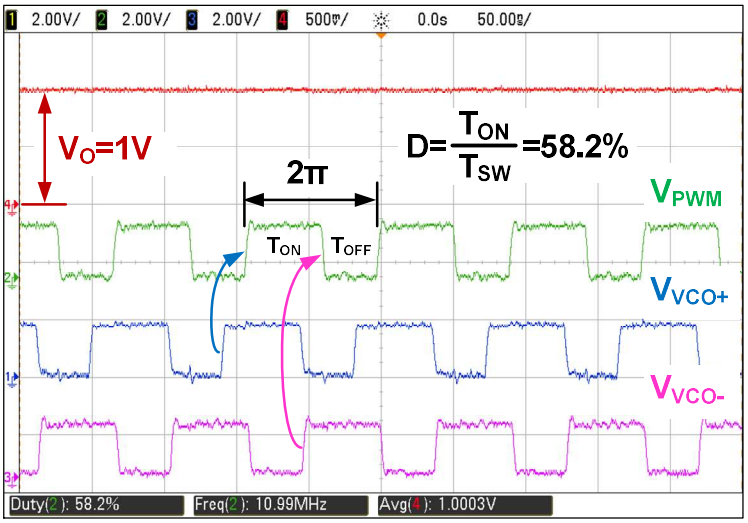
- Phase detector is implemented with SR latch
- Fully differential control eliminates reference clock
- Shared VCDL for proportional and derivative control

Prototype Buck Converter in 180nm CMOS

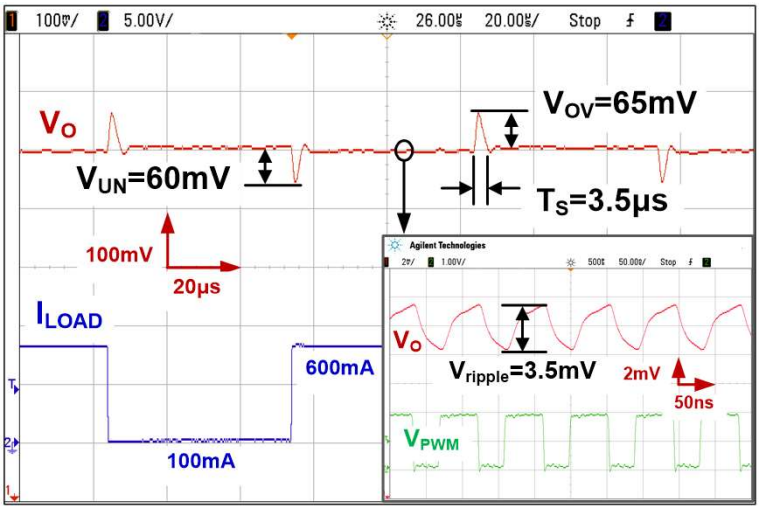


- "A 10–25 MHz, 600 mA buck converter using time-based PID compensator with 2µA/MHz quiescent current, 94% peak efficiency, and 1MHz BW," *Symposium on VLSI Circuits (VLSIC), June 2014.*
- "High frequency buck converter design using time-based control techniques," *IEEE JSSC, Apr. 2015.*

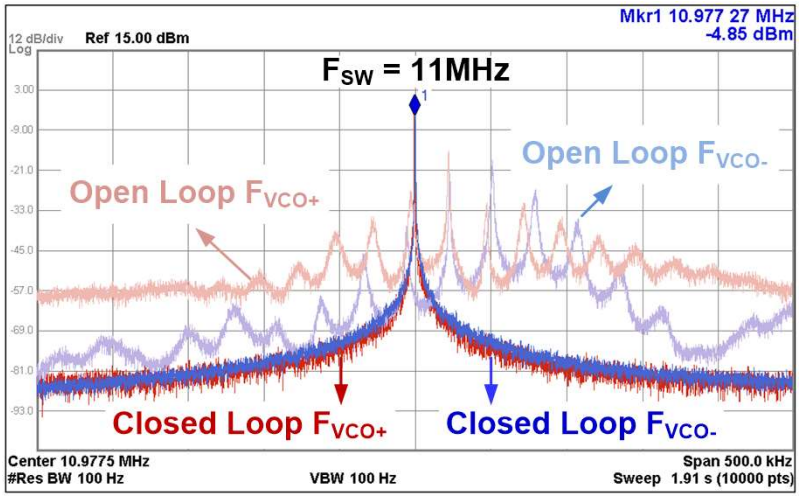
Steady-State Waveforms (V_O = 1V)



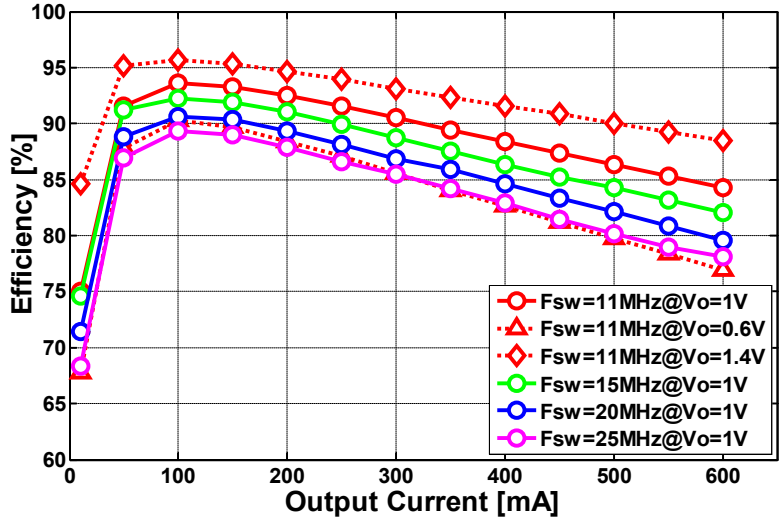
Load Transient Response



Oscillator Frequency Spectra



Efficiency vs. Output Current

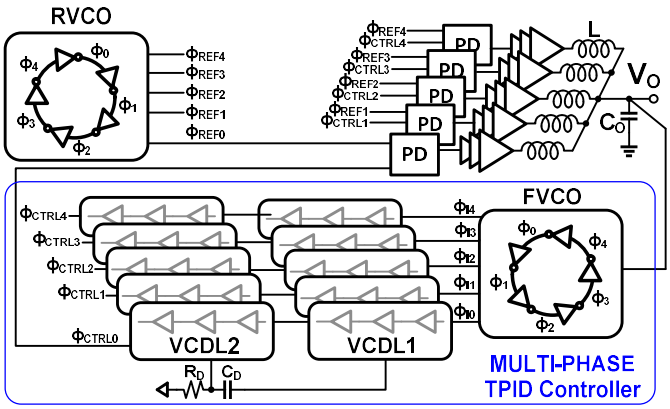


Performance Summary

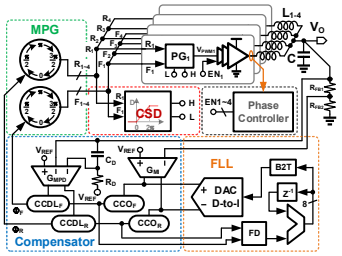
Publication	ISSCC 2014	This Work
Control Loop	Voltage mode PID	Time based PID
Process	0.13µm CMOS	0.18µm CMOS
Supply Voltage	3.3V	1.8V
Output Voltage	0.37V – 2.85V	0.6V – 1.5V
F_{SW}	10MHz(30MHz)	11-15MHz
L / C	330nH/3.3µF(1uF)	220nH/4.7µF
Max. Load Current	1.5A@V_O=2.4V	600mA
Settling Time	n/a	3.5µs
Output Ripple	n/a	3.5mV
Controller Current	n/a	23µA@11MHz
Peak Efficiency	91.8%(86.6%)	94%@V_O=1V
Active Area	n/a	0.24mm^2

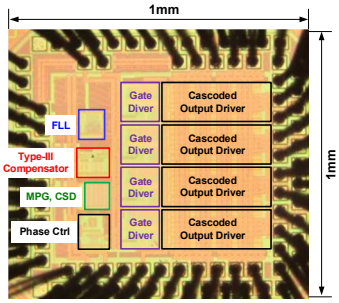
Application in Multi-Phase

- Since VCOs come inherently with multiple phases, different phases from VCOs can be tapped
- All phases use common integrator (VCO) but separate VCDLs



30-70MHz 4-Phase Time-Based Buck





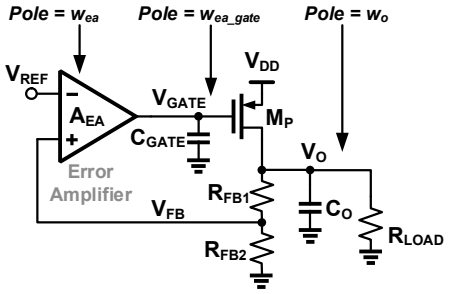
	This Work	JSSC `05 Hazucha	JSSC `09 P. Li	VLSI`14 Harish
Process	65nm CMOS	90nm CMOS	0.5µm CMOS	22nm CMOS
Control	T-PID PWM	Hysteretic	Hysteretic	Digital PWM
Synchronization	MPG	Injection	DLL	DPWM
Number of Phases	4	4	4	4
Input Supply [V]	1.8	1.2/1.4	4-5	1.5
Output Voltage [V]	0.6-1.5	0.9/1.1	0.86-3.93	1
F_{SW}[MHz]	30-70	233	25-70	500
Inductance [nH]	90	2.5	110-220	1.5
Capacitance [nF]	470	6.8	8-190	10
Load Current [A]	0.8	0.3/0.4	1	N/A
Controller Current	90µA@30MHz	N/A	N/A	N/A
Peak Efficiency [%]	87@V_O=1V	83.2/84.5	83@V_O=3.3V	68@V_O=1V
Power Density [W/mm^2]	2.5	1.93/3.14	1.2	N/A

- A 1.8V 30-to-70MHz 87% Peak Efficiency 0.32mm2 4-Phase Time-Based Buck Converter Consuming 3uA/MHz Quiescent Current in 65nm CMOS, " *ISSCC-2015.*
- A 4-phase 30-70 MHz switching frequency buck converter using a time-based compensator," *IEEE JSSC, Dec. 2015*

Time-Based Low Drop-Out Regulator (LDO)

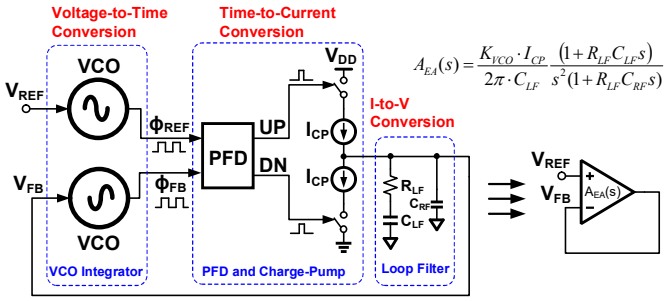
Low Drop-Out Regulator

- A conventional low drop-out regulator (LDO) suffers from trade-off between power and area.
- Pole, w_o, worsens the situation particularly under light-load condition due to high output resistance.
- Most of state-of-the art LDOs either consume high quiescent current, large on-chip capacitance or achieve limited bandwidth.
- Reduced bandwidth degrades power supply rejection (PSR) and transient response.



Time-Based Error Amplifier

- Concept of time-based error amplifier is derived from type-II phase locked loop (PLL).
- A voltage-controlled oscillator (VCO) is used for voltage-to-time/phase conversion which also acts as a phase integrator.
- Under lock condition, $F_{FB}=F_{REF}$ → $V_{FB}=V_{REF}$, assuming two VCOs are identical.

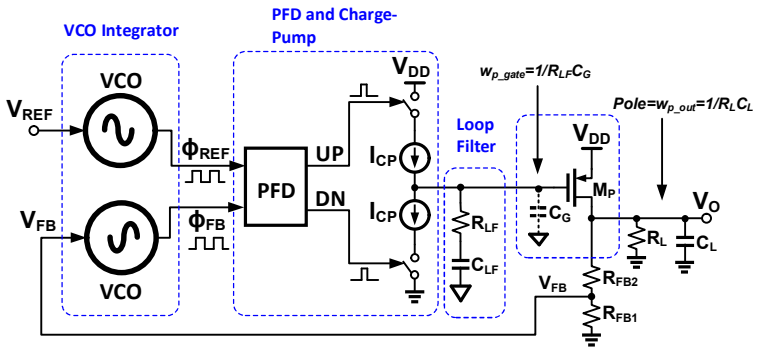


$$A_{EA}(s)=\frac{K_{VCO}\cdot I_{CP}}{2\pi\cdot C_{LF}}\frac{(1+R_{LF}C_{LF}s)}{s^2(1+R_{LF}C_{RF}s)}$$

Time-Based LDO

- Concept of time-based error amplifier can be extended to LDO by adding a pass element, M_P to drive the output load R_L and C_L.

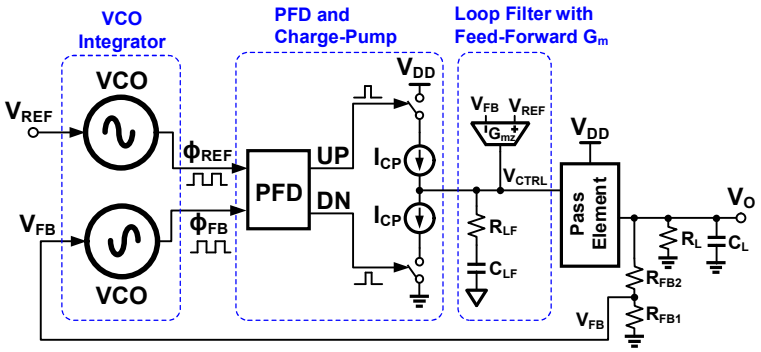
$$H_{LG}(s) = \frac{A_{PE} \cdot \beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot C_{LF}} \cdot \frac{(1 + w_{z\_LF})}{s^2(1 + w_{p\_gate})(1 + w_{p\_out})}$$



Time-Based LDO with FF Compensation

- Feed-forward compensation cancels one of the poles (w_{p_gate} and w_{p_out}) and stabilizes the loop

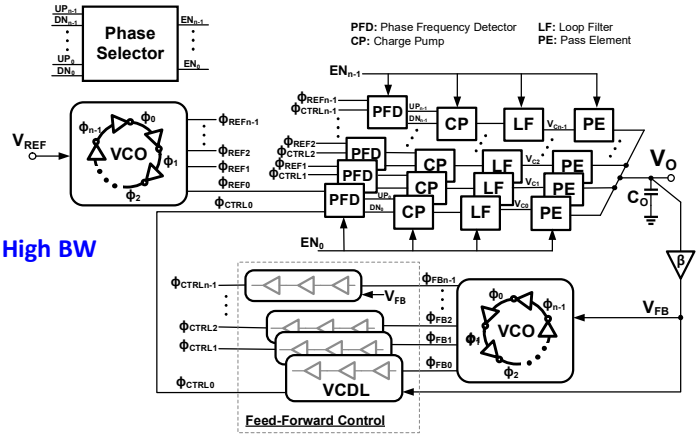
$$H_{LG}(s) = \frac{A_{PE} \cdot \beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot C_{LF}} \cdot \frac{(1 + w_{z\_LF})(1 + w_{z\_FF})}{s^2(1 + w_{p\_out})} \qquad w_{z\_FF} = \frac{\beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot G_{mz}}$$



Area and Current Efficient Capacitor-Less Low Drop-Out Regulator Using Time-Based Error Amplifier, ISCAS-2018, Florence, Italy, May, 2018.

Multi-Phase Time-Based LDO

- Auto-Reconfigurable → numbers of phases are turned on/off based on load currents
- Seamless transition between number of phases

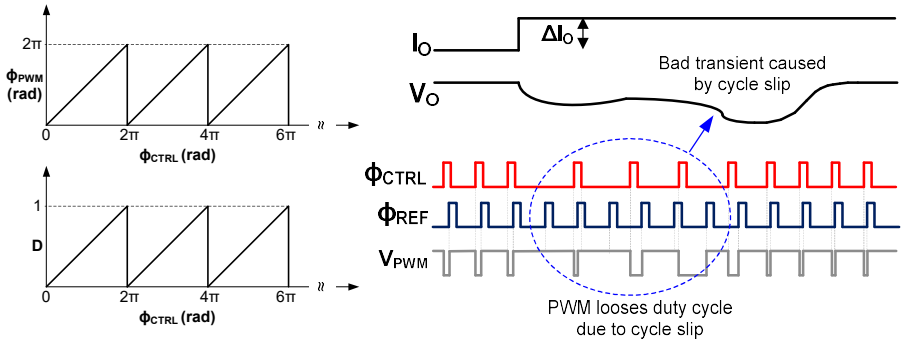


- Low IQ and High BW

Issues with Time-Based Controller

Problem-1: Cycle Slipping

- Since VCO phase folds back after every 2π, it causes duty cycle to reset and losing the duty cycle lock
- Duty cycle slipping may cause instability in the output before it acquires the phase lock again



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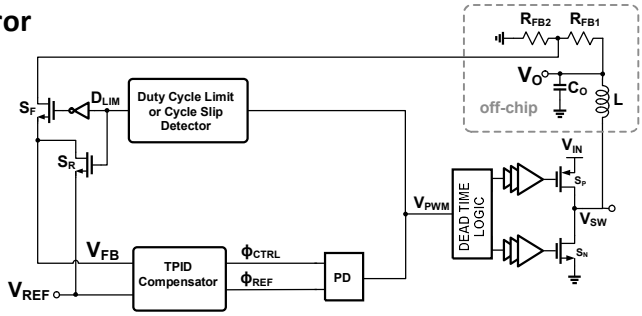
Solution: How to Avoid Duty Cycle Slip

- A cycle slip or min/max duty cycle detector can be used
- Once cycle slip is detected, error current to VCOs is made zero by applying V_{REF} to V_{FB}
- VCO phase will not accumulate further when there is no error



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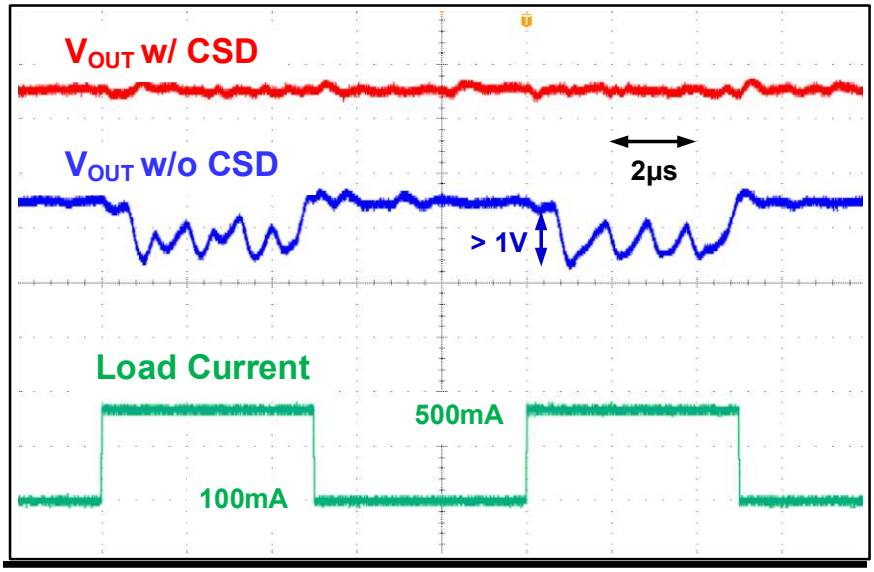
CSD Operation



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Problem-2: Offset Due to VCO Mismatch

- Since any error between frequencies of two VCOs is integrated in phase, mismatch in VCOs will cause offset in input voltage
- Considering 10MHz frequency and K_{VCO} of 1MHz/V, 1% mismatch in VCO will introduce 100KHz offset in frequency
- Assuming offset frequency due to mismatch is Δf_{VCO}, absolute input referred offset voltage can be represented as:

$$V_{OS} = \frac{\Delta f_{VCO}}{K_{VCO}}$$

- 1% between VCOs causes 100mV offset which is 16.67% for V_{REF}=600mV.

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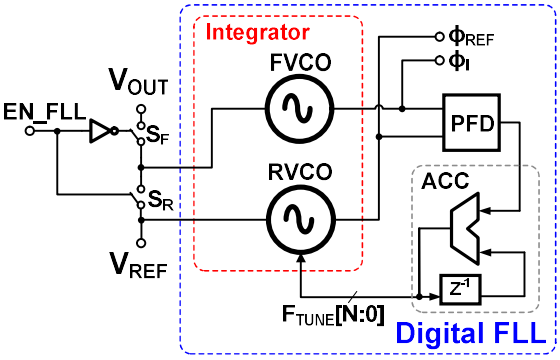
Solution: Offset Cancellation

- Mismatch between VCOs can be corrected by locking two VCOs to same frequency during startup
- Digital FLL is used for frequency locking
- Any offset in Gm also gets corrected during the calibration



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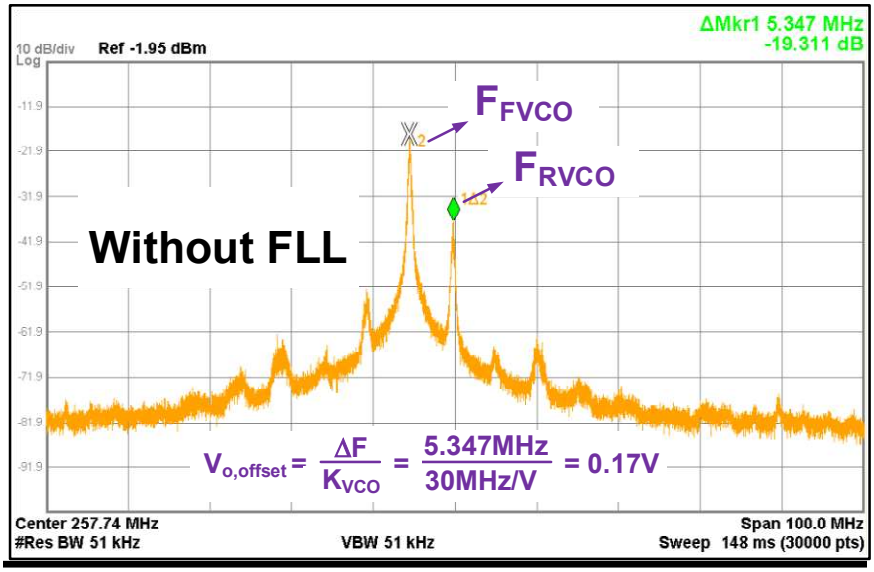
Oscillator Frequency Spectra



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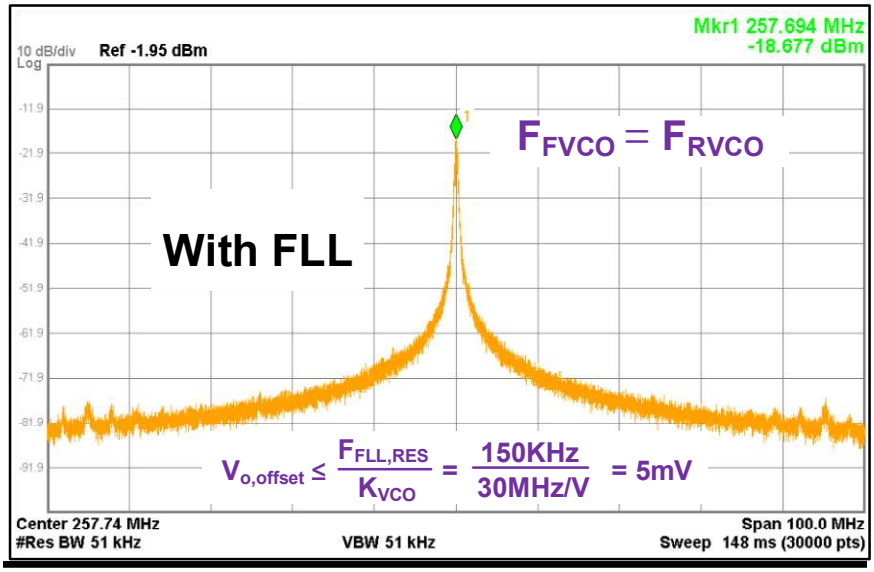
Oscillator Frequency Spectra



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