Analog Layout Techniques

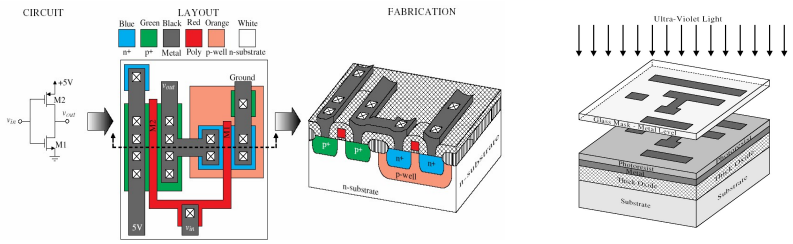
EE5325 Power Management Integrated Circuits

Dr. Qadeer Ahmad Khan

Integrated Circuits and Systems Group
Department of Electrical Engineering
IIT Madras

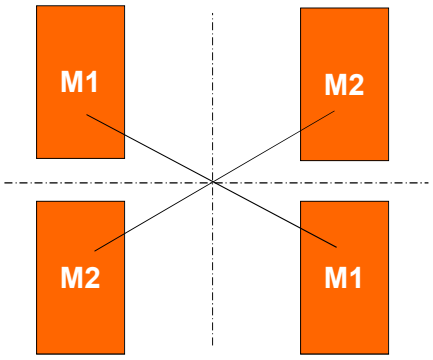
Introduction

- **The layout design is the representation of electrical design in form of many distinct geometrical rectangles at various level**
- **The layout is used to create the mask that enables the fabrication of chip**



Device Matching

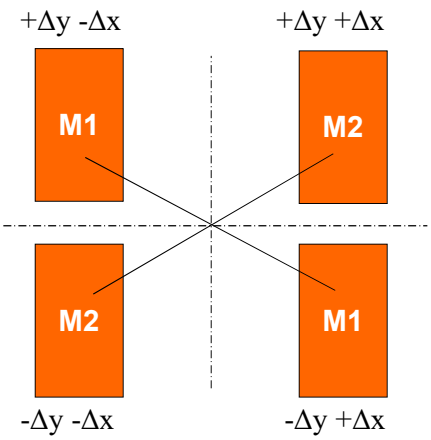
- **Common centroid: common centroid technique is used to compensate the mismatch in devices due to non-idealities of process and operating conditions.**



All the matched devices are placed along diagonals in such a ways that all the diagonals should intersect at the centre.

Device Matching

- **How the variations are cancelled out**



Assuming the varaition in y-axis is ±Δy and in x-axis is ± Δx

Total variation in M1:

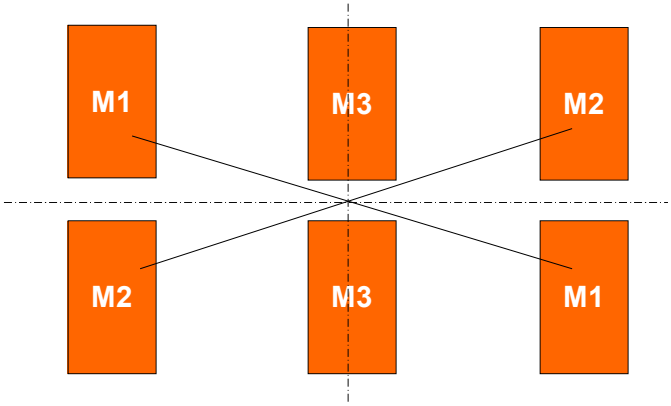
= +Δy-Δx -Δy +Δx = 0

Total variation in M2:

= +Δy +Δx -Δy –Δx = 0

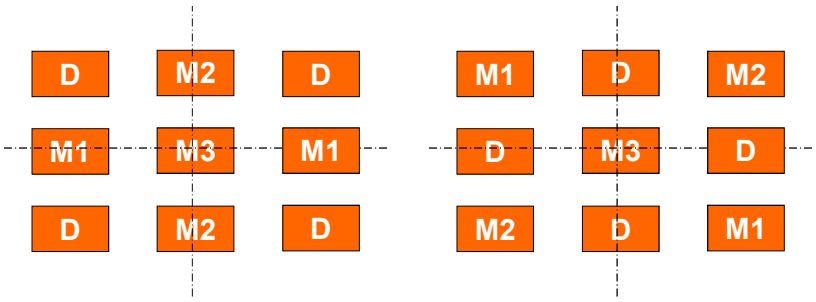
Device Matching

- Common centroid for three matched devices



Device Matching

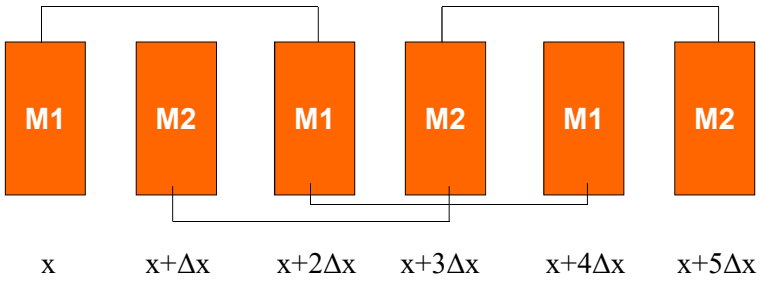
- Common centroid for unequal number of devices



Dummy device D are inserted for proper matching

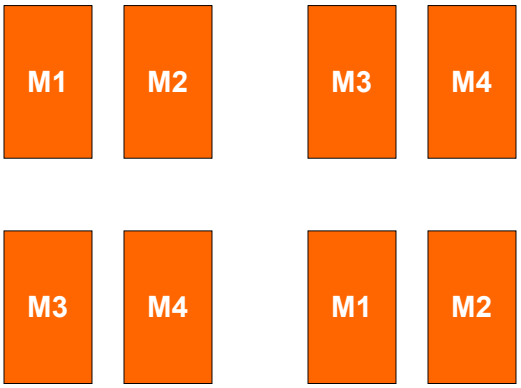
Device Matching

- Intergitized layout: the cells are placed in alternate order to average out the variation
  - Generally used when less no. of devices are to be matched (2 or 3)



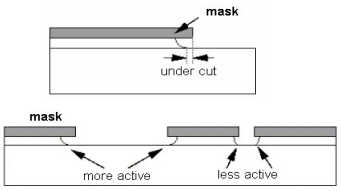
Device Matching

- Combination of common centroid and Intergitized layout could also be used

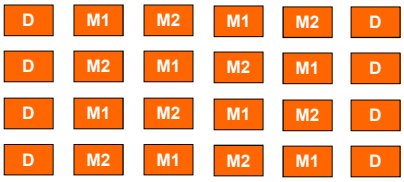


Device Matching

- **Dummy cells**
  - **Mismatch occurs due to boundary dependant etching, CMP and doping**
  - **Addition of dummy cells at the boundary helps in improving matching.**
  - **All the matched devices see same adjacent structure**



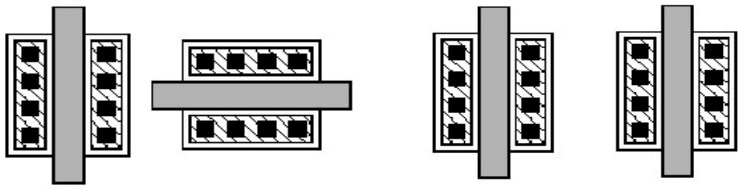
Edge effect during etching



Use of dummy cells to avoid effect in matched devices

Device Matching

- **Orientation**
  - **Matched devices should have identical orientation**



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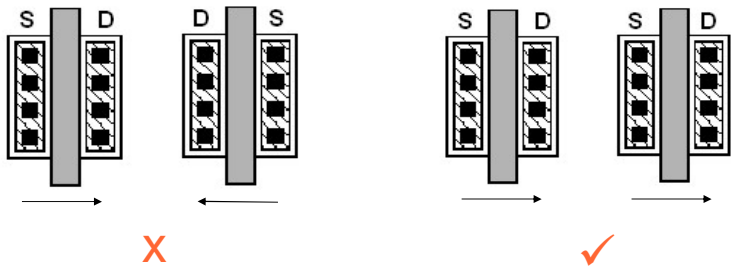
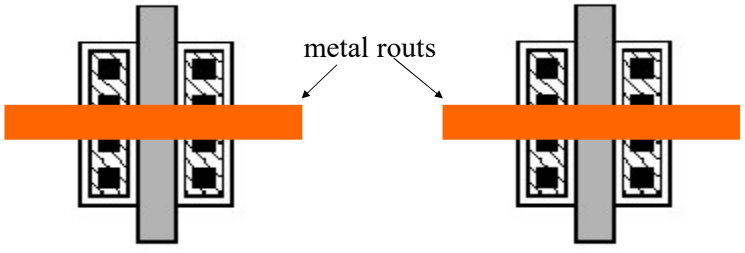
Device Matching

- Direction of current
  - Matched devices should have the same direction of current flow



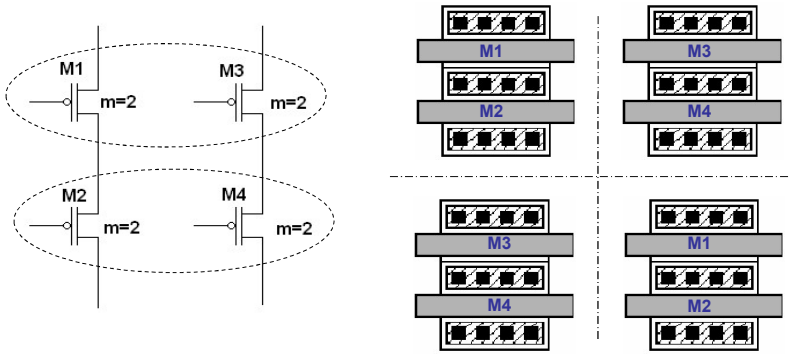
Device Matching

- Dummy routs: if a signal is routed over one device then identical dummy rout should be put on the other device



Device Matching

- Layout of matched cascode devices

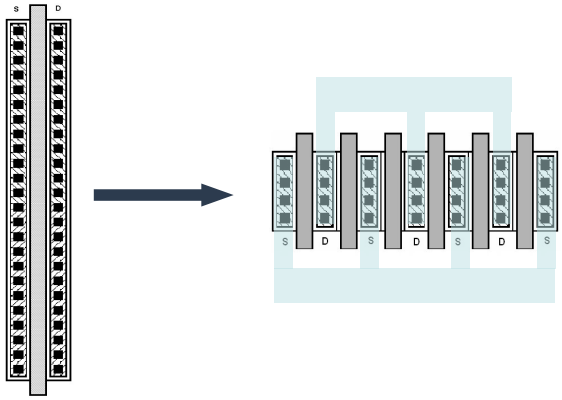


Device Matching

- Guidelines for matching
  - Use multiple number of devices with same unit size and change muliplier as per the requirement
  - Use interdigitated or common centroid
  - Even number of multipliers help in better matching
  - Dummy cells should be used at boundary to take out the edge effect
  - Use antenna diodes(diffusion) at the gate of matched devices to avoid Vt mismatch due to charge injection
  - Don't rout voltages a long way – IR drops can cause big mismatch
  - Matched signals should be routed together and in the same metal
  - Matched devices should be palced in close proximity
  - Don't use cells with very small W & L as they may cause bigger mismatch
  - Routing should be avoided over the gate of critically matched transistors

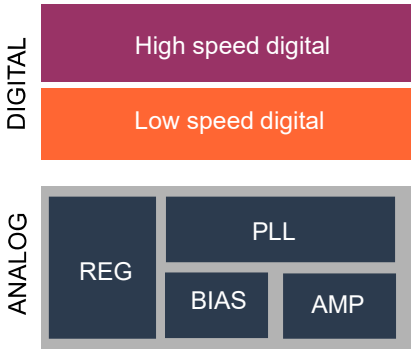
Fingering of transistors

- The multi finger technique enables the sharing of drain/source hence reducing the parasitic caps
- Reduces the gate resistance – helps in fast charging



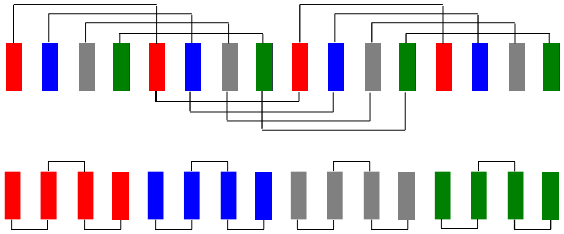
Placement

- All the analog should be placed together
- Separate the analog and digital blocks as much as possible
- Should be kept away from switching I/Os
- It is preferable to keep the regulator near supply pad to minimize the ESR of external de-cap



Laying out Resistors

- Matching techniques should be used for critically matched resistors and capacitors
- Head contacts should be increased to reduce the mismatch due to contact resistance
- Special care should be taken while routing of matched resistors/capacitors to avoid any mismatch due to routings
- For timing critical applications, sometimes common centroid/interdigitized is not preferred because of routing parasitic – A simple straight method is used



interdigitized
- good resistor matching
- complex routing
- large parasitics

simple
- poor resistor matching
- simple routing
- reduced parasitics

Laying out 4 matched resistors in two different manners

Guidelines for Resistors and capacitors

- For proper matching the size of resistors and capacitors should not be too small
- The matched capacitors and resistors should be placed closely but minimum spacing is required to avoid any kind of signal coupling if there is any
- For fringe caps it's recommended to use odd number of fingers
- Always use dummy capacitors and resistors at boundaries to avoid edge effect

Noise decoupling and shielding

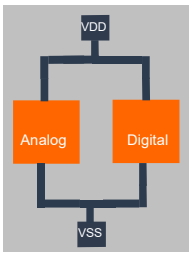
- All the critical signals should be shielded with gnd or clean reference signal
- For high speed signals, the shield line shouldn't be put closer to the signal to avoid loading
- Use proper spacing between two signal

Signal route with two side shielding

Cross section of a signal route with four side shielding

Noise decoupling and shielding

- Supply and ground routings
  - Digital and analog blocks should have separate supply and ground pads to minimize the ground/supply noise due to Ldi/dt and IR drops
  - If separate pads are not possible then the two supplies should be star connected from pad



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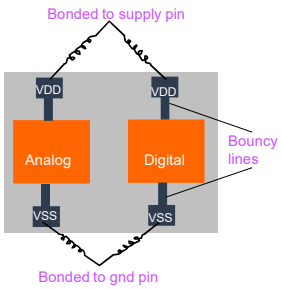

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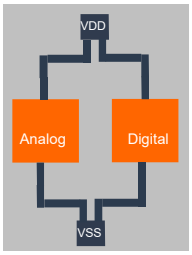

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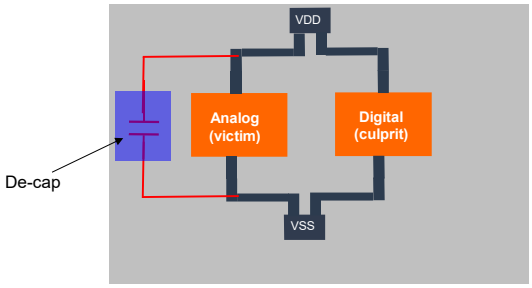
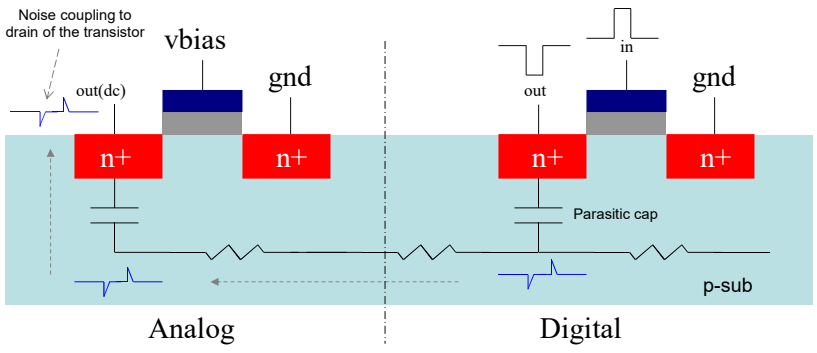
Noise decoupling and shielding

- **Decoupling caps**
  - Decoupling caps helps in filtering supply noise caused by switching
  - On-chip de-caps are more effective as they are more closure to the both culprit and victim hence have lower ESR
  - De-caps should be put as close as possible to prevent it from propagating further. It should be ensured to connect the decap with reference to clean gnd.



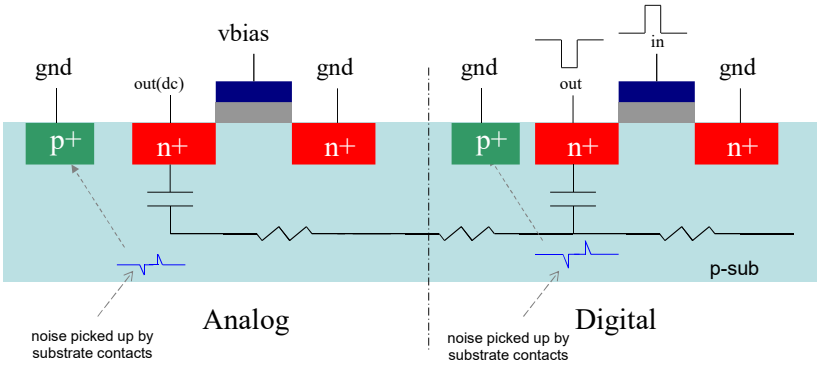
Noise decoupling and shielding

- Substrate noise causes Vt modulation due to body effect
- Substrate and well ties (guard rings) should be added to reduce the substrate noise
- Can be reduced by increasing the spacing between sensitive analog and switching digital blocks



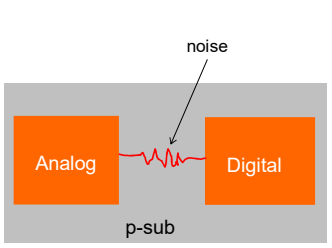
Noise decoupling and shielding

- **Substrate tie provides a low resistive path and the noise is picked-up thus avoiding any coupling with the signal**

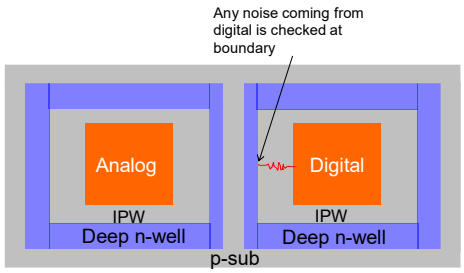


Noise decoupling and shielding

- **Isolated P-Well**
  - **Noise gets propagated through substrate as all the modules sits on a common sub**
  - **For better isolation modules can be put in separate p-wells**
  - **If possible put both analog as well as digital in IPWs**
  - **Use separate gnd connections for both the IPWs**



Noise coupling through substrate



Isolated P-Well (IPW)

Latchup guidelines

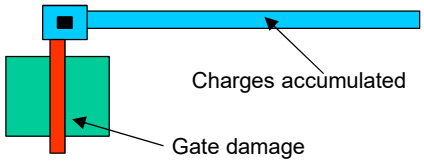
- Large area of well should not be left without ties – put as much ties as possible
- All p-type devices should be placed together and kept apart from n-type devices
- Double guard bar (both p and n) provides better immunity to latchup
- Floating bodies are prone to latchup – if putting the devices in IPW, make sure they are tied to gnd
- Supply and GND resistance should be as low as possible. If there is scope then stack supply and gnd line with multiple metals. Low GND resistance also enhances ESD
- If ESDs are sandwiched between two pads then makes sure that pmos faces pmos and nmos to nmos. The placement pattern should be

NMOS ESD1- PAD1 – PMOS ESD1 – PMOS ESD2 – PAD2 – NMOS ESD2
Or PMOS ESD1- PAD1 – NMOS ESD1 – NMOS ESD2 – PAD2 – PMOS ESD2

Avoid using the pattern: NMOS ESD1- PAD1 – PMOS ESD1 – NMOS ESD2 – PAD2 – PMOS ESD2

Antenna Effect

- During fabrication, plasma etching charges metal lines
- Degrades MOS Vt, or damage gate oxide

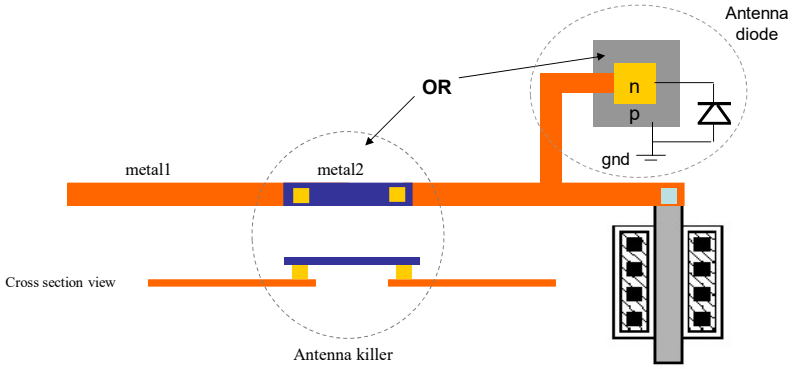


Antenna ratio = Area (metal) / Area (gate) < 70 (0.13µm process)

Although, rule for antenna ratio is technology dependent but should always be kept as low as possible

Antenna Guidelines

- Addition of antenna diode(p/n diffusion) prevents the gate damage due to charge injection by dissipating the charge
- The ratio of metal/gate poly area should be kept low to avoid the antenna effect
- Metal jumpers are used as antenna killers
- Large diodes are not used on high speed circuits to avoid the loading



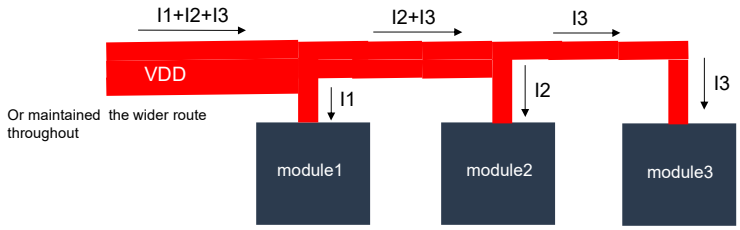
Electromigration

- Electromigration – higher flow of current through metal may cause melting of metal
- May be caused due to both peak as well as dc/avg current
- Width of the routes should be calculated as per the current
- Fingering/splitting of devices helps in improving electromigration
- Supply and gnd lines should be routed in higher metal and if possible stack with multiple metals
- High current lines shouldn't be routed a long way – place the module as close as possible to the source/sink
- 90deg bend in high current lines should be avoided – if process allows then use 45deg bend

Bending of a high current line

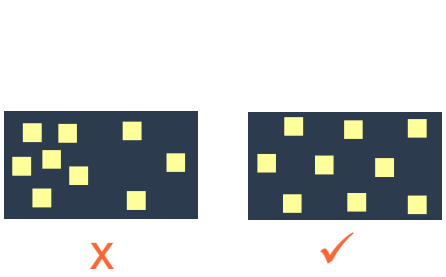
Electromigration

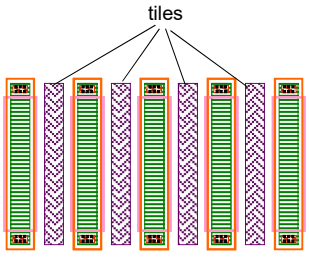
- For feeding multiple modules, the main supply width should be multiplied with the no. of modules



Tiling methodology

- Used to protect the oxide during CMP
- Tiles should be distributed evenly rather than concentrating in one area
- Automatic tiling is random so should be avoided for critically matched devices
- Tiling of matched devices should be taken care at module level and always done manually
- Stacking of metals helps in meeting tiling requirement

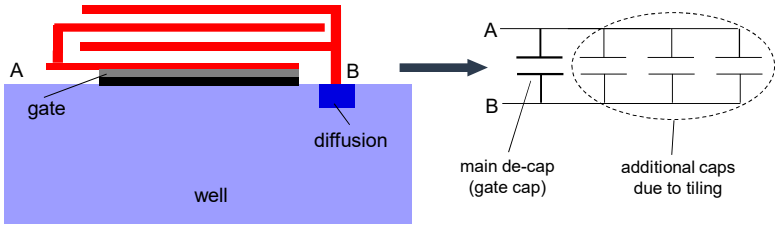




Tiling of matched resistors

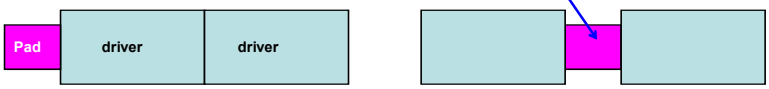
Tiling methodology

- Tiles over de-caps can be connected to the cap terminals to get additional caps

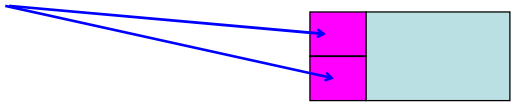


HV(Power) Layout Design Considerations

- Ron of the driver (Power FET) is quite critical so driver should be sized carefully
  - Total Ron = Ron of driver + routing resistance + bond wire resistance
- Driver occupies large portion of the die so inner bonding could be used to reduce the area
- Bond over Active (not supported by all processes) also helps in reducing area and Ron

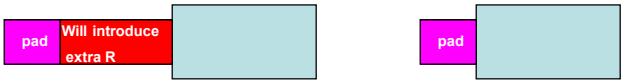


- Multi bonding techniques can be used to reduce the total Ron

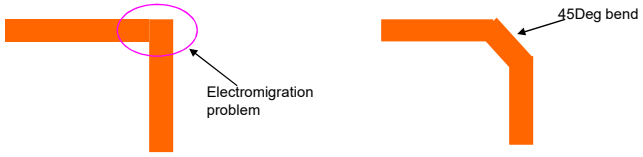


HV Layout Design Considerations

- Driver should be placed closest to the pad to reduce Ron and hence I^2R heat dissipation

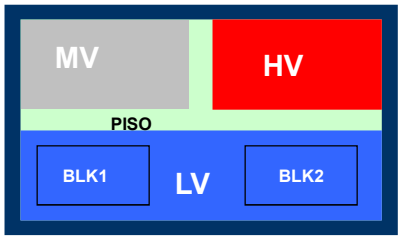


- High current carrying metal lines should be bent at 45deg instead of 90deg to avoid the electromigration



HV Layout Design Considerations

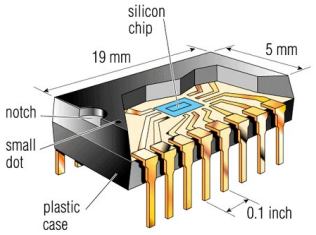
- LV, MV, HV circuits should be separated with the guard bars



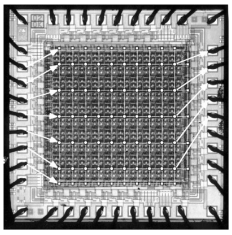
Sub-blocks of the same voltage ckts should be place together

- ESDs and clamping diodes should be placed at input to the chip

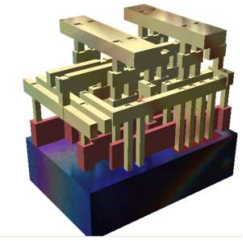
Chip Snapshots



Package



Bonding



A 3-metal silicon chip