Fixed Frequency Hysteretic Converter

EE5325 Power Management Integrated Circuits

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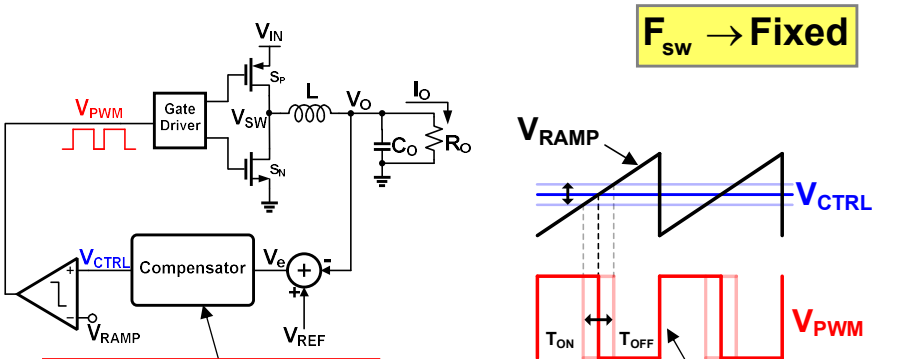
Switching Converter Control Techniques

PWM Control



Requires compensator
Limits BW to $1/10^{th} \cdot F_{SW}$

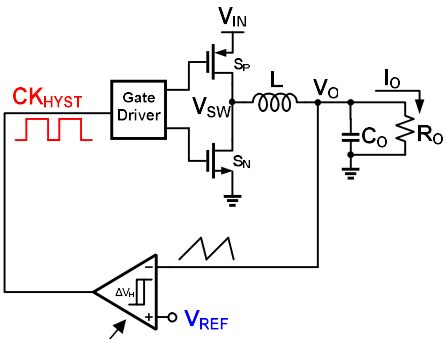
Slow transient response

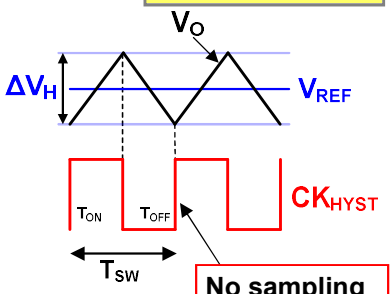
Switching Converter Control Techniques

Hysteretic Control

$$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{in}R_{ESR}t_d}$$

$F_{sw} \rightarrow$ Variable





No compensation is required
No 1/10th BW limitation

No sampling delay

Fast transient response

PWM Vs. Hysteretic Control

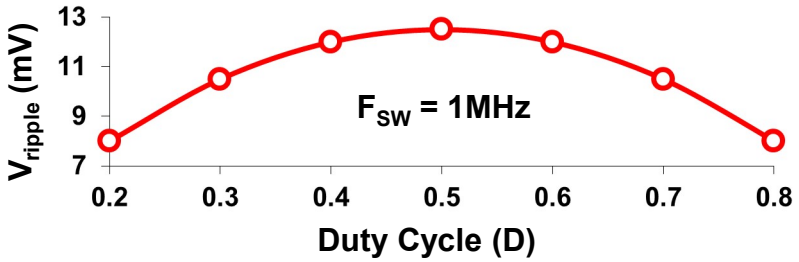
Hysteretic Control	PWM Control
▪ No compensation needed ☺	▪ Requires loop compensation ☹
▪ Fast transient response ☺	▪ Transient response limited by loop BW ☹
▪ Variable frequency ☹	▪ Fixed frequency operation ☺

Solution: Fixed frequency hysteretic control

Ripple of a Fixed Frequency Converter

- Output voltage ripple is a function of duty cycle (D) for fixed frequency

$$V_{ripple} \propto D(1-D)$$



Frequency of Hysteretic Converter

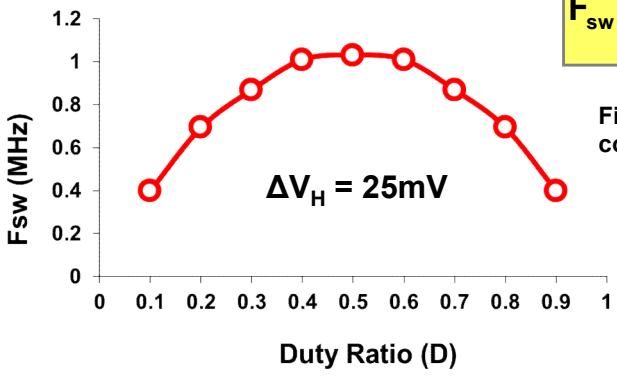
- Limiting the ripple between fixed hysteresis window (ΔV_H) varies switching frequency

Variable

$$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{in}R_{ESR}t_d}$$

Fixed in a hysteretic converter

$$V_{ripple} = \Delta V_H$$



Fixed Frequency Hysteretic Control

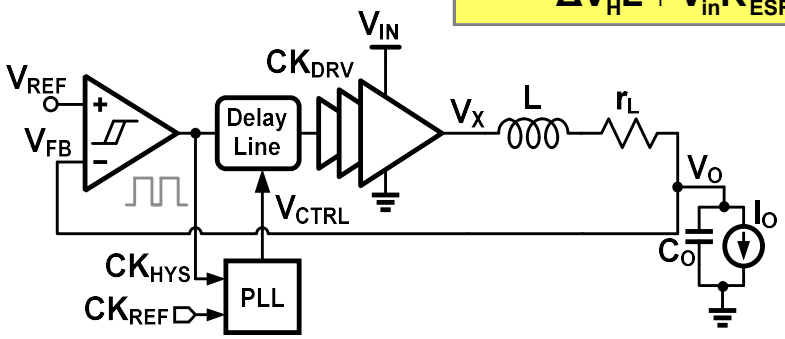
- **Two options to tune F_{SW}:**
  1. **Tune loop delay, t_d**
  2. **Tune hysteresis, ΔV_H**

$$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{in}R_{ESR}t_d}$$

Controlling t_d

- **PLL tunes t_d such that $F_{SW} = F_{REF}$**

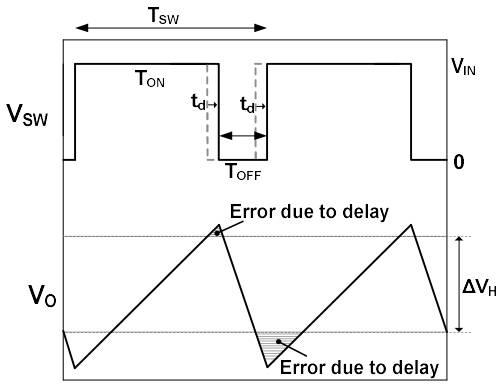
$$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{in}R_{ESR}t_d}$$



Chung-Hsien Tso, et al. *IEEE Power Electronics Letters*, Sept. 2003.

Drawbacks of t_d Control

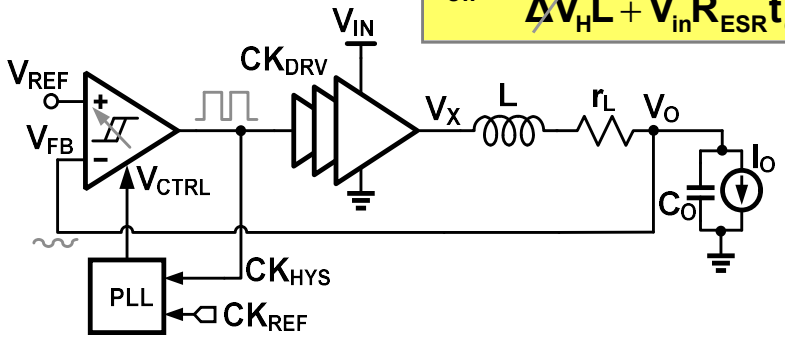
- Large t_d causes DC error
- Large t_d degrades transient response



Controlling ΔV_H

- PLL tunes ΔV_H such that $F_{SW} = F_{REF}$

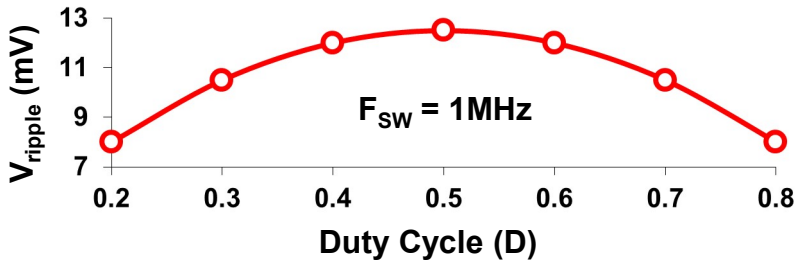
$$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{in}R_{ESR}t_d}$$



Y. Zheng, *et al.*, *IEEE TVLSI*, Jun. 2011.

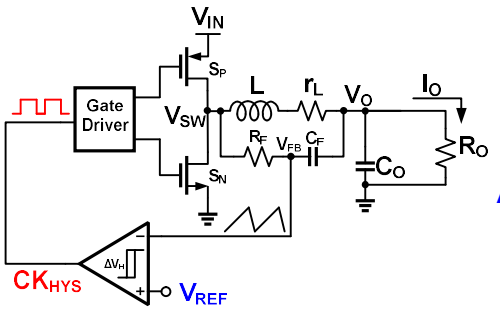
Drawbacks of ΔV_H Control

- Trade-off between accuracy and output ripple

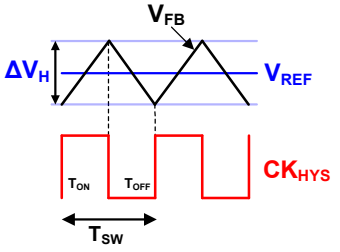


Current Mode Hysteretic Converter

- Uses internal ripple by emulating inductor current in R_FC_F filter
- Hysteresis (ΔV_H) and output ripple are independent



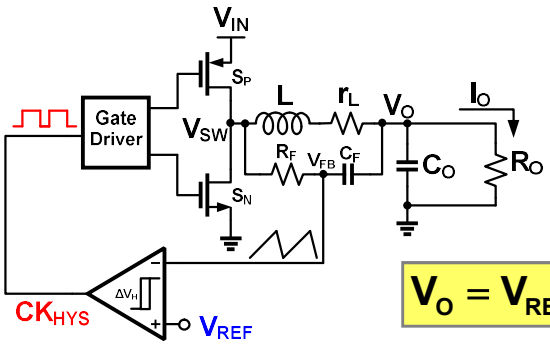
$$F_{sw} = \frac{V_{IN}D(1-D)}{\Delta V_H R_F C_F + V_{IN} t_d}$$



T. Nabeshima, et al, *IEEE Power Elect. Specialist Conf.*, 2004.

Drawbacks of CM Hysteretic Converter

- No dc feedback from output
- Poor load regulation due to r_L



$$V_O = V_{REF} - I_O r_L$$

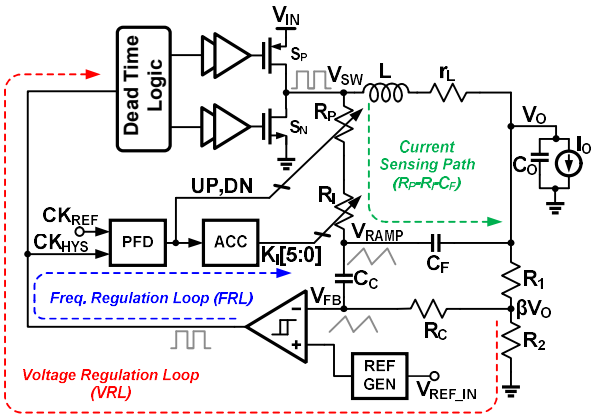
For example: I_O=1A, r_L=50m, Voltage error = 50mV

Trade-offs in Voltage & Current Mode

Voltage Mode	Current Mode
$F_{sw} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L + V_{IN}R_{ESR}t_d}$ $V_O = V_{REF}$	$F_{sw} = \frac{V_{IN}D(1-D)}{\Delta V_H R_F C_F + V_{IN}t_d}$ $V_O = V_{REF} - I_O r_L$
▪ Good load regulation ☺	▪ Poor load regulation ☹
▪ Large output ripple ☹	▪ Small output ripple ☺

Solution: Hybrid Voltage and Current Mode Hysteretic Control

Hybrid Hysteretic Control

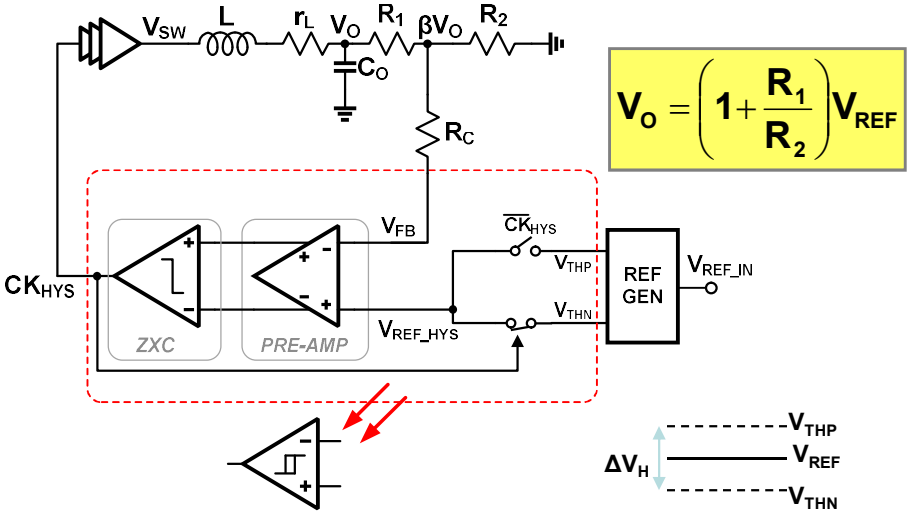


$$V_{FB} = \beta V_O + V_{RAMP}(ac)$$

VRL FRL

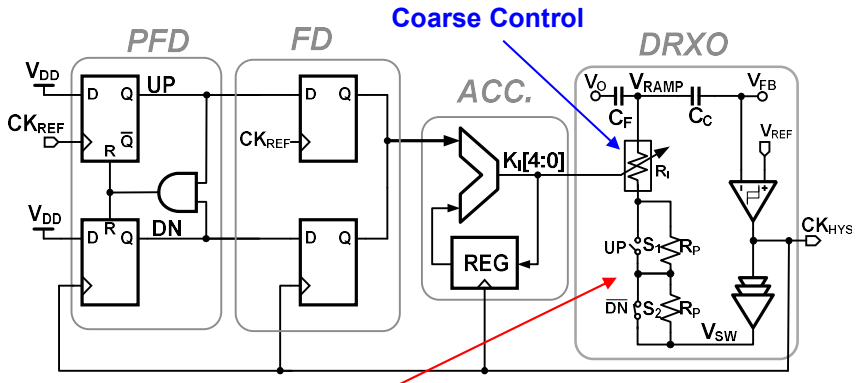
Q. Khan, et al, "A 900mA 93% Efficient 50uA Quiescent Current Fixed Frequency Hysteretic Buck Converter Using a Highly Digital Hybrid Voltage- and Current-mode Control," VSLI Symp., June 2012, Honolulu.

Voltage Regulation Loop (VRL)



$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

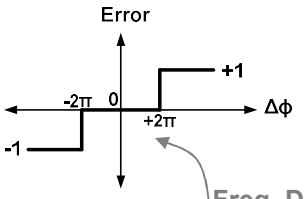
Frequency Regulation Loop (FRL)



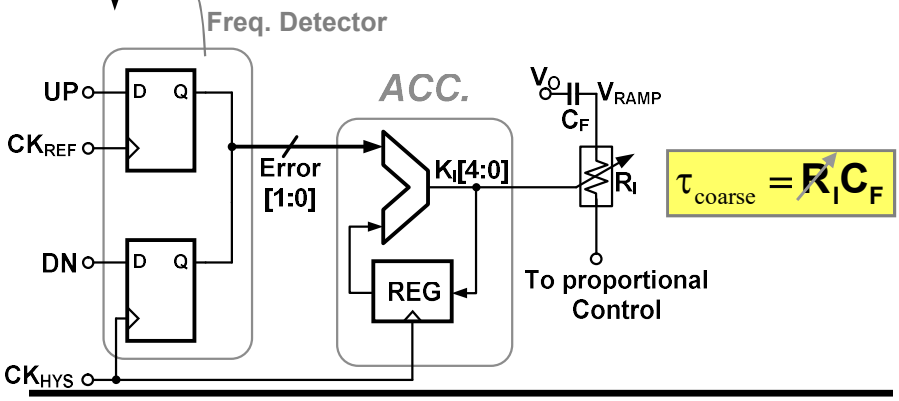
$$F_{sw} = \frac{V_{IN} D(1-D)}{\Delta V_H (R_I + R_P) C_F}$$

Coarse Fine

Coarse Control

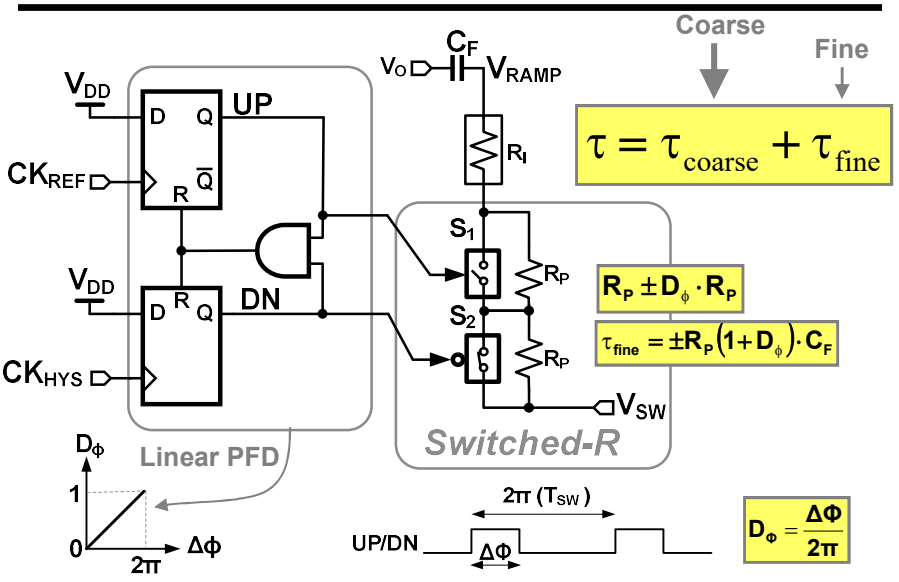


- Three level phase detector detects error when phase error exceeds ±2π
- Acts like a freq. only detector

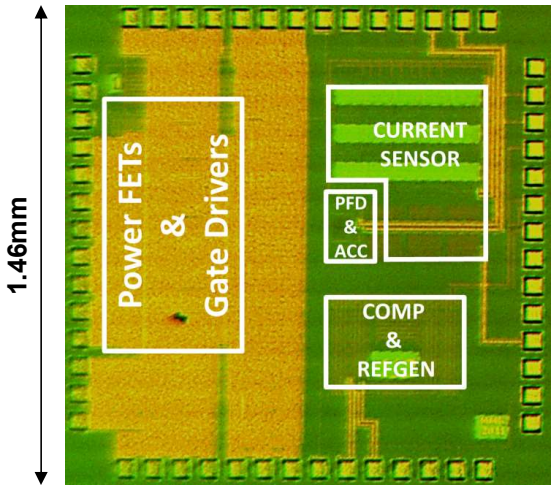


$$\tau_{coarse} = R_I C_F$$

Fine Control



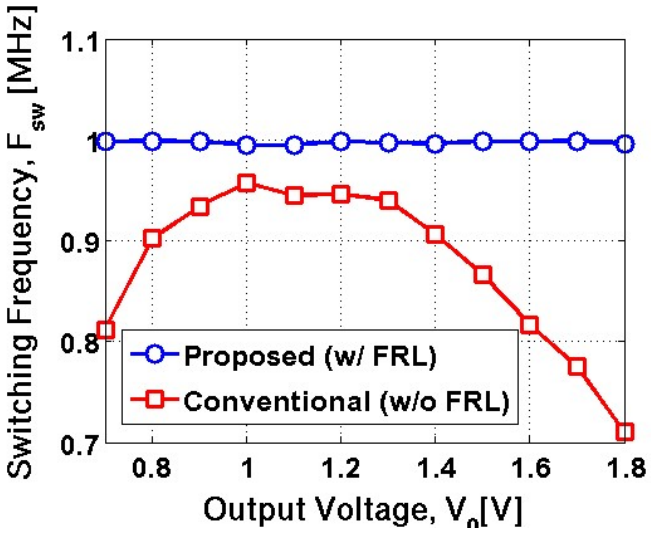
Implementation



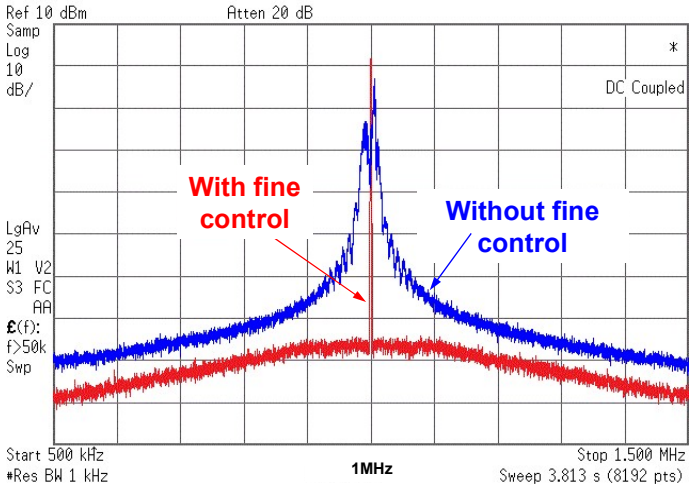
Process: 130nm CMOS

Active area: 0.713mm^2

Measured Results: F_{SW} Vs. V_O

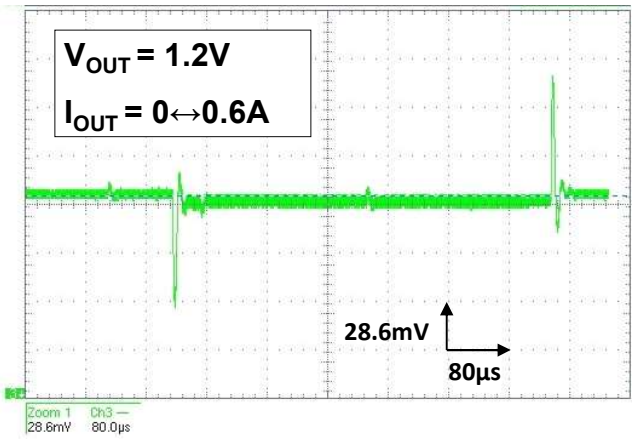


Measured Results: Clock Spectrum



Measured Transient Response

L=1.8µH, C=10µF



Measured Transient Response

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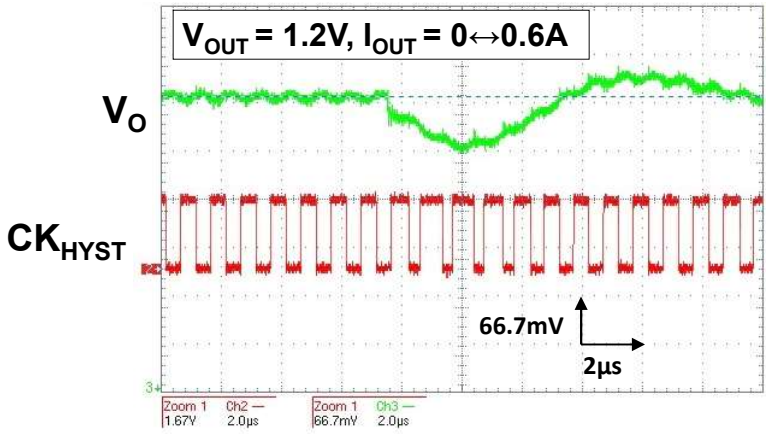
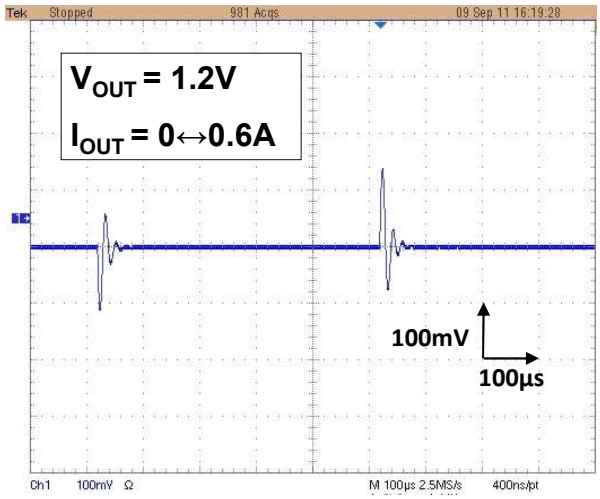
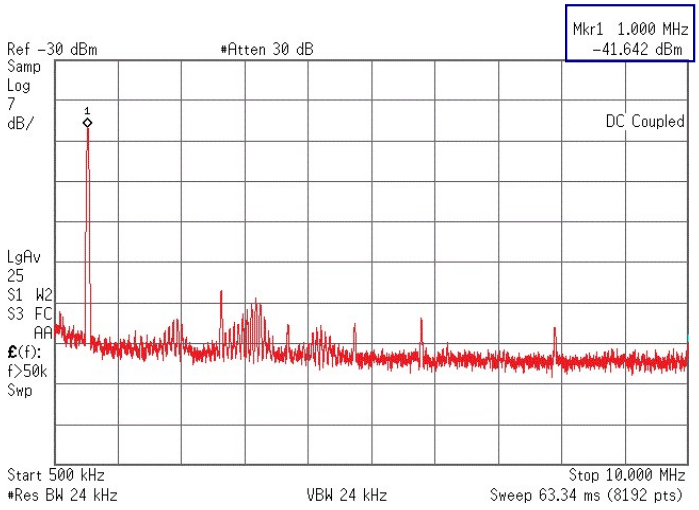


Measured Transient Response

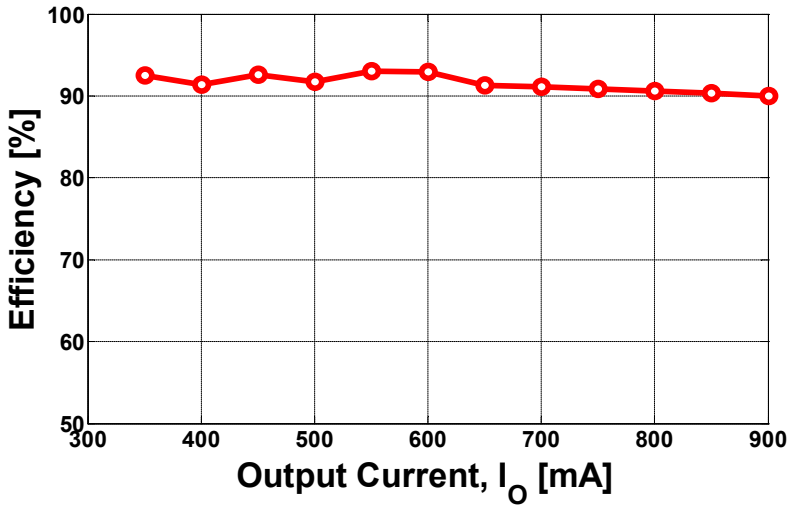
L=4.7µH, C=10µF



Measured Output Ripple



Measured Efficiency



Performance Summary

Fabrication Process	130nm CMOS
Die size with Pad	2.13 mm² (1.46mm x 1.46mm)
Active Area	0.713 mm²
Input Supply Voltage (Vin)	2.5V
Output Voltage Range (Vout)	0.7V – 1.8V
Inductor	1.8uH – 4.7uH (DCR 50mΩ – 70mΩ)
Capacitor	10uF (ESR <20mΩ)
Total on-chip Capacitor	50pF
External Compensation Cap.	None
Load Current	350mA – 900mA
Efficiency	90% - 93% @ Iload = 0.35A – 0.9A
Switching Frequency	1 MHz
Switching Frequency Variation	0.1% - 0.5%
Load Regulation	< 2mV / A
Line Regulation	5mV/V @ Vout = 1.2V
Load Transient (0 ↔ 600mA) Undershoot/Overshoot/Set.Time	@ 1.2V, L=1.8uH, C=10uF 61mV/72mV/< 10us
Output Ripple Quotient/switching Current (Iq)	5mV (p-p) 40uA