

Current Mode Control

EE5325 Power Management Integrated Circuits

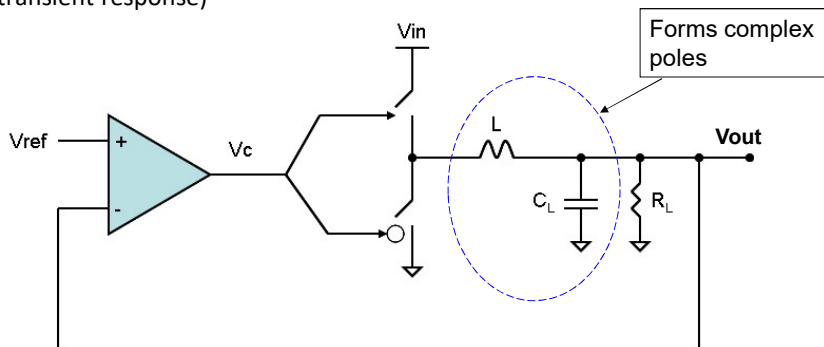
Dr. Qadeer Ahmad Khan

Integrated Circuits and Systems Group
Department of Electrical Engineering
IIT Madras



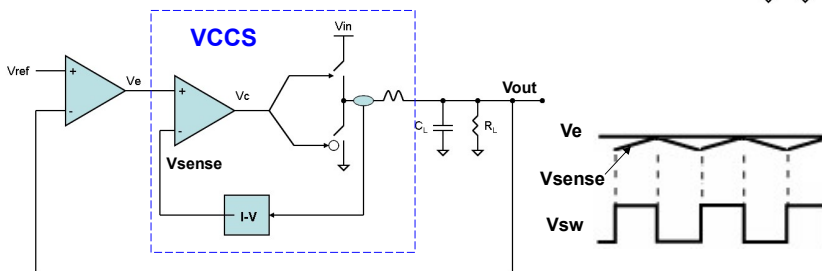
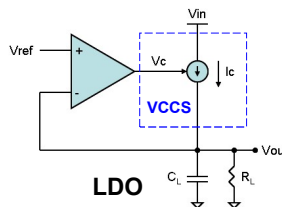
Voltage Mode Control

- Switch duty cycle controlled by the error voltage between output and reference
- L and C forms a pair of complex poles which makes the system inherently unstable
- Requires complex PID compensation to achieve high loop BW (good transient response)



Current Mode Control

- Uses concept of LDO Regulator where output voltage is by controlling the output current using VCVS
- In case of LDO, pass transistor acts as a lossy VCCS hence exhibits poor efficiency
- In case of current controlled dc-dc, Inductor is converted into a lossless VCCS

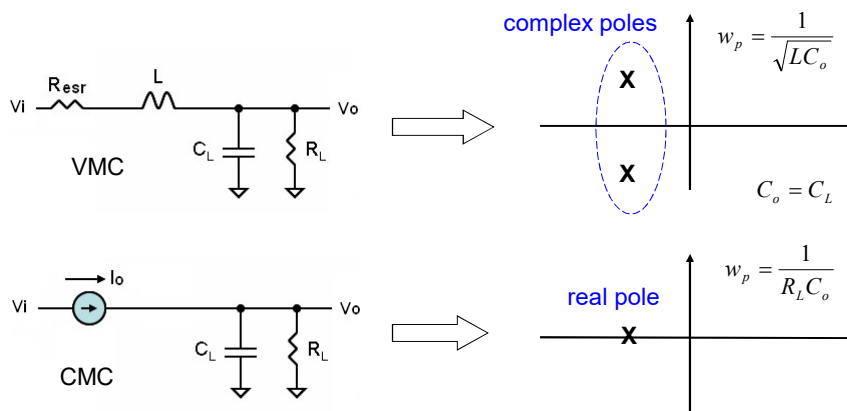


Current Mode Controlled DC-DC



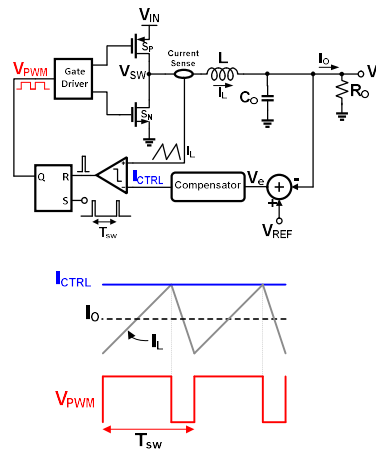
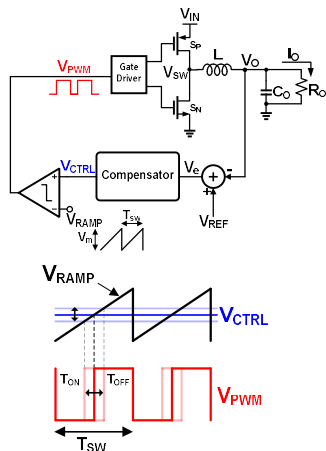
Complex – Real Pole Transformation

- Unlike the Voltage Mode controlled, the complex poles due to L & C is converted into real pole because of the inner current loop



Voltage Mode Vs Current Control

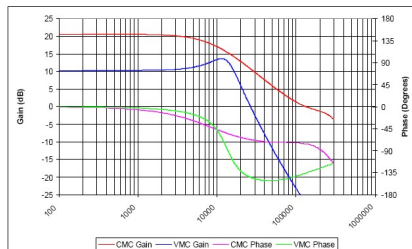
- Duty cycle is controlled only by voltage
 - Uses an external ramp
- Duty cycle is controlled by both voltage and current
 - Doesn't require external ramp



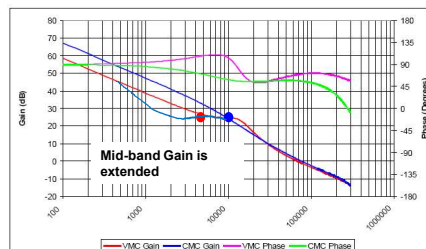
VMC vs CMC Frequency Response

- Phase and Magnitude roll-off in CMC is not as steep as in VCM
 - Smoother frequency response
- It becomes easier to stabilize the loop due to single pole
 - Only PI (type-II) compensation is required

Brian Lynch, "Current mode vs. voltage mode control in synchronous buck converter", Texas Instruments



Before compensation



After compensation



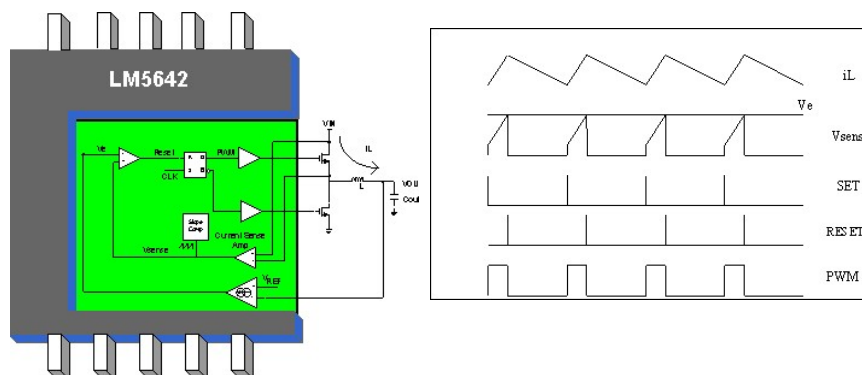
Current Mode Control Techniques

- **Peak Current Mode Control**
 - Peak Current (high side) is used to control the duty cycle
- **Valley Current Mode Control**
 - Valley current (low side) is used to control the duty cycle
- **Emulated Current Mode Control**
 - Both peak and valley currents are used to control the duty cycle



Peak Current Mode controlled

- Senses the peak inductor current information when the power switch is on, then uses it to turn off the switch → trailing edge PWM
- Suffers from sub-harmonic oscillation at duty cycles higher than 50%
- Easy to operate at higher duty cycle but difficult at lower duty cycle



Voltage Mode Control (VMC) vs. Current Mode Control (CMC)

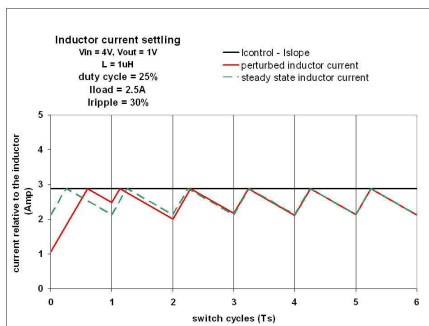
| Parameter | VMC | CMC |
|-------------------------------|--|--|
| Line transient | Good with line feedforward $(V_M \propto V_{IN})$ | Good (inherent line feedforward in peak current mode) Bad in valley CMC |
| Load transient | Good (bandwidth is independent of load current in CCM) | Good at high BW but degrades at lower load current (BW is dependent on load current) |
| Very low duty cycle operation | Good | Poor |
| Noise insensitivity | Good | Poor |
| Compensation | Complex (Type-III) | Simpler (Type-II) |



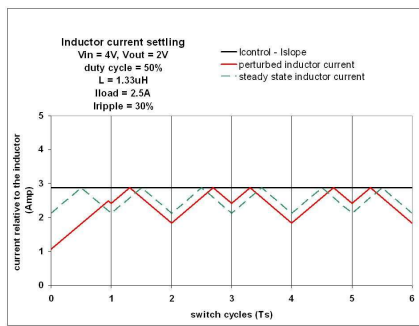
Sub-harmonic Oscillations

- Caused due to instability in the current loop

Peak CMC



D < 0.5 (Stable)

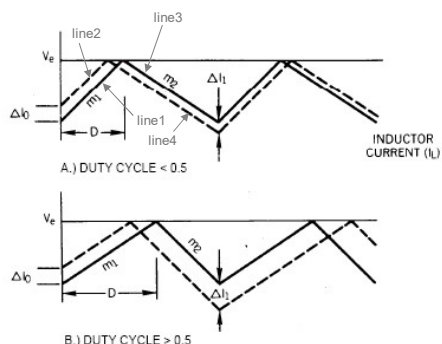


D > 0.5 (Un-stable)



Current loop instability

- Current Loop suffers from sub-harmonic oscillations when $D > 0.5$ (for peak CMC) and $D < 0.5$ (for valley CMC)
- This sub-harmonic oscillation is suppressed by adding a compensating ramp in the control signal



Using eq. of straight line

For line1, $i_1 = m_1(T_0) + I_0$

For line2, $i_1 = m_1(T_0 - \Delta T_0) + I_0 + \Delta I_0$

Subtracting two eq.

$\Delta T_0 = \Delta I_0 / m_1$

similarly line3 and line4 gives

$\Delta I_1 = -m_2 \Delta T_0$

Substituting ΔT_0 , we get

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1} \right) \quad (1)$$

Case-1: $D < 0.5 \rightarrow m_1 > m_2 \rightarrow \Delta I_1 < \Delta I_0$; stable

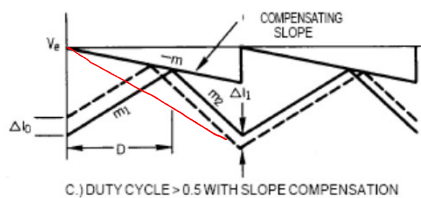
Case-2: $D = 0.5 \rightarrow m_1 = m_2 \rightarrow \Delta I_1 = \Delta I_0$; critically stable

Case-3: $D > 0.5 \rightarrow m_1 < m_2 \rightarrow \Delta I_1 > \Delta I_0$; unstable



Ramp Compensation

- The current loop is stabilized by adding a small ramp in the current or subtracting the same from error signal



$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 - m}{m_1 + m} \right) \quad (2)$$

Disturbance after n cycles:

$$\Delta i_n = \left(-\frac{m_2 - m}{m_1 + m} \right)^n \cdot \Delta i_0 \quad (3)$$

Hence to ensure the stability of current loop Δi_n should die out $\rightarrow (m_2 - m) < (m_1 + m)$

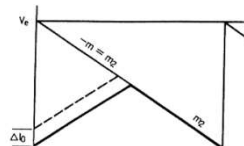
Stability Condition: $\Delta i_n / \Delta i_0 < 1$

Can be achieved by two ways

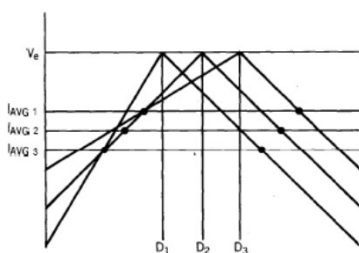
$$m > \frac{1}{2} m_2 \quad \text{OR} \quad m > \frac{1}{2} (m_2 - m_1)$$

Substituting both the case in (3) results in $(m_2 - m) < (m_1 + m)$ hence satisfying the condition of stability

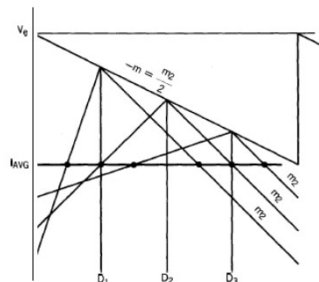
Ideal slope for compensating ramp, $m = m_2$ causes the output to settle in one clock cycle



Ramp Compensation



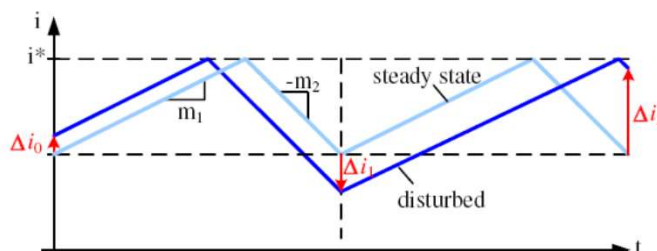
PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION
ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH
DUTY CYCLE



- AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUN
CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE
COMPENSATION OF $m = -\frac{1}{2} m_2$.



Slope Compensation

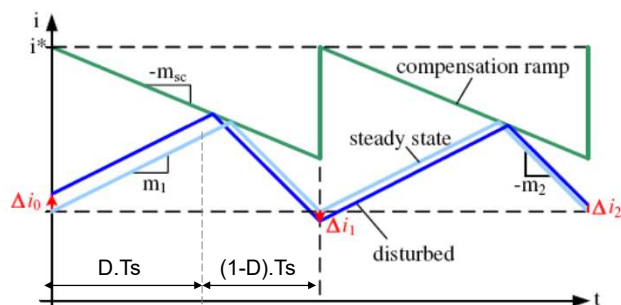


Disturbance after n cycles:
$$\Delta i_n = \left(-\frac{m_2}{m_1} \right)^n \cdot \Delta i_0$$

Condition for stable operation:
$$m_1 > m_2 \quad (D < 0.5)$$



Slope Compensation



$$\frac{m_2}{m_1} = \frac{D}{1-D}$$

Disturbance after n cycles:

$$\Delta i_n = \left(-\frac{m_2 - m_{sc}}{m_1 + m_{sc}} \right)^n \cdot \Delta i_0$$



Required compensation:

$$m_{sc} > \frac{1}{2}(m_2 - m_1)$$



Adaptive Slope Compensation

$$m_{sc} > \frac{1}{2}(m_2 - m_1) \rightarrow \frac{1}{2}m_1 \left(\frac{m_2}{m_1} - 1 \right) \quad (1)$$

$$\frac{m_2}{m_1} = \frac{D}{1-D} = \frac{V_{out}}{V_{in} - V_{out}} \quad (2) \text{ For buck: } D = V_{out}/V_{in}$$

substituting (2) in (1)

$$\Rightarrow m_{sc} > \frac{1}{2}m_1 \frac{V_{in}}{V_{in} - V_{out}} \quad \text{or} \quad \frac{m_{sc}}{m_1} > \frac{1}{2} \frac{V_{in}}{V_{in} - V_{out}}$$

$$\text{also } m_1 = \frac{V_{in} - V_{out}}{L} \Rightarrow m_{sc} > \frac{V_{in}}{2L}$$

The optimum slope compensation can be calculated by knowing one of the followings:

- m_1 , V_{in} and V_{out}
- V_{in} and L

