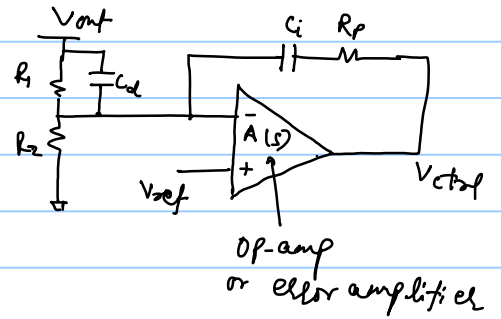
## Error Amplifier




① Bandwidth of op-amp should be high enough not to interfere with loop gain T.F.

op-amp $\omega_{ugb} \geq 10\times$ dc-dc $\omega_{ugb}$

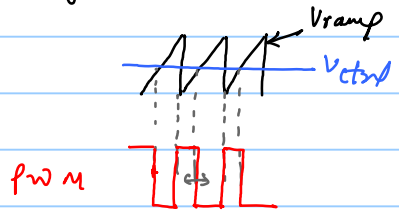
$$A(s) = \frac{A_0}{1 + s/\omega_p}$$

② High frequency poles (outside $\omega_{ugb}$) in type-III compensator help in suppressing resonance which might occur due to internal poles of op-amp.

③ Any op-amp topologies can be used.

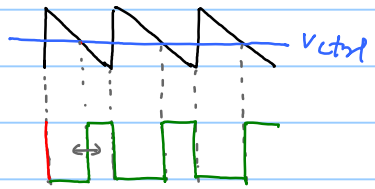
## Delays associated with PWM modulator

### Trailing edge




$T_d = (1-D)T_{sw}$

### Leading Edge

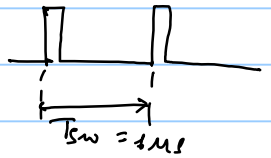



$T_d = D.T_{sw}$

## Pulse Skip Mode (PSM) & Pulse Frequency modulation (PFM)

→ used in light load condition or when duty cycle is saturated

$D_{min} \rightarrow T_{on\_min}$

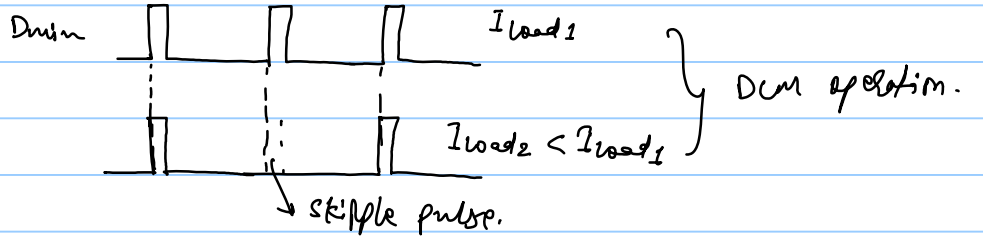



$T_{on\_min} = 50ns$

$D_{min} = 5\%$

To operate at below 5% duty cycle, $T_{OFF}$ must be increased.

One way is to reduce the switching freq. while keeping $T_{on}$ fixed at $T_{on\_min}$.




1:1 → $D_{min}$:0

For higher resolution

10 Duty : 0

9 Duty : 0

8 Duty : 0

⋮

Duty : 0

Duty : 20%

" : 30%

" :

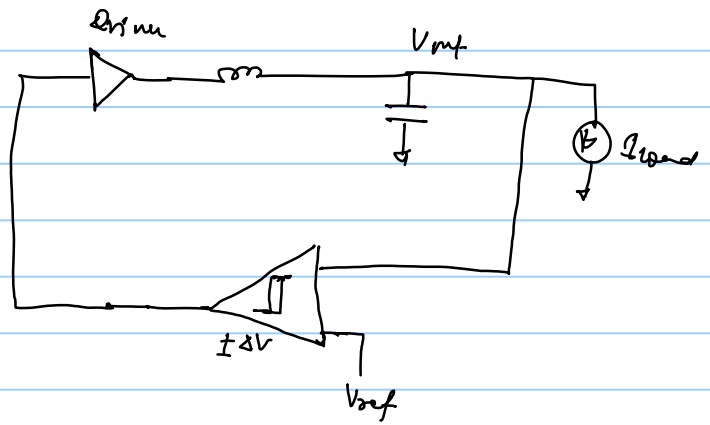
⋮

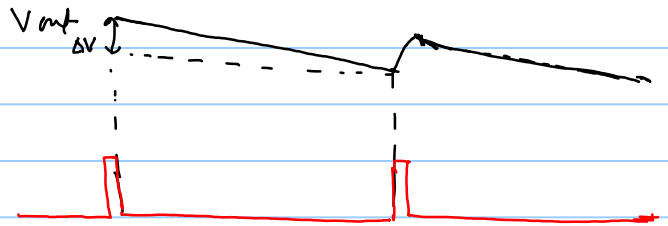
10 @ 0%

PSM → digital way of implementing PFM.

PFM → Instead of Vctrl controlling the duty cycle, it controls only $T_{OFF}$.

$T_{OFF} \longrightarrow \frac{1}{I_{Load}}$


Vout
Iload
Isv
Vref


Vout
ΔV