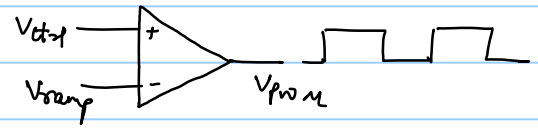
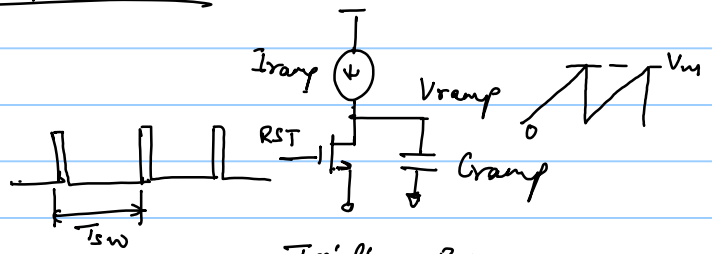
PWM Modulator



1. Ramp Generator / Oscillator
2. Comparator.

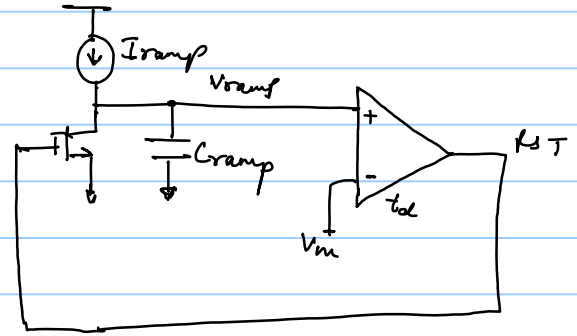
Ramp Generator

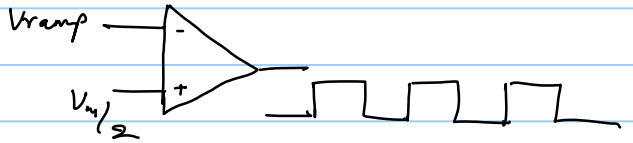


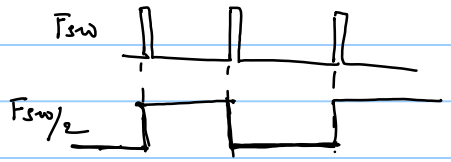
Trailing Edge.

$$I_{ramp} = \frac{C_{ramp} V_m}{T_{sw}} \Rightarrow V_m = \frac{I_{ramp} T_{sw}}{C_{ramp}}$$

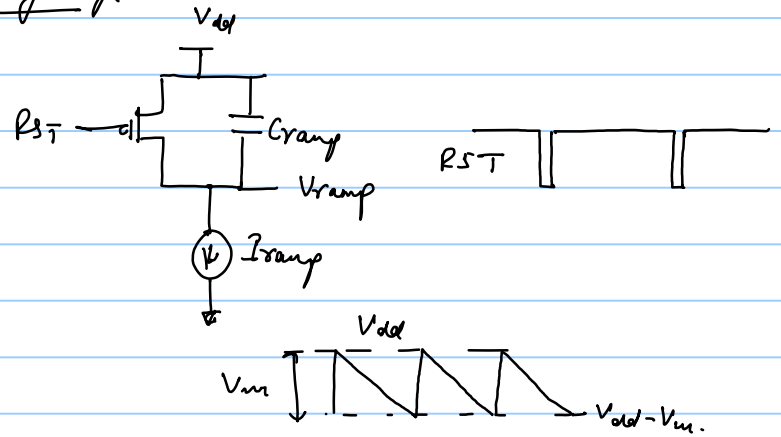
$$V_m = \frac{I_{ramp}}{C_{ramp} F_{sw}}$$





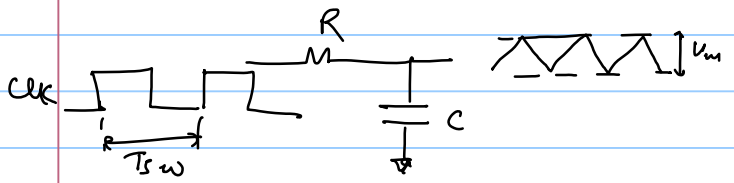


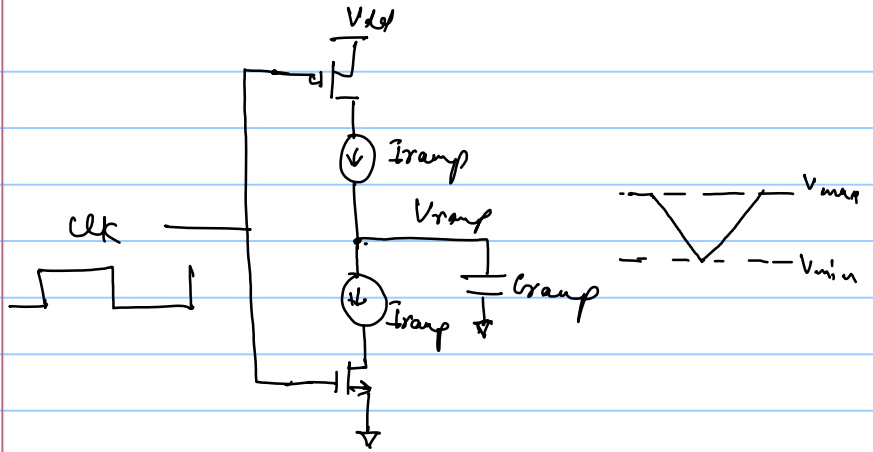
Leading Edge



Dual Edge Modulator

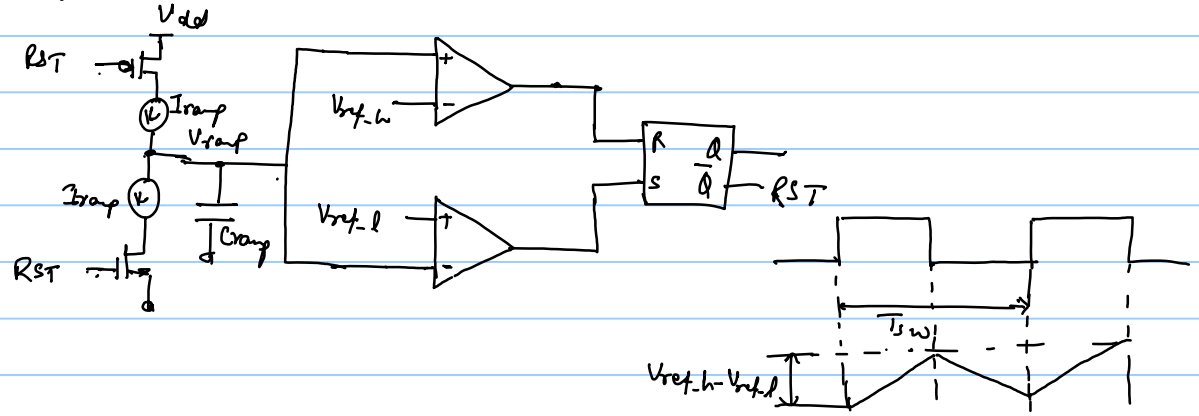
For small V_m $\left(< \frac{1}{10} V_{dd} \right)$



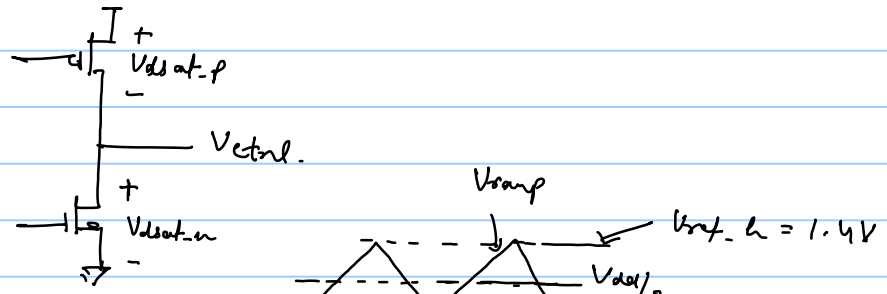


Any mismatch between top & bottom currents will get integrated and Vramp will saturate.

Triangle wave generator



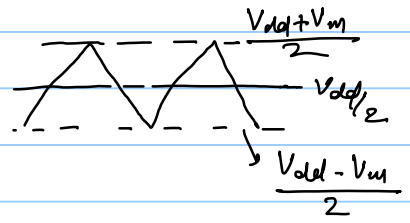
2nd stage of error amplifier



$V_m = 1V$

$V_{dd} = 1.8V$

Keeping common mode voltage of $V_{ramp} = V_{dd}/2$ ensures enough headroom for both NMOS & PMOS to keep them in saturation for entire duty cycle range (0 — 100%)



Shifting the common mode of single edge modulator.