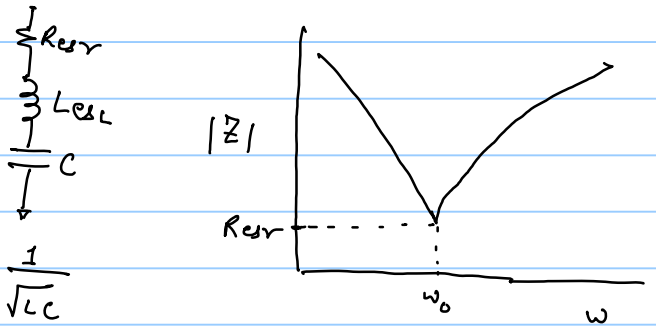
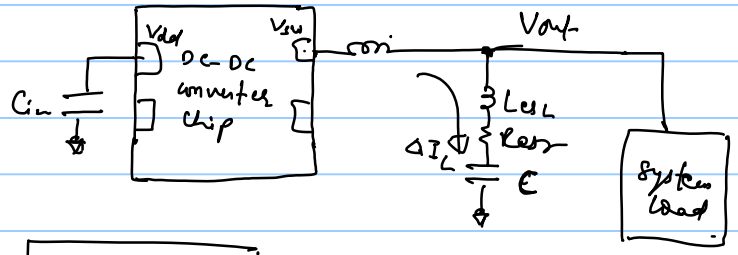
ESL in capacitor.



$$\omega_0 = \frac{1}{\sqrt{LC}}$$

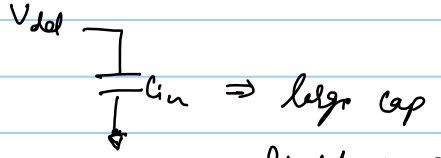


$$V_L = L \frac{di}{dt}$$

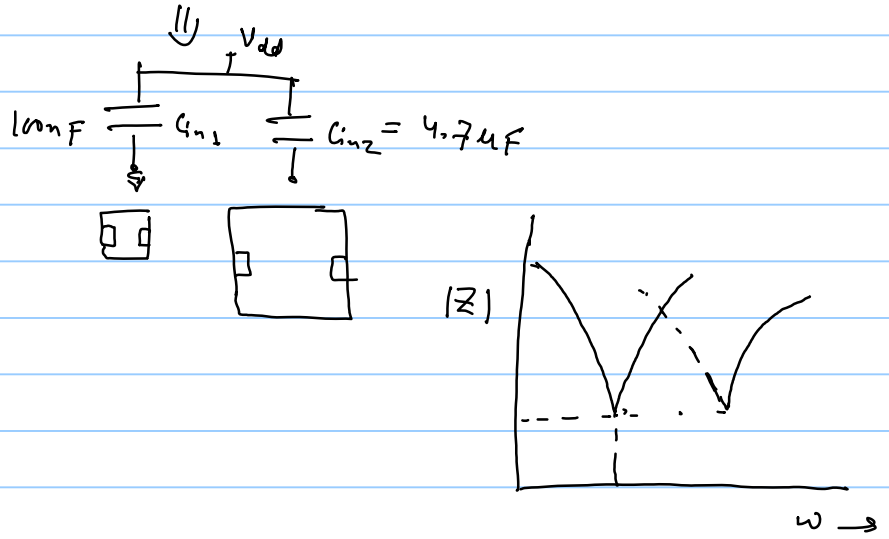
$L = 1\mu H$, $di = 1A$

$dt = 1ns$

$V_L = 1V$

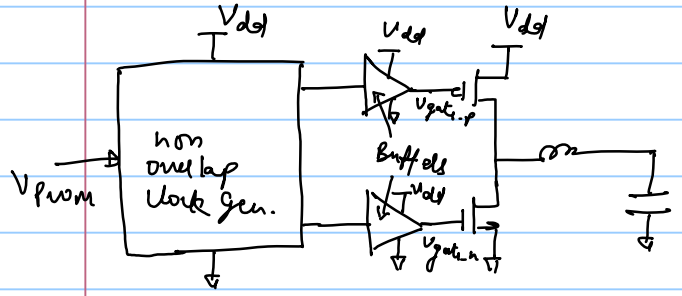


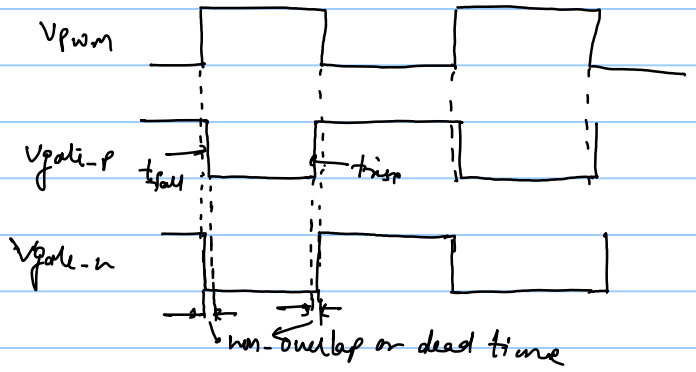
⇒ large cap to place closer to V_{dd} pin due to limited space



Gate driver Circuit

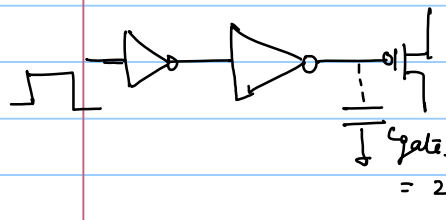
= non-overlap clock generator + Gate buffer





t_{fall} & t_{rise} → 1 - 2ns

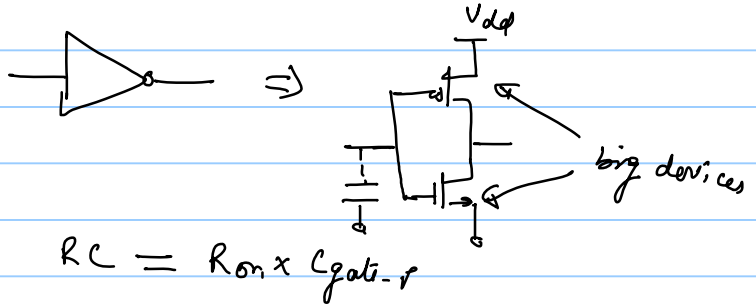
t_{dead} → 1 - 2ns



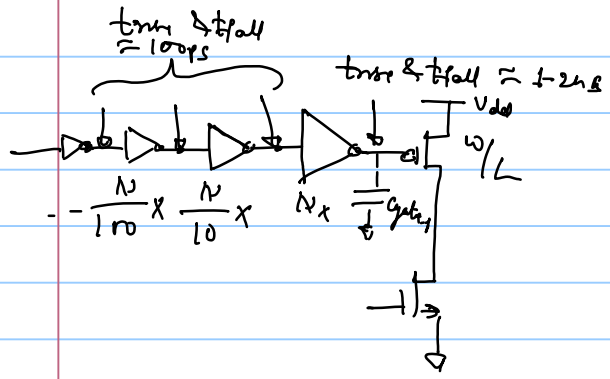
$t_{rise} = t_{fall} = 1ns$

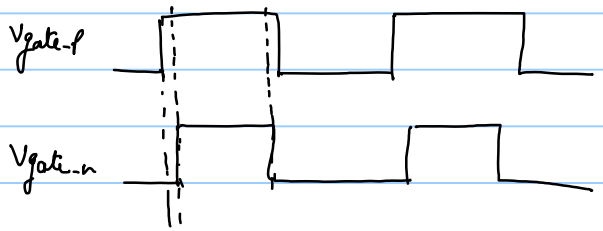
2 to 3 RC time constant $\simeq 1ns$

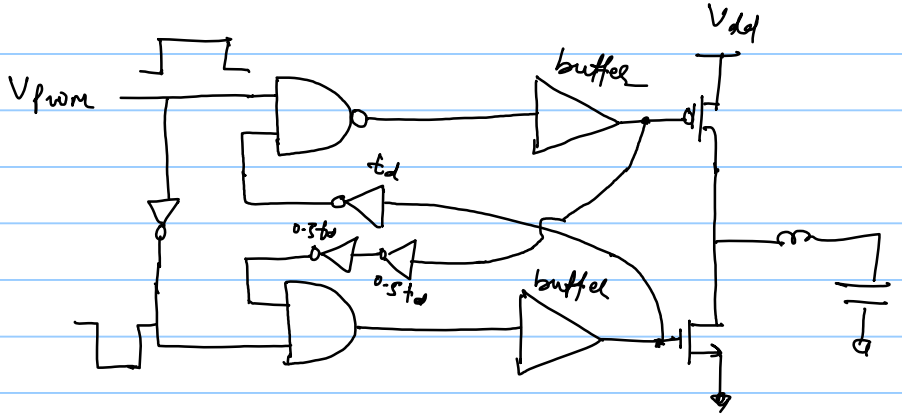
$RC \simeq 0.5\ ns$



$RC = R_{on} \times C_{gate\_p}$


trise & tfall
≃ 100ps
trise & tfall ≃ 1-2ns
Vdd
W/L
N/100 X
N/10 X
Nx
Cgate


Vgate-p
Vgate-n


Vpwm
buffer
Vdd
td
0.5td
0.5td
buffer