

Mitigating the effect of R.H.P. zero

Method -1: Nulling Resistor.

$$\rightarrow R_c > \frac{1}{g_m 2}$$

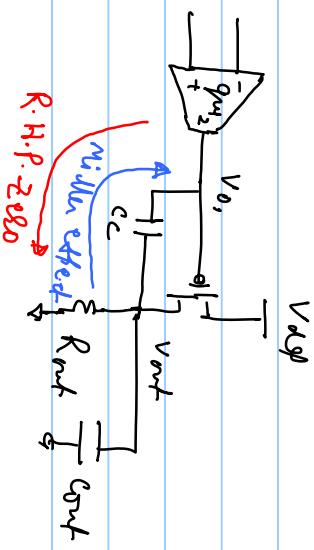
R.H.P. will go away or convert to L.H.P.

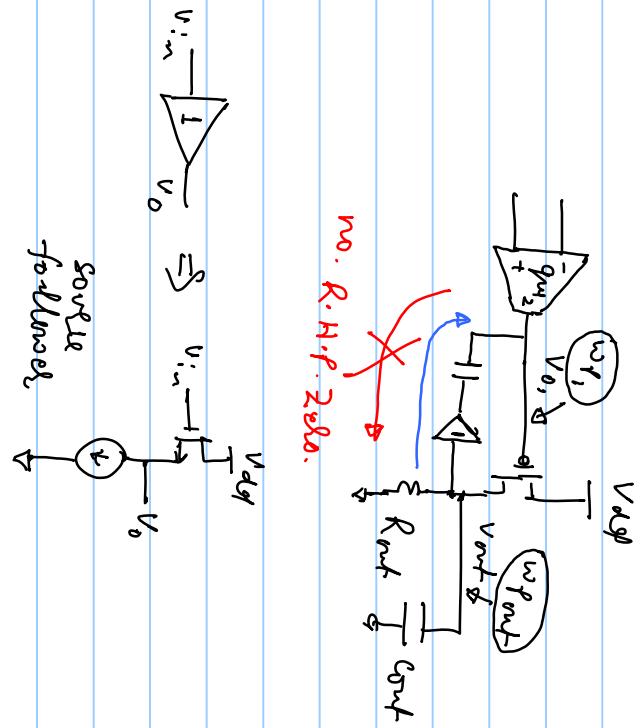
Method -2

choose $g_m 3 > g_m 2$

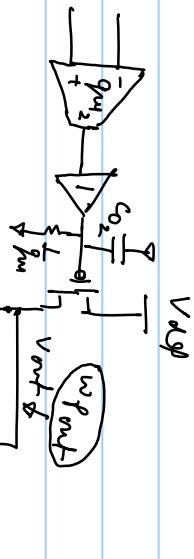
so R.H.P. is pushed at high freq.
and phase margin is not affected.

Method -3





Reducing the effect of w_1 if w_{nt} is dominant



$$w_{P_1} = \frac{g_m}{C_{02}} \gg \frac{1}{R_{02} C_{02}}$$

Reducing the gate capacitance.

V_{dsg}

$$V_dsg = \begin{cases} 100mV & V_{dsg} > V_{th} \\ -100mV & V_{dsg} < V_{th} \end{cases} \quad \text{if } V_{dsg} = 100mV$$

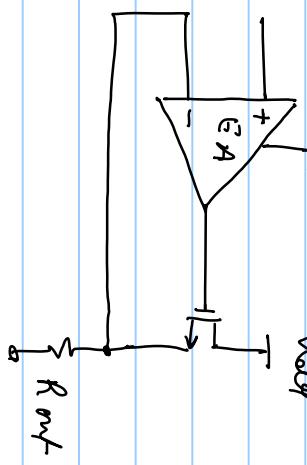
$$V_g = V_{dsg} - 100mV$$

$$V_D > V_{TH} + V_{DEP} - 10mV$$

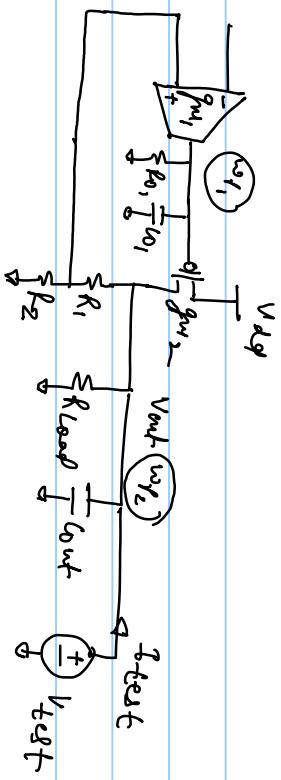
$$V_{TH} = \frac{V_{DD}}{2} + V_{DSAT}$$

$$V_D > V_{DSAT} + V_{DSAT}$$

$$V_{DSAT} = \frac{V_{DD} - 3mV}{2}$$



Output Impedance of PMOS LDO



$$R_{out} = (R_1 + R_2) // r_{o2} // R_{load}$$

$$R_{out} = \frac{V_{test}}{I_{test}}$$

ΔQ c output impedance.

$$Z_{out}(dc) = \frac{R_{out}}{1 + \beta A_o}$$

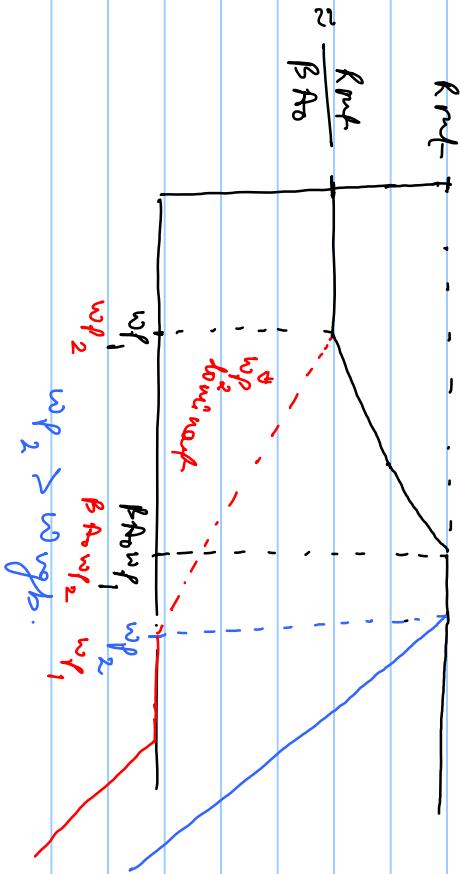
$$A_o = g_m, R_o, \times g_m \times R_{out}$$

$$\begin{aligned} Z_{out} &= \frac{R_{out}/(1 + R_{out} \text{const})}{1 + \beta A_o} = \frac{R_{out}}{(1 + \delta l_{wp_2})(1 + \beta \frac{R_o}{l + \delta l_{wp_1}})(1 + \delta l_{wp_2})} \\ &= \frac{R_{out}}{\overbrace{(1 + \delta l_{wp_2})}^{\text{const}} \overbrace{(1 + \delta l_{wp_1})}^{\text{const}} \overbrace{(1 + \delta l_{wp_2})}^{\text{const}}} \end{aligned}$$

$$= \frac{R_{mt} (1 + \delta / w_{p_1})}{(1 + \delta / w_{p_1})(1 + \delta / w_{p_2}) + \beta_{A_0}}$$

for $w \ll w_{p_0}$

$$\frac{Z_{mt}}{R_{mt}} = \frac{R_{mt} (1 + \delta / w_{p_1})}{1 + \delta / w_{p_1} + \beta_{A_0}} = \left(\frac{R_{mt}}{1 + \beta_{A_0}} \right) \frac{(1 + \delta / w_{p_1})}{1 + \delta / (1 + \beta_{A_0}) w_{p_1}}$$



$$\frac{Z_{mt}}{R_{mt}} \approx \frac{R_{mt}}{\beta_{A_0}}$$

$$w_{p_2} > w_{p_0}$$

